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Implementation of DDS Based Harmonic Signal Generator

P. Poornima, Solomon Gotham

Abstract: ***A harmonic signal generator with adjustable frequency, phase and harmonic proportion is designed in this paper. The design of this harmonic signal generator is based on direct digital frequency synthesis (DDS) technology. The classic structure of DDS is introduced and a kind of compression ROM is designed. Then, the DDS core with compression ROM is compiled using Xilinx Xc3s500e fpga by VHDL language. The performances such as integration, expansibility are very much improved. The principle of DDS is discussed particularly; the optimized structure of DDS core is presented in this paper. The total power consumption of the device was foundto be 0.081W.***

Key Words: DDS, SOPC, harmonic signal generator, Noise

I. INTRODUCTION

In modern industrial detection and communication, a signal generator has gained increasing applications. Especially the harmonic signal generator with adjustable frequency and phase is very much preferred. In addition, in some special situation such as power system, the harmonic proportion control and the multi-channels and the mixing-frequency sine wave output are demanded. Currently available signal generators are mainly based on the DDS technology. The DDS technology was presented by Tierney, Rader and Gold in 1971 [1]. It is a kind of frequency synthesis technology which directly synthesizes waveform on the basis of phase. The classic structure is also introduced by Tierney, Rader and Gold in 1971. With the development of microelectronic technology, more and more single channel DDS chips are made by chips supplier such as analog device Inc. and so on. The DDS is very much preferred in some modern communication and detecting systems owing to its advantages, e.g. ,fast switching, fine frequency resolution, low phase noise, continuous-phase frequency switching. However, the limitations of single channel DDS chips are serious problem. The system with multi-channels adjustable

frequency, phase and harmonic proportion is very huge and

expensive if it is made with single channel DDS chips. And

it is difficult to be controlled flexibly. As the appearance of

Field Programmable Gate Array (FPGA) chips, FPGA is used to realize DDS logic to meet different demand of the user. But it also has the problem to be controlled flexibly.

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In1990s, the concept of system on chip (SOC) is presented. In one system, a several function modules are integrated in one silicon chip. So, the integration of the system is improved, the mount of the chips and the PCB connection between chips are reduced, and the performance and function of system are improved very much. As the development of Field FPGA chips, it is possible that embed the CPU in FPGA chips. Xilinx Inc. and Xilinx Inc. supply the solution of System on a Programmable Chip (SOPC). SOPC is an on chip reconfigurable system based on FPGA. It integrates processor, me morizer, I/O ports and other necessary modules into a holonomic system which is designed for realizing some logic functions. SOPC is a flexible and effective SOC solution because of its flexibilities on system design, reduction, extension, upgrading, etc. And its hardware and software system are programmable [2]. So, the idea of the SOPC could be adopted when the signal generator is designed to resolve the control problem. In this paper, a signal generator with adjustable frequency, phase and harmonic proportion is designed. A FPGA chip is used to realize the DDS logic and other modules. A kind of soft core Nois II is embedded in FPGA chip to make the system controlled flexibly [3]. Besides, some simple circuits are designed to make the output signals stable and pure.

I. PRINCIPLE OF DDS SYNTHESIS

The direct digital frequency synthesis is a new frequency synthesis technology which directly synthesizes waveform on basis of phase. Using the relationship between phase and amplitude, the phase of waveform is segmented and assigned to relevant addresses [4]. DDS technology has a lot of advantages such as fast switching, fine frequency resolution, low phase noise, continuous-phase frequency switching and so on. The principle of DDS is easy to understand. Firstly, a single frequency sine signal should be sampled for one period with the satisfaction of Shannon Sampling Theorem. It is assumed that we sample N 2 points in one period of sine signal, and then put the points into a ROM which has N 2 addresses. We convert the order of the above course. The data stored in the ROM are outputted firstly. If the sampling frequency is the output frequency of the sampled data in the ROM [5], the output data could form sine wave and the frequency of the output sine signal is stored in the ROM are outputted firstly. If the sampling frequency is the output frequency of the sampled data in the ROM [5], the output data could form sine wave and the frequency of the output sine signal is

$$f_o = \frac{M}{2^N} f_c$$

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f_o – the frequency of output sine wave

f_c – the sampled frequency (the base clock)

M – the step of the address of output data

N – the number of ROM's address lines

Via the above formula, given constant clock frequency, the frequency of the output sine wave can be controlled with the control of parameter step M. Besides, the initial phase could also be changed with the change of the output position of the sampled sine wave serial. The position of the sampled data serial is transformed the address of the ROM. When the address of the ROM is over 11 …11 (N bits), it means the phase of the output sine wave is over one period. The address will start from begin again. So with the address of the ROM accumulated with the step M, the continuous sampled data of sine wave is outputted. And the frequency of the output sine signal is related with the step M. Through the digital to analog converter (DAC) and the low pass filter, a sine wave whose frequency and phase can be controlled is outputted [6]. The principle of the DDS is showed in Figure 1.

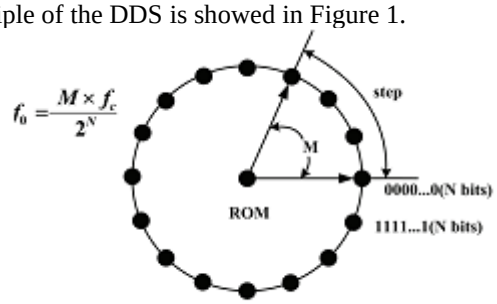

Fig 1. Principle of the DDS.

The classic constructer of the DDS is composed of Numerically Controlled Oscillator (NCO), Digital to Analog Converter and Filter. It is showed in Figure 2.

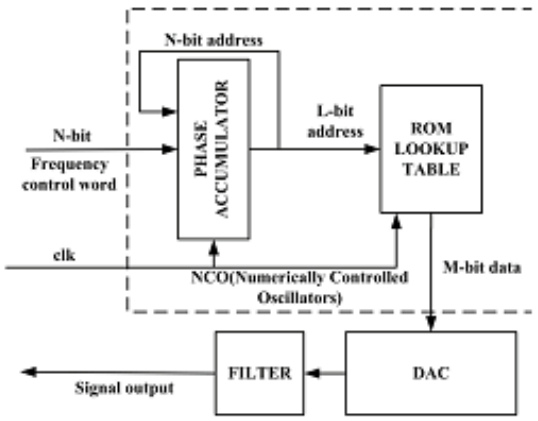

Fig 2. Block diagram of classic DDS.

The NCO contains the phase accumulator and ROM lookup table. It is the core of DDS. In each clock period, the output of phase accumulator is accumulated with frequency control word M (N-bit) and high L-bit results of the output are used as address input to the ROM lookup table. In the ROM lookup table, these addresses are converted to the M-bit sampled data of expected signal. Suppose that the clock frequency is constant, we can absolutely get the formula (1). According to the Shannon Sampling Theorem, upper limit the output frequency is 0.5 f_c However, the biggest output frequency in practice is about 0.25 f_c, and the resolution of output frequency is

$$\frac{1}{2^N} f_c \quad [7].$$

II. DESIGN OF SIGNAL GENERATOR

3.1 Description of System:

The signal generator is designed to output single-frequency or mixing-frequency signal. The mixing-frequency signal is composed of fundamental wave, the 3rd harmonic and the 5th harmonic. The frequency and the phase of the fundamental wave are adjustable, and the proportion of every single frequency harmonic in mixing-frequency signal can also be controlled. It is required that the frequency of the signal generator should be adjustable from 1kHz to 1MHz with the resolution of 10Hz; the phase should be adjustable from 0º to 360º with the resolution of 1º; and the harmonic proportion should be from 0 to 40% with the resolution of 1%. The typical output signals are two channels 100 kHz sine wave and the phase difference is 180º. According to formula (1), if clock frequency is 50MHz, and the phase accumulator is 32 bits, the biggest frequency of output signals is 25MHz and the resolution of frequency is 0.0116Hz. The 12-bit phase control word is used, the initial phase of output signals is also adjustable from 0º to 360º, and the resolution of the phase is about 0.1º. With 8 bits harmonic proportion control word, the harmonic proportion is adjustable from 0 to 127%. It meets the requirements completely. The diagram of the whole system is shown in Figure 3 [8].

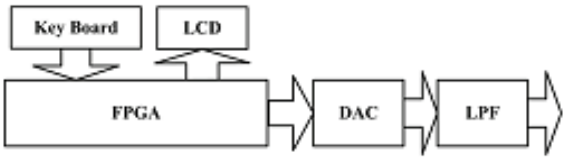

Fig 3. Block diagram of system.

3.2 System Clock:

The system clock is generated by external crystal. It is very important not only for soft core CPU which embeds in FPGA, but also for the DDS core and SDRAM which is used to store the program of the soft core. In order to ensure the stability of the system clock, the phase locked loop (PLL) which exists as one kind of source in FPGA chip is used. And then in the help of Xilinx spartan which is the FPGA develop tool supplied by Xilinx Inc., the PLL module is adopted. With Xilinx spartan, we can set some parameters of PLL module, such as clock multiplication factor, clock division factor and clock phase shift etc. In this design, we need three clocks which come from a base 50MHz external clock and the PLL module. The module is shown in Figure 4. The first clock output from PLL is the clock of soft core CPU, the second is the SDRAM clock, and the third is the DDS core clk after frequency dividing appropriately by clk_fre module.

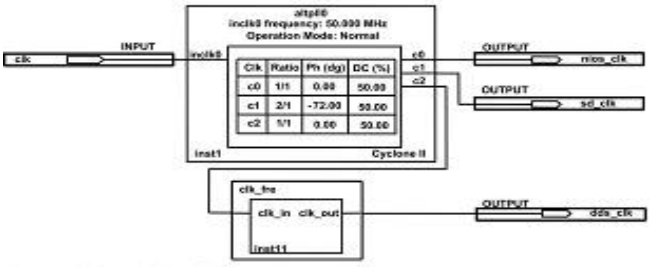

Fig 4. Clock module of the system.

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3.3 Design of DDS Core:

The DDS core has two important parts, the frequency and phase control module and the ROM lookup table. The two parts are compiled with the Very-High-Speed Integrated Circuit Hardware Description Language (VHDL) [9]. 1) Frequency and Phase Control Module the frequency and phase control module is composed of an accumulator and an adder. The frequency of the signal is controlled by accumulator and the initial phase of the signal is controlled by the adder [10]. The initial value of the accumulator is 0. In every clock period, the frequency control word is added at the previous result of the sum in accumulator, and then the result of the accumulator is added with the phase control word in the adder. Finally, the result input to the ROM lookup table.

The initial phase and frequency of the signal can be changed by this module flexibly. The same time, the control precision can be increased by increasing the bit number of the frequency control word and initial phase control word. The module which is created in Xilinx spartan is showed in figure5.

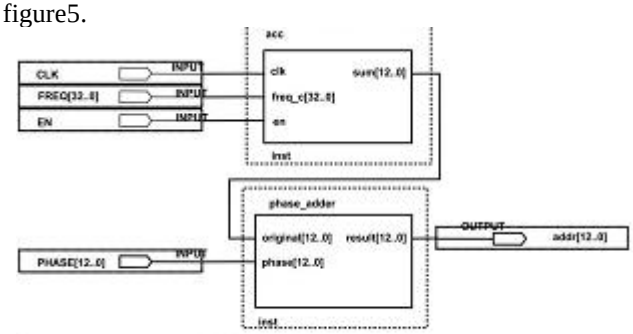


Fig 5. Frequency and initial phase control module.

2) ROM Lookup Table :

ROM lookup table is critical and difficult in the design of the DDS core. It stores the data of sampled sine wave data. The function of the ROM lookup table is mapping from phase to sine amplitude. Meanwhile, ROM lookup table is also the main disadvantage of DDS core. It costs a lot of source to store more points of sine wave of one period and more bits. This disadvantage can be reduced using several compression methods [11]. For a high spectral purity a lot of compression algorithms are developed: the CORDIC algorithm [12], the Nichllas method [13][14], the use of Taylor series and quadratic approximations [15]. The most elementary and well-known technique is to store only 0º~90º sine information, and generate the ROM samples for the full range of 360º by exploiting the quarter-wave symmetry of the sine function. The decrease in lookup table capacity is paid by the additional logic necessary to generate the complements of the accumulator and lookup table output. The principle is showed in Figure 6.

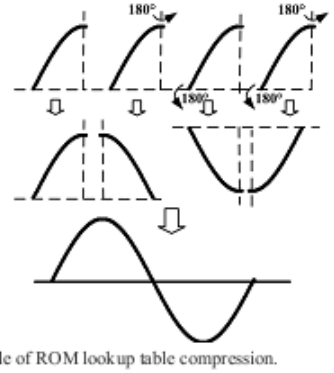


Fig 6. Principle of ROM lookup table compression.

For implementation of the compression algorithm which is explained above, the output address data of the frequency and initial phase module and two complementation modules, which are the phase complementation module and the data complementation module, are used. The sine wave data whose phase is from 0º to 90º of one period is stored in the ROM, and the address of the ROM is mapping to the phase of the sine wave. The high 2 bits of the output address data is the enable signals of the two complementation modules. When the high 2 bits of the output address data is “00”, it indicates that the signal date whose phase is from 0º to 90º should output. The sine wave data outputs directly from the compression ROM without transform. When the high 2 bits of the output address data is “01”, it indicates that signal date whose phase is from 90º to 180º should output. For getting the right waveform data from the ROM, the address data should be transformed using the phase complementation module. When the high 2 bits of the output address data is “10”, it indicates that signal date whose phase is from 180º to 270º should output. For getting the right waveform data, when the wave data output from the ROM, it should transformed using complementation module. Finally, when the high 2 bits of the output address data is “11”, it indicates that the waveform data whose phase is from 270º to 360º should output. So, we not only transform the address data using phase complementation module, but also transform the data output the compression ROM using data complementation module. The reality of the compression algorithm in FPGA reduces the cost of resource of the FPGA and improves the mount of sampled sine wave points. The cost of the ROM is quarter of the ROM without compression algorithm. In the design of the signal generator described in this paper, the 10 211× bits ROM is used to reach the same effect as 10 213× bits ROM without compression algorithm. The module designed in Xilinx Xc3S500e fpga is showed in Figure 7.

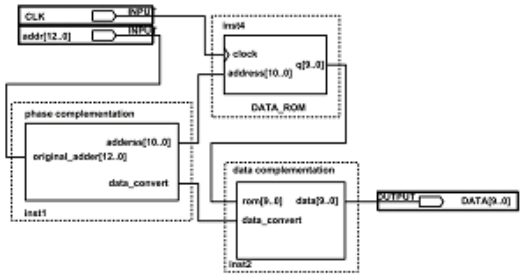
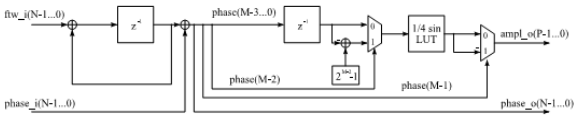


Fig 7. ROM lookup table module.

III. IMPLEMENTATION RESULTS.



Block diagram of the DDS Implementation

Name	Direction	Wordsize	Description
clk_i	in	1	clock
rst_i	in	1	reset
ftw_i	in	ftw_width	Frequency Tuning Word, see Formula (1)
phase_i	in	phase_width	Phase Tuning Word, see Formula (2)
phase_o	out	phase_width	Instantaneous Phase Output
ampl_o	out	ampl_width	Amplitude Output

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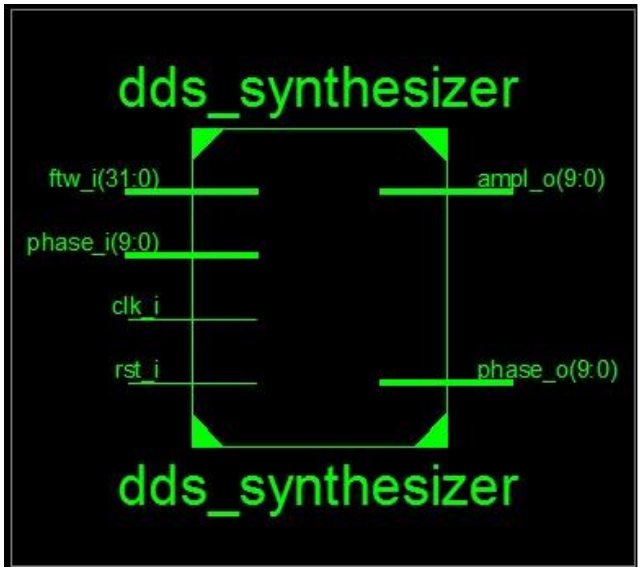

RTL Block

Device		On-Chip	Power (W)	Used	Available	Utilization (%)
Family	Spartan3e	Clocks	0.000	1	---	---
Part	xc3s500e	Logic	0.000	225	9312	2.4
Package	fg320	Signals	0.000	287	---	---
Grade	Commercial	IOs	0.000	64	232	27.6
Process	Typical	Leakage	0.081			
Speed Grade	-4	Total	0.081			

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Grade	Commercial	IOs	0.000	64	232	27.6
Process	Typical	Leakage	0.081			
Speed Grade	-4	Total	0.081			

The total power consumption of the device was found to be 0.081W.

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