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Design and Analysis of a low Power CMOS Sense Amplifier for Memory Application

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Abstract— This paper we design a low power high speed sense amplifier for CMOS SRAM. It has to sense the lowest possible signal swing from the SRAM bit lines and its response time should be very fast while keeping the power consumption within a tolerable limit. in this presented sense amplifier will be based on latest architectures available in literature and we focus will be to improve the power consumption and response time of this sense amplifier. Typical memory that is available has read access time of 12 ns and power consumption of 160 mW and supply voltage ranges from 1.8 to 3.3V and rise time SAEN signal ranges from 100 to 400ps and offset voltages ranges from 45 to 80mv. In this paper we present to improve access time power consumption two parameters of sense amplifier. Presented Sense amplifier CMOS SRAM all schematic are design tanner EDA S-edit , Simulate T-spice and 0.18µm technology.

Index Terms— Sense amplifier,offset in sense amplifier, Advanced current latched sense amplifier,Precharged circuit.

I. INTRODUCTION

On the modern trends quick memories are highly required with low power consumption. The low power and low voltage CMOS techniques were applied extensively in analog and mixed mode circuits for the compatibility with the present IC technologies[14]. Low power consumption can be achieved by using sense amplifiers which are main part of CMOS memory. Parasitic capacitance is much higher if memory is of high densit[15]y. The large capacitance is an issue to make our each cell more energy to charge means low to sense amplifier. To achieve a faster memory and less power dissipation we have to design sense amplifiers as. Increase in number of cells per bit line which will increase the parasitic capacitance. Minimize supply voltage lead to short noise margin that affects the sense amplifier reliability. To maintain small voltage swing over the bit line, increase the area of each cell for design more memory on the chip which decreased the load on bit line. The wide range of applications of sense amplifier as it provides a photovoltaic system which usually stores enough energy for uncertainty in availability of solar radiation due statically nature of biosphere. These typical ICs are the complex component to measure the charge battery and discharge current. sense amplifiers plays a very smart role to maintain the reliability , accuracy and extended battery life by cutting power down over certain region to control heat .Mainly two types of SRAM sense amplifier linear amplifier and latch type amplifier. Linear type amplifier has the main benefit of rejecting the common mode voltage variation, it demands sufficient gate source voltage over drive Vgs - Vth at its input transistor gates for proper operation and Latch Type Amplifiers amplifier is based on a cross- coupled inverter unlike a linear SA, a latch type SA requires an accurate timing for proper operation

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II. LITERATURE REVIEW

Sense amplifier the main circuits used in the memory design. There are mainly two types of sense amplifiers and they can be categorized in current mode and voltage mode sense amplifier. Current mode sense amplifier detects the current difference between the bit lines and voltage mode sense amplifier detects the voltage difference between the bit lines to determine whether a “0” or a “1” is stored in the memory cell .It amplifies the voltage signal and transfers it on the output circuits. Various architectures of sense amplifiers are available in literature. We will discuss following architectures**.**

A. Current Mode PMOS Bias Type Sense Amplifier:

The fundamental reason for applying current-mode sense amplifiers in sense circuits is their small input impedances and, in cross-coupled feedback configuration, their small common input/output impedances. Benefits of small input and input/output impedances, which are coupled to a bit line, include significant reductions in sense circuit delays, voltage swings, cross talking, substrate currents and substrate voltage modulations.[6]

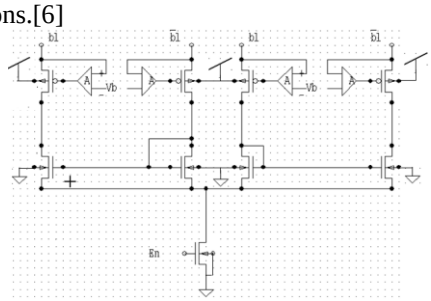

Figure1: PMOS Bias type (PBT6) Sense Amplifier [6]

Current amplification in memories is implemented almost exclusively in feedback circuits. Yet, numerous feedback circuits other than current amplifiers can also provide small input- or small common input-output impedances. Generally, sense amplifier input and output impedances may be optimized for specific memory cell type, load circuit, amplification and other requirements.

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Clearly, the design should use that amplifier type, or that combination of various amplifiers, which provides the highest performance at the least costs when combined with the other parts of the sense circuit. This architecture includes two current mirror cells that copy the current of bit-lines and then subtract them and the outputs are complementary. PMOS transistors are used for the bit line loads .In this architecture the gain element has been used to increase the bit-line loads and to reduce the effect of bias voltage on delay.

Advantages:

- The active-load PBT architecture (PBT6) gives the best performance in terms of delay.
- The active-load PBT is not affected by changes in Vdd and bias voltage, and proves to be fairly robust.

Disadvantages:

- However, the implementation of the differential gain element is critical to minimize the size of the overall sense amplifier, as well as the power consumed by the sense amplifier.

B. Current Mirror Sense Amplifier:

The traditional form of the primitive current amplifier is the current mirror amplifier. In the current-mirror amplifier, if devices M1 and M2 are identical, then the bit line or input current I_i is the same as the read line or output current I_o , because the gate-source voltage V_{gs} is common for both devices M1 and M2. If M1 and M2 differ only in their aspect ratios W/L otherwise they are identical, then the application of MOS current equations yields [5]

$$i_0 = \beta_q \frac{(1+\lambda V_{DS2})}{(1+\lambda V_{DS1})} i; \text{ if } V_{DS1} \neq V_{DS2} \quad (1)$$

$$i_0 = \frac{\left(\frac{W}{L}\right)_{M2}}{\left(\frac{W}{L}\right)_{M1}} I \, , V_{DS1} = V_{DS2} \quad (2)$$

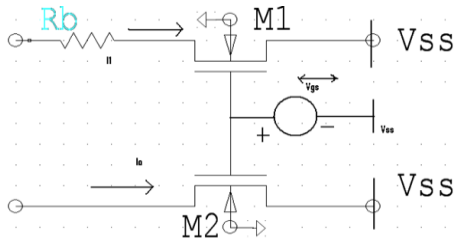

Figure2: Current Mirroring and Multiplication.[5]

where $\beta_q = \beta_2/\beta_1$, β_1 and $\beta 2$ are the respective gain factors of M1 and M2, VDS1 and VDS2 are the respective drain-source voltages for M1 and M2, and λ is the channel-length modulation factor, (W/L) M1 and (W/L) M2 are the respective aspect ratios of M1 and M2, W is the channel width, and L is the channel length. Current mirroring and multiplication by β_q are implemented usually by shorting the drain and gate of device M1, rather than by using an extra bias voltage source V_{GB}. An additional device M3 combines the bit line selection with the current sense circuit. In this circuit, the common gate voltage V_{GS} tends to increase when I_i increases. An increased in V_{GS}, however, reduces the drain-source resistance r_{d1} in M1, and V_{GS} tends to decrease. At little changes in V_{GS}, small variations in current I_i can be detected and amplified. The practical limit of the current amplification Ai is set by the silicon surface area available for the output device M2 which is determined by the column or by the decoder pitch in most of the designs. The conventional current-mirror sense amplifier in figure 4 is easy to control with the sense-amplifier activation timing signal, SE, and the speed of the current-mirror sense amplifier can be easily accelerated by increasing the operating current. Thus, memories frequently use this type of sense amplifier. However, the static current flows through the transistor MNS connected to ground; to accelerate the sense speed needs much power.

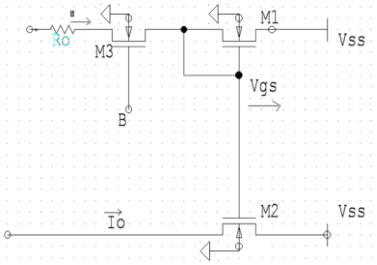

Figure 3: Current sensing combined with bit line selection.[5]

To realize a low power and automatic power-saving scheme, a current-latch sense amplifier is needed. Cascade connection of this sense amplifier allows logic functions to be performed on small-swing differential signals directly, thus reducing delay and power. However, the idea of applying small-swing differential signals for performance and power saving is the cross-coupled sense amplifier.

Advantages:

- It is easy to control with the sense-amplifier activation timing signal, SE.
- Speed of the current-mirror Sense amplifier can he easily accelerated by increasing the operating current.

Disadvantages:

- It needs much power to accelerate the sense speed.
- To realize a low power and automatic power-saving scheme, a current-latch sense amplifier is needed.

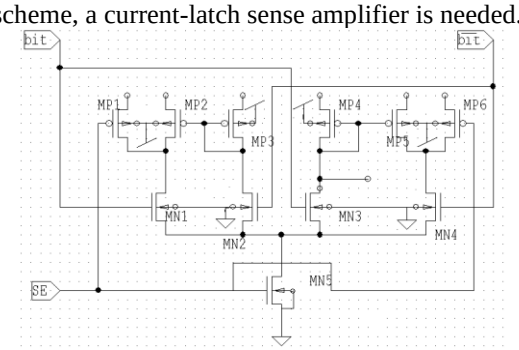

Figure 4: Current Mirror Sense Amplifier [4]

C. Cross Coupled Voltage Mode Sense Amplifier:

Transistors MPI, MP2**,** MNI and MN2 form a cross-coupled complementary structure. The speed and loading characteristics of any cross-coupled sense amplifier depend on the conductivity of the discharging chain and the capacitances of cross-coupled nodes. The higher the conductivity and the lower the capacity can speed an amplifier. Discharge chain of sense amplifier consists of only two n channel transistors MN1 (MN2) and MN3, connected in series and thus satisfies the condition on fast discharging the cross coupled nodes. Moreover, this sense amplifier has two decouple transistors isolate the loading of output nodes because the bit line loading is decoupled from the output nodes and a lot of improvement has been made in the sensing delay.

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However there still exists a current flow, which is caused by the voltage difference between bit lines and output nodes.[4]
Advantages:

- Sensing delay is improved over current mirror Sense Amplifier.
- For having small-swing differential signals for better performance, we use cross-coupled sense amplifier.
- Cross coupled inverter pair provides high gain.

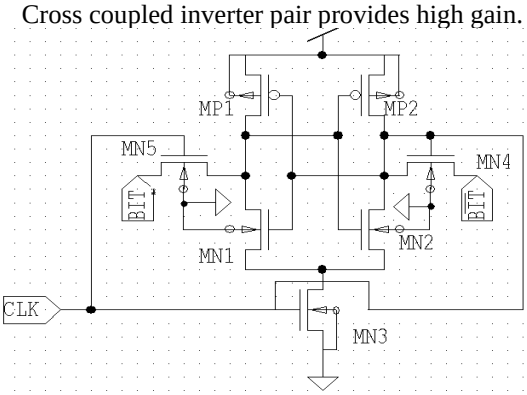

Figure 5 : Cross-coupled Sense Amplifier [4]

Disadvantages:

- Current flow makes additional and unexpected power dissipation when SA senses data signal form bit lines.

D. Modified Latched Sense Amplifier:

The Current Latched Sense Amplifier (CLSA) is shown in Figure 2.6. The bit line signal difference affects on the gate voltage of transistors MN1 and MN2, and the drains of transistors MP1, MN5, MP2 and MN4 are output nodes. There is no current flow from bit lines to output nodes. When sensing signal SE is at logic 0 (GND), the output node is isolated to GND, and the precharge transistors MP3, MP4 charge output nodes to $V_{dd.}$ Because the output nodes O and O are precharged to V_{dd}, the transistors MP1, MP2 are at cut-off region and MN4, MN5 are at saturation region.

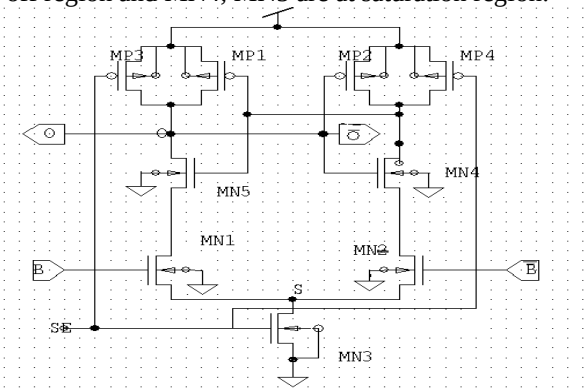

Figure 6: Current Latched Sense Amplifier [4]

When the sensing signal SE changes to logic 1 (V_{dd}), MN3 is turned on and the node S is pulled down to GND level. Under this condition, MN1 and MN2 are working as a common source differential amplifier. The voltage difference between B and B bar is transferred to the output nodes O and O bar by the common source differential amplifier. After a small voltage difference between O and O bar is generated, the cross-coupled amplifier which is constructed by MN4, MN5, MP1 and MP2 will finally amplify the voltage difference between O and O to a full swing voltage level. Therefore, we can sense and amplify the bit line signal without any current drifting from bit line to output node.[4] This result shows that the bit line voltages will not be amplified, so the sensing and precharging power dissipation will be reduced. However, the CLSA has four transistors cascaded from V_{dd} to GND. This is a major disadvantage of CLSA to work at low working voltage (under 1.8v). When CLSA is working at low voltage, the differential current may be too small to be used for fast operation, which would even lead to the erroneous operation. Therefore, a low voltage sense amplifier with better performance is needed.

Advantages:

- Sensing and precharging power dissipation will be reduced.

Disadvantages:

- However, the current latch sense amplifier has four transistors cascaded from V_{dd} to GND. This is a major disadvantage of the current latch sense amplifier to work at low voltage.
- When the current latch sense amplifier is working at low voltage, the differential current may be too small to be used for fast operation, which would even lead to the erroneous operation.

E. Advanced current latched sense amplifier:

A high-speed sense amplifier using the switch circuits (MN5, MN6, MP7 and MP8) to improve the power consumption and operation speed. Figure 2.7 illustrates the circuit architecture. Notably, the input node bit (bit bar) is controlled by the sensing signal and is isolated to the output node out bar (out). Thus the sensing power can be reduced. Also, a better performance at lower working voltage can be obtained by using the switch circuits. Two operation modes, the precharge mode and the sense mode, are analyzed and discussed as follows.[4]

1. Precharge Mode:

In the precharge mode, the sensing signal SE is at logic 0 and the output nodes out bar (out) must be cleared for preparing the next sensing operation. Restated, the transistors MP7 and MP8 of the switch circuit are turned off in this mode. Thus, the input signals from bit lines cannot enter the sense amplifier and the drain voltages of transistors MN5 and MN6 are pulled down to zero. At this condition, transistors MNl, M N2, MN3 and MN4 are turned off and the output nodes out bar *(out)* can be charged to V_{dd} through the precharge transistors MP1 and MP6**.** Notably, the output nodes will hold at Vdd level since transistors MN1 and MN4 are turned off.

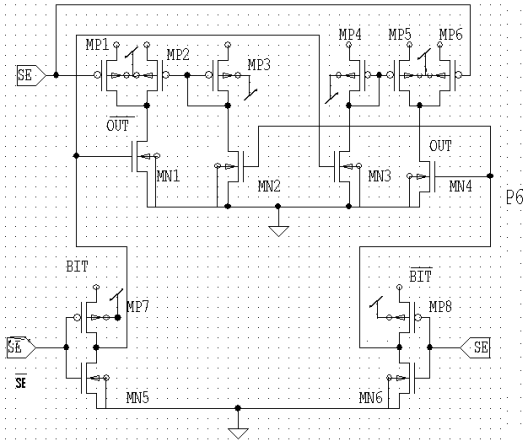

Figure 7: Advanced current latched Sense Amplifier [4]

2 Sense Mode: —

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The sensing signal SE is set at logic 1 in the sense mode operation. In this mode, the transistors MP7 and MP8 of the switch circuit are turned on, meanwhile transistors MN5 and MN6 are turned off. Thus, the input signals bits (bit bar) are transferred to the sense amplifier and transistors MN1, MN4 can work as a common source differential amplifier. Restated, a drain-to-source current difference between transistors MN1 and MN4 are induced. Finally, the current mirror architecture constructed by transistors MP2, MP3, MP4 and MP5 will convert and amplify the current difference to a voltage difference between the output nodes out bar and out.

Advantages:

- The sensing delay of this sense amplifier has greatly improved from 84% to 87.3%. [6]
- This sense amplifier can operate quite well at supply voltages from 1.8 - 3.3 V**.** It is good for wide range of small-swing circuits.
- Thus, applying such circuits in VLSI design can improve the performance and reduce the power consumption.

Disadvantages:

- This design is more complicated than crossed coupled SA and previous current latch sense amplifier.

*F. High Speed Low Power Current Latched Sense Amplifier***:** This SA is shown in Figure 2.8. There are only three transistor stages cascaded from VDD to GND. Note that the transistor stage number is less than that of lower working voltage can be obtained. CLSA, and the input nodes B, B are isolated to output nodes O, O bar. It is expected that the proposed SA has the same power consumption as CLSA; meanwhile a better performance at lower working voltage can be obtained. The circuit operation is described as follows.[13]

In Precharge Mode, the sensing signal SE is at logic 0. In this mode, the data on output nodes must be cleared and the SA prepares for next sensing operation. Because the sensing signals SE=0 and SE bar =1, MP1, MP4, MN5 and MN6 turn on, meanwhile MP5, MP6 turn off. Thus the input signals from bit lines can't enter through MP5 and MP6. Nodes 1 and 2 are pulled down to GND

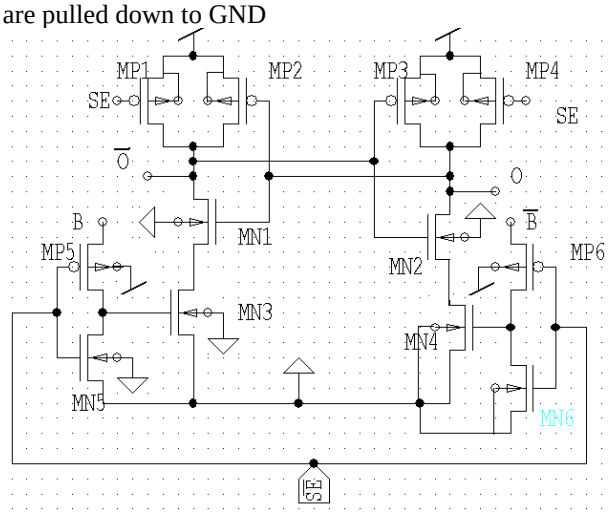

Figure 8: High speed low power Latch Type Sense Amplifier [13]

level by MN5, MN6, so MN3, and MN4 will be cut off. The precharge transistors MP1, MP4 charge the output nodes to V_{dd}. Because MN3, MN4 are turned off, both the output nodes will hold at V_{dd} level. In this time interval, the operation detail is shown in Figure 2.8 (a).

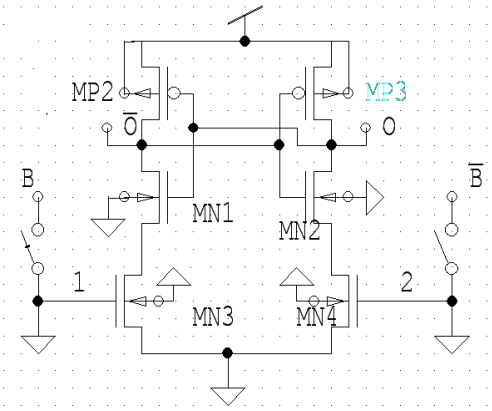

Figure 8 (a): Sense Amplifier in Precharge Mode

In Sense Mode, the sensing signal SE is at logic 1. In this mode, the bit line input signals B, and B bar must be transferred to SA's differential input nodes 1 and 2. Therefore, MN3 and MN4 work as a common source differential amplifier. This operation situation is just like CLSA in sensing operation. As the sensing signals SE=1 and SE bar =0, MP5, MP6 turn on and MN5, MN6, MP1, MP4 turn off. The bit line signals are transferred to nodes 1 and 2 by MP5 and MP6.The voltage difference between nodes 1 and 2 induces a drain-to-source current difference between MN3 and

MN4. Finally, the cross-coupled amplifier constructed by MP2, MP3, MN1 and MN2 will convert and amplify the current difference to a voltage difference between output nodes O, and O bar. For a very short time, the full swing logic value appears on output nodes. This operation detail is shown in Figure 8 (b).

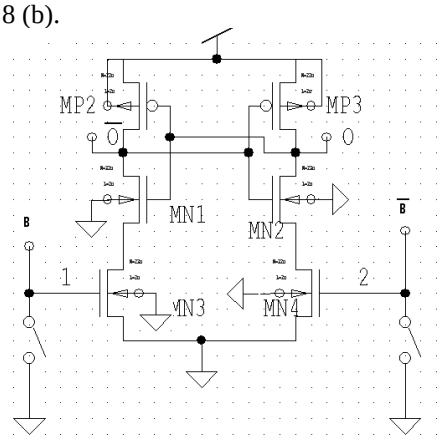

Figure 8 (b): Sense Amplifier in Sense Mode

Advantages:

- This proposed sense amplifier which is implemented in CMOS process can work at voltage as low as 1V.
- As the proposed SA works at 3.3V, this design has 14% and 63% power delay product Improvement over the advanced current latch SA and conventional sense amplifier, respectively.

Disadvantages:

- Due to process variations, current mismatch in the evaluation branches of the sense amplifier circuit, resulting in operational failures.
- Size of this sense amplifier architecture is large.

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III. SENSE AMPLIFIER

Memory Sensing and amplifying the data signal which transmits through memory cell to bit lines are the most important capability for a sense amplifier. However, to sense the data correct and fast becomes more and more difficult when the working voltage scales down to low voltage. In an integrated circuit "sensing" means the detection and determination of the data content of a selected memory cell. The sensing may be "nondestructive," when the data content of the selected memory cell is unchanged (e.g., in SRAMs, ROMs, PROMS, etc.), and "destructive," when the data content of the selected memory cell may be altered (e.g., in DRAMS, etc.) by the sense operation. Sensing is performed in a sense circuit.

The full-complementary positive feedback sense amplifier (Figure 9) improves the performance of the simple positive feedback amplifier by using an active load circuit constructed of devices MP4, MP5 and MP6 in positive feedback configuration. In practice, device pairs MP4-MP5 and MN1 -MN2 can not be completely matched despite carefully symmetrical design. Usually the non-symmetricity between the p-channel MP4 and MP5 is more substantial than that between the n-channel MN1 and MN2, because most of the CMOS processes optimize n-channel device characteristics.

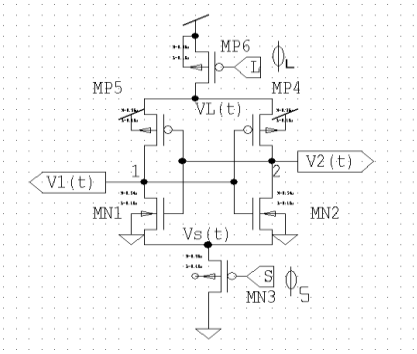

Figure 9: Sense Amplifier

To avoid a large initial offset resulting from the added effects of imbalances in the NAND p-channel device pair, source devices MN3 and MP6 are not turned on simultaneously, but first the n-channel and later the p-channel complex is activated by impulses ΦS and ΦL respectively. The delayed activation of transistor triad MP4-MP5-MP6 by clock ΦL results that until the time MP6 is turned on, device triad MN1-MN2-MN3 operates alone.When the sense signal on the bitline is large enough, e.g., when the drain-source voltage of either MN1 or MN2 reaches the saturation voltage VDSAT, clock ΦL activates triad MP4-MP5-MP6. The activated feedback in MP4-MP5-MP6 introduces a pair of time dependent load resistances r L l (t) = r d4 (t) + 2r d6 (t) and r L2 (t) = r d5 (t) + 2rd6 (t). Here, rd (t) is the time dependent drain-source resistance, and indices 4, 5 and 6 represent devices MP4, MP5 and MP6. The resistances of these devices may be considered as time invariant parameters during the activation of MP6 tSAT , so that rL = r L1= r L2 may be used.In the transient analysis, the differential signal development time td during the presence of impulse ΦS until the appearance of clock ΦL is determined by the switching time of the n-channel triad tdN, and thereafter td is dominated by the transient time of the p-channel triad tdP .With this, the sense-signal development time in the full-complementary positive feedback differential voltage sense amplifier td may be approached as

$$t_d = t_{dN} + t_{dP} \approx t_{dN} \log \frac{V_{DSAT}}{2\Delta V_0} + t_{dp} \ln \frac{0.9(V_{DD} - V_{PR})}{V_{DSAT}} \quad (3)$$

where

$$t_{dN} \approx \frac{C_B + C_{GSN} + 4C_{GDN}}{\beta_N [V_{PR} - V_S(0) - V_{TN}(V_{BC})]} \quad (4)$$

$$t_{dP} \approx \frac{C_B + C_{GSP} + 4C_{GDP}}{\beta_P [V_L(0) - V_{PR} - |V_{TP}(V_{BC})|]}) \quad (5)$$

indices N and P designate n- and p-channel, devices, VDSAT is the saturation voltage, ΔVo is the amplitude of the initial voltage difference generated by the accessed memory cell on nodes 1 and2 , VPR is the precharge voltage, CB is the bitline capacitance, CGS and CGD are the gate source and gate-drain capacitances, and β is the individual gain factor for devices MN1, MN2, MP4 and MP5, vS(0) and vL(0) are the initial potentials on the drains of device MN3 and MP6, VT is the threshold voltage and VBG is the backgate bias.

III. OFFSET IN SENSE AMPLIFIER

The offset in sense amplifier is due to transistor mismatch in the supposedly identical matched transistor pair. This mismatch results from process variations such as random dopant number fluctuations, interface-state density fluctuations etc. The transistor mismatch is expected to get worse with technology scaling due to the demanding requirements on process tolerance. Hence, it becomes extremely important to develop the techniques to minimize the external manifestation of mismatch on circuit performance.The importance of transistor mismatch in the sense amplifier circuit for SRAM application has been very well recognized. This effect is more severe in the positive feedback latch type sense amplifier, which is the preferred configuration for high speed memory. Several techniques have been proposed to minimize the offset in sense amplifier. Most of these techniques increase the sense amplifier circuit complexity, which is not desirable. In this work we systematically investigate the effect of transistor mismatch on latch type sense amplifier and propose a technique to minimize the offset by varying the rise time of SAEN signal and varying the transistors sizing. More complete list of variability sources are listed in Table 1. This is one of the commonly used sense amplifier in high speed memory applications. Without loss of generality we assume that BL_ goes down and BL remains high, when the memory cell is accessed. The offset voltage of the latch is characterized as the minimum input differential voltage between BL_ and BL that is required for

Table I: Variability sources [10]

Process Variation	Variation in Circuit Operation	Simulation Tools Accuracy
Channel Length	Supply Voltage	Timing Analysis
Channel Width	Temperature	RC Extraction
Threshold Voltage	Aging	Cell Modeling
Overlap Capacitance	Cross-Coupling Capacitance	Circuit Simulations
Interconnect	Multiple input Switching	Process Files
etc.	etc.	Transistor Models

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the correct output of the latch. Ideally the two cross coupled NMOS transistors (MN0 and MN1) and the two PMOS pass transistors (R1 and R2) are perfectly matched. For this ideal case, BL_ can be infinitesimally less than VDD for SAO_ to go down. But due to process variations, perfect matching is not possible, and hence, BL_ needs to be less than VDD by a finite amount for correct reading. This finite value is the offset voltage of the sense amplifier. [11] For the latch output nodes precharged to VDD, mismatch in pull-down NMOS (MN0 and MN1) and input PMOS pass transistors (R1 and R2) contributes to the latch offset. In this thesis, offset contribution from MN0 and MN1 is named as the intrinsic latch offset and that of R1 and R2 as the extrinsic latch offset. The total latch offset is sum of these two offsets. The variations in column pass transistors do not influence the latch offset because column pass transistors remain ON during sensing operation. The pull-up PMOS transistors (MP0 and MP1) do not contribute to the latch offset because they are in subthreshold region during sensing period. It appears that the tail transistor MN2 does not influence the offset, as it is a common mode transistor. But as will be shown in the following discussion, the size of the tail transistor has a significant impact on the latch offset. Also, the rise time of sense enable signal (SAEN), has a very profound influence on both the intrinsic and the extrinsic offset.There are two types of offset in sense amplifier, first one is intrinsic offset and second one is extrinsic offset. Difference in drain current of lower two NMOS transistor of CMOS inverters resulting from V_T and β variations causes the intrinsic latch offset. Due to decouple transistors R1 and R2, extrinsic offset occurs. In this thesis, I systematically investigate the effect of transistor mismatch on latch type sense amplifier and use a technique to minimize the offset by varying the rise time of SAEN signal and thus reducing power consumption and sensing delay.[9]

A. Effect of Offset on SRAM Performance:

The access time of the memory in presence of offset depends on two factors:

- First Delay Factor- time required to develop the required differential input at the sense amplifier.
- Second Delay Factor-delay due to sense amplifier itself.

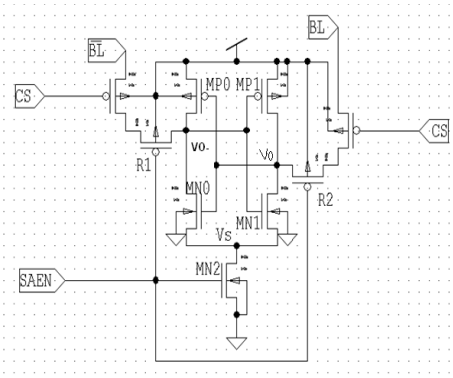

Figure 10: Input decoupled latch type Sense Amplifier [7]

B. Delay affect factors depend on C_{BL} and rise time of SAEN

- The first delay factor is approximately (ΔV_{BL} C_{BL}) / $I_{MEMCELL}$ where ΔV_{BL} is difference in bit lines voltage or offset voltage of sense amplifier. C_{BL} is directly proportional to the number of rows in memory array.
- The second delay factor is independent of C_{BL} but depends upon the rise time of SAEN.

C. Reduction in overall delay and power dissipation by increasing rise time of SAEN signal

- By decreasing the size of MN2 in the sense amplifier and increasing the rise time of SAEN signal, the second factor increases but first factor decreases. For large C_{BL}'s the decrease in first delay factor can overweigh the increase in second delay factor, resulting in lower total delay.
- The power dissipation in bit lines is (ΔV_{BL} .C_{BL} .V_{dd}) which decrease with decrease in ΔV_{BL}. Thus low offset or low ΔV_{BL} results in low power.

IV. DESIGNING SENSE AMPLIFIER AND MEMORY

Sense amplifier mainly three part access transistor, driver transistor and load transistor Figure 11 shows the schematic of basic cell structure sense amplifier it consists of six transistors where MN5 and MN6 is called the access transistor and MN3 and MN4 is called the driver transistor and MP3 and MP4 called the load transistor. It is just like two inverter connecting back to back or cross supled. V_{dd} supply is 3.3 volt word line is applied to the gates of both the access transistors. Substrate of P channel transistor is connetcted to the V_{dd} supply and substrate of N channel is connected to the ground terminal.To understand the working of basic cell we have to assume the previous state of cell. Suppose cell has already store the high data that will result out the node Na has high status and node N_b has the low status, that results out the transistor MP4 & MN3 gets on and MP3 & MN4 gets off. When the data comes to the bit lines of the cell, Suppose zero is being placed on the bit line and one is placed on the bit complement line. As soon as the word line goes to high then node Na will discharge through the bit lines and will goes to low status which forces the transistor MN4 to become off and when node N_b goes high it will force MN3 Transistor to gets on. In this way the cell will flip the state from MN3 and MP4 off to MN4 and MP3 gets on. In this way the write operation get performed and after the write operation word lines goes to low status when the word line goes to low the pass transistor gets off and data which is get stored in the cell remains as such as long as the power supply is apply.

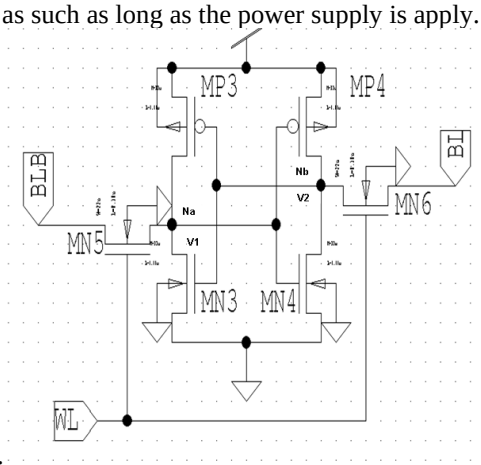

Figure 11: Basic cell when "0" is stored (V_2 = 0 v and V_1 =V_{dd})

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A.To Calculate the W/L ratio:

After making a schematic we have to set the W/L ratio of the driver, access and load transistor which we have used in the basic cell design in any CMOS circuit design W/L ratio is important parameter because this is the only parameter in the hand of the design engineer. So it should be care fully selected in the design of memory cell. There are number of design criteria must be taken into consideration. The two basic criteria which we have taken is given below

1. The data read operation should not be destructive.
2. Static noise margin should be in the acceptable range.

We take the static noise margin (SNM) consideration to calculate the W/L ratio. SNM is defined as maximum value of noise that can be tolerated by cross coupled inverters before altering the state SNM is very important parameter to design any of the memory cell because it indicate the stability of the cell .

B. Calculation of W/L ratio of driver and access transistor:

Consider the data read operation first assume that the logic "0" is stored in the cell. The voltage levels in the CMOS SRAM cell the beginning of the read operation is shown in the figure 11. Here the transistor MP3 and MN4 are off while MP4 and MN3 are on .Thus the internal node voltages are $V_2 = 0$ v and $V_1 = V_{dd}$ before the cell access (pass) transistors are turned on After the pass transistor gets turn on by the word selection circuitry the voltage level of the bit complement will not shows any significant variation since no current will flow through MN6. On the other half of the cell MN4 and MN5 will conduct the non zero current and voltage level of the bit complement will begin to drop slightly. because the column capacitance is large so that is why decrease in the column voltage in the bit lines is very small during the read phase in this process voltage V_1 will increase slightly from its initial value "0" so if the W/L ratio of the access transistor MN5 is large as compared to the driver transistor MN3 than the voltage V_1 may exceed the threshold voltage of the MN4 which will force an unintended change of the stored value. So this is the key design issue, that during data read operation voltage V_1 should not be exceed the threshold voltage of the MN3 so that transistor MN3 remains turned off during the read phase so by keeping these thing in mind we calculate the W/L ratio of the transistors which is given below. When the data come than word lines goes high then access transistor will work in saturation region and driver will work in linear region. So to calculate the W/L ratio of driver and access transistor we have to compare the drain currents of both (driver and access) transistor. In the following equation,3 represents MN5 and 2 representsMN3.The corresponding equation is given below.

Drain current of the access transistor

$$I_{d3} = \beta_3[(V_{dd} - V_{tn})^2]/2 \qquad (6)$$

Drain current of driver transistor

$$I_{d2} = \beta_2[2(V_{dd} - V_{tn})V_1 - V_1^2]/2 \qquad (7)$$

As from the circuit $V_1 = V_{tn}$

By putting this value in the above value in equation a and b We get the given equation

$$(W/L)_3/(W/L)_2 = [2(V_{dd} - 1.5V_{tn})V_{tn}]/(V_{dd} - V_{tn})^2 \qquad (8)$$

Put the following value in equation (8)

$V_{dd} = 3.3$ V

$V_{tn} = 0.6$ V

We get the following value

$(W/L)_3/(W/L)_2 = 3.24 / 4.41$

$(W/L)_3/(W/L)_2 = 0.7$

$(W/L)_3 = 0.7 * (W/L)_2$

Generally from the literature survey we find that the W/L ratio of the driver transistor is generally taken as 3 so W/L ratio of the access transistor is given as

$(W/L)_3 = 0.7 * 3 = 2.1 \qquad (9)$

Approximately W/L ratio of the access transistor is = 2

D. Calculat ion of W/L ratio of load transistor:

First method is as usual we have to compare drain current of both the transistor. For this consider the Write "1" operation , assuming that logic zero is initially stored in the cell.The voltage level of the CMOS SRAM cell at the beginning of the data write operation is shown in the figure 3.6.From figure 3.6 ,it is clear that transistor MP4 and MN3 will turn on and MP3 and MN4 gets off so it shows that MN5 is operating in the linear region and the MP3 is operated in the saturation region so to calculate the W/L ratio of both the transistor we have to compare the drain current of both the transistor the corresponding mathematical calculation is given below. Here 3 represents MN5 and 2 represents MP3.

Drain current of the access transistor

$$I_{d3} = \beta_3[2(V_{dd} - V_{tn})V_{tn} - V_{tn}^2]/2$$

Drain current of the load transistor

$$I_{dp2} = ß_{p2}(0 - V_{dd} - V_{tp})^2/2 \qquad (10)$$

Now compare the above two equations

$$ß_{p2}(0 - V_{dd} - V_{tp})^2/2 = ß_3[2 (V_{dd} - V_{tn})V_{tn} - V_{tn}^2]/2$$

$$ß_{p2}/ ß_3 = [2(V_{dd} - 1.5 V_{tn}) V_{tn}]/ (V_{dd} + 2V_{tp})^2$$

$$(W/L)p_3/(W/L)n_5 = [u_n(2(V_{dd} - 1.5 V_{tn}) V_{tn})]/ [u_p (V_{dd} + 2V_{tp})^2]$$

We have to put the parameter in the above equation which is given below

$V_{dd} = 3.3$ V

$V_{tn} = 0.6$ V

$V_{tp} = 0.56$ V

Mobility of electron as per the model file $u_n = 446$

Mobility of electron as per the model file $u_p = 155$

By putting the above parameter in the equation we get the following value

$(W/L)p_3/(W/L)n_5 = 1.05$

As we know that $(W/L)n_5$ is 2 so

$(W/L)p_3 = 1.05 * 2 = 2.1$

Approximately $(W/L)p_3 = 2$

From then above method it is clear the W/L ratio of the load transistor should be 2 So from above calculation we get the parameter of the basic memory cell as

W/L ratio of the load transistor = 2

W/L ratio of the access transistor = 2

W/L ratio of the driver transistor = 3

C. Schematic of Precharge Circuit:

In a read operation, the bitlines start precharged to some reference voltage usually half of the positive supply. When word line turns high, the access transistor connected to the cell node storing a 0 starts discharging the bitline, while the complementary bitline remains in its precharged state, thus resulting in a differential voltage being developed across the bitline pair. SRAM cells are optimized to minimize the cell area, and hence their cell currents are very small, resulting in a slow bitline discharge rate. To speed up the RAM access, sense amplifiers are used to amplify the small bitline signal and eventually drive it to the external world.

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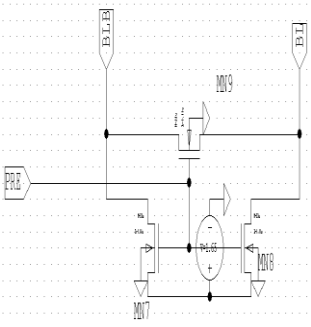

Figure 12: Precharge Circuit

Where MN7 and MN8 are the load transistor and MN9 is used to equalize the voltage equally to the bit lines when the equalizing voltage is applied to the MN9 transistor then it precharge the bit lines to half of V_{dd}.

V. SIMULATION RESULT

The figure13 shows the output voltage of Sense Amplifier. It is to read 1 from memory cell. Output voltage shows the logical 1 i.e. V_{dd} .Access time of memory is shown in figure below by an arrow. It is 3 ns. Precharge signal and sense amplifier enable signal also shown in figure The figure 14 shows the bit line voltage of memory cell. It is to read 1 from memory cell. Difference in bit line voltage is amplified by sense amplifier and gives out when sense amplifier enable signal is enabled. Differential voltage developed between the bit lines is called also offset voltage. The figure 15 shows the variation in bit line voltage. Bit lines first precharged to 1.65 V during PRE signal and when the memory cell is read, these voltage changes The output of sense amplifier is complementary. One is O4 and another is O4B. These output voltages is shown in figure 16 below. Figure shows that the cell is storing 1. The figure 17 shows power consumption during reading operation of the cell. The 18 shows a read cycle when cell is storing 1.This shows the output voltage and bitline variation during read operation. It also shows the column select CS4 and precharge signal PRE..

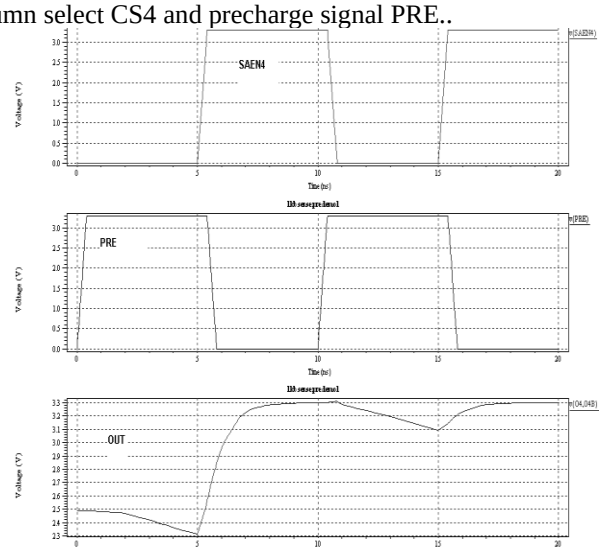

Figure 13: Output Voltage of Sense Amplifier

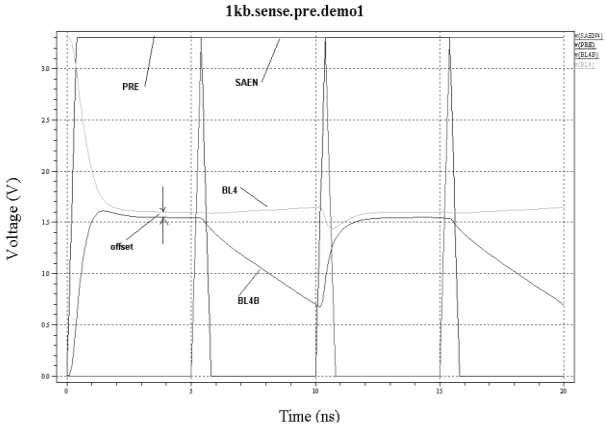

Figure 14: Bit Lines Voltage of Memory Cell

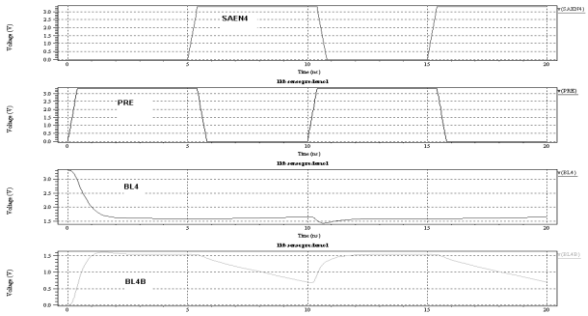

Figure 15: Bit Lines Voltage of Memory Cell

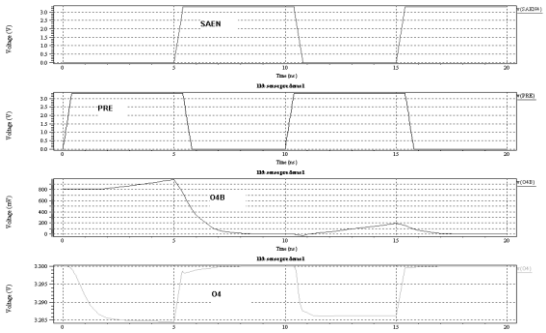

Figure 16: Output Voltage O4 and O4B of Sense Amplifier

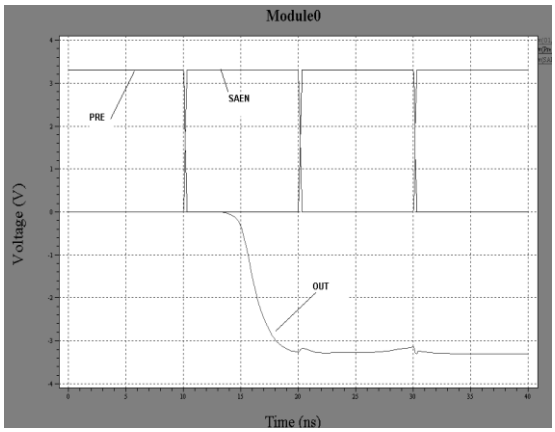

Figure 17: Output Voltage of Sense Amplifier

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Some important results that are observed from simulation of the schematic designed in S-Edit are summarized below

Table II: Variation in Power Consumption and Delay

Size of transisto MN2 W(µm)	delay factor (ns	Offset volta (mV)	Power consumpti (mW)
0.54	3.3	82.53	15.45
0.36	3.8	75.66	14.56
0.18	4.4	61.90	13.32

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