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Performance Analysis of Multi Level Inverter with DC Link Switches for Renewable Energy Resources

Karthika N, Sangari A, Umamaheswari R

***Abstract*— The main objective for a grid-tied Photo Voltaic (PV) inverter is to feed the harvested energy from PV panel to the grid with high efficiency and high power quality. This paper reveals a novel modulation scheme called single carrier Phase Opposition Disposition (POD) Pulse Width Modulation (PWM) technique for H Bridge Multi Level Inverter topology for the solar plants that can account for voltage profile fluctuations among the panels during the day and the performance is studied by comparing total harmonic distortion and switching losses at different switching frequencies. The operating principle and performance of the proposed inverter is verified through simulation studies**.

***Index Terms*— PV system, Pulse Width Modulation, THD, Simulation.**

I. INTRODUCTION

Grid connected inverter systems are gaining importance due to the increase in demand on renewable energy sources. Generally two-level PWM inverter is used for grid-tied operation. In case of a two-level inverter, the switching frequency should be high or the inductance of the output filter need to be big enough to satisfy the required THD. To cope with the problems associated with the two-level inverter, Multi Level Inverters (MLIs) are introduced for grid connected inverter as shown in fig 1. The major advantage of cascaded Multi Level Inverter is the switching frequency and device voltage rating can be much lower than those of a traditional two level inverter for the same output voltage level. Since there is a significant reduction in MOSFET switching loss, the inverter system efficiency can also be increased.

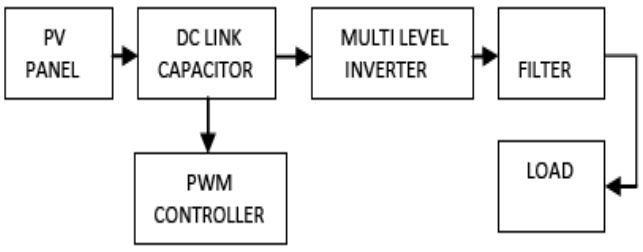

Fig 1. Block Diagram of proposed Multi Level Inverter

II. PV CELL MODEL

A photovoltaic system converts sunlight into electricity. The basic device of a photovoltaic system is the photo voltaic cell. Several cells are grouped in series and/or parallel to form panels or modules. In practical, photovoltaic device presents a hybrid behavior, which may be of current or voltage source depending on the operating point. The device has a series resistance R_s whose influence is stronger when the device operates in the voltage source region, and a parallel resistance R_{sh} is with stronger influence in the current source region of operation. These resistances are the sum of several structural resistances of the device.

A. Mathematical Model of PV Panel

$$I = I_{PV} - I_O \left[\exp\left(\frac{V + R_S I}{V_t a}\right) - 1\right] - \frac{V + R_S I}{R_P}$$

$$\text{Where,} \quad I_o = \frac{I_{sc,n} + K_I \Delta_T}{\exp\left(\frac{V_{oc,n} + K_V \Delta_T}{a V_t}\right) - 1}$$

B. Simple Circuit Model of a Typical Solar Cell

An ideal solar cell is modeled by a current source in parallel with a diode. However no solar cell is ideal and thereby shunt and series resistances are added to the model

- I - Cell output current
- V - Cell output voltage
- I_{PV} - Photovoltaic current
- I_O - Saturation current
- V_T - Thermal voltage
- T - Cell temperature in ^{o}c
- K - Boltzmann's constant
- q - Electronic charge
- k_I - Current coefficient
- k_V - Voltage coefficient
- R_S - Series Resistance
- R_P - Parallel Resistance
- I_{SC} - Short-circuit current at 25^o C and 1000 W/m^2
- T_r - Reference temperature
- I_{or} - Cell saturation current at T_r

as shown in the PV cell diagram in fig 2. R_s is the intrinsic series resistance whose value is very small. R_{sh} is the equivalent shunt resistance which has a very high value.

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PG Student. Karthika N, Power Electronics And Drives, EEE Department, Anna University, Rajalakshmi Engineering College, Chennai, Tamil Nadu, India.

Asst. Prof. **Sangari A**, EEE Department, Anna University, Rajalakshmi Engineering College, Chennai, Tamil Nadu,India.

Prof. Dr. R. Umamaheswari, EEE Department, Anna University, Rajalakshmi Engineering College, Chennai, Tamil Nadu, India.

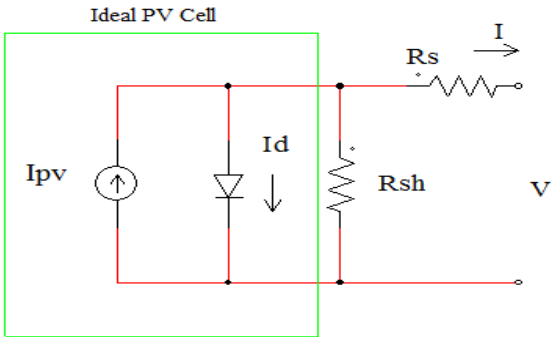

Fig 2. Circuit Diagram of Solar Cell

Fig 3 shows the model of PV Panel where the subsystem consists of PV panel equations referred in [1].

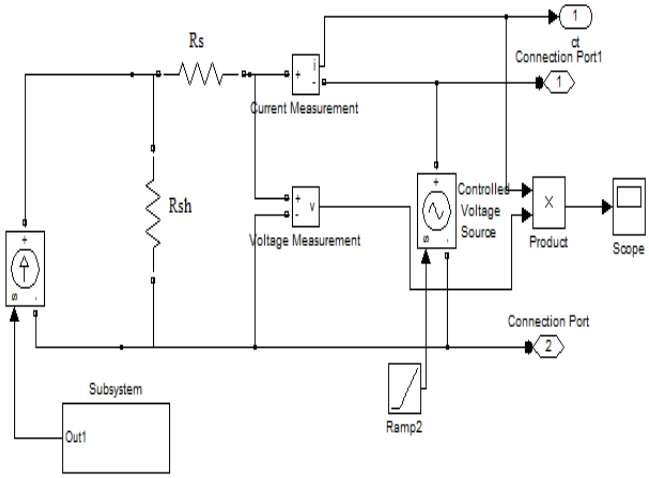

Fig 3. PV Panel Simulation Model

For different values of Irradiance and temperature the PV cell current corresponding to the cell output voltage is obtained by simulation of the model and V-I and P-V characteristics are obtained as shown in fig 4 at varying Irradiance and 5 as varying temperature for the particular PV cell.

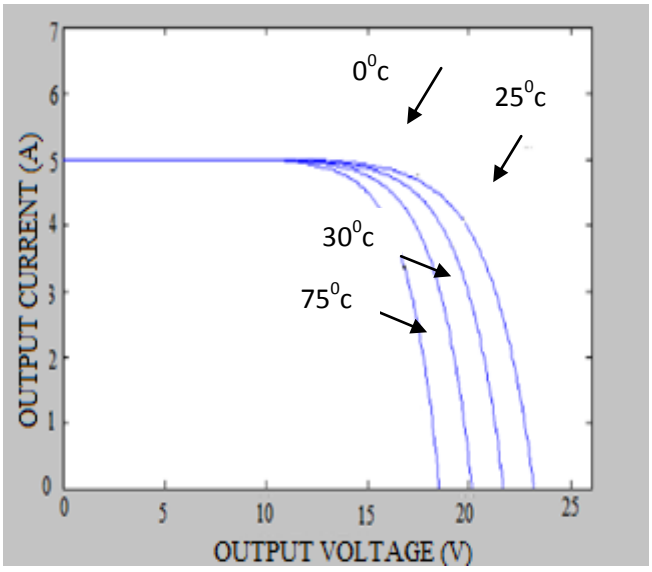

Fig 4. V- I Characteristic of a Solar Panel For a Fixed Irradiance and Varying Temperature

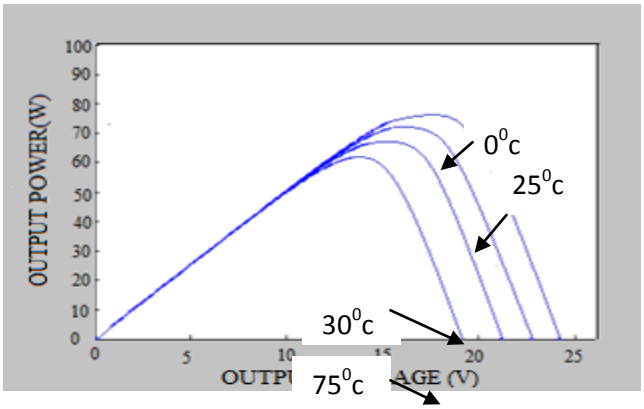

Fig 5. Typical P-V Characteristic of A Solar Panel For a Fixed Irradiance and Varying Temperature

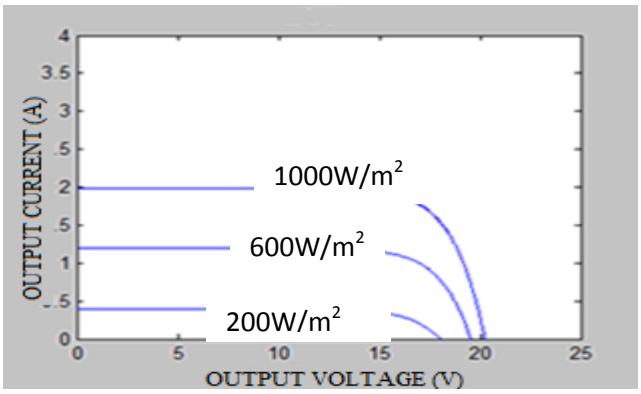

Fig 6. V- I Characteristic of a Solar Panel For Varying Irradiance and Fixed Temperature

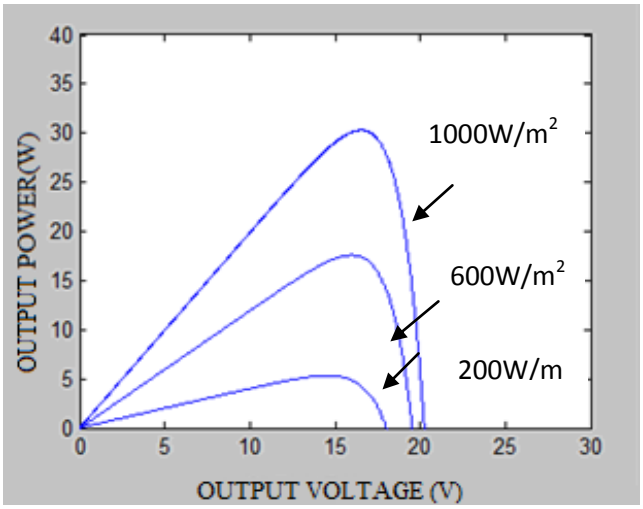

Fig 7. P-V Characteristic of A Solar Panel For Varying Irradiance and Fixed Temperature

Thus from the characteristics of solar cell it is understood that in a day the output power is varying in proportional to irradiance and inversely proportional to temperature. So it is important to track the maximum power output by setting varying over wide output voltage range.

III. MPPT AND GRID TIED INVERTER

In solar generation system, many PV cells should be connected in parallel and series to obtain the require load current and Voltage. Since Solar panels have a nonlinear voltage-current characteristic, with a distinct Maximum

Power Point (MPP), which depends on the environmental factors i.e., temperature and irradiation and in order to continuously harvest maximum power from the solar panels. They have to operate at their MPP despite the inevitable changes in the environment, a power electronic controller is employed with some method for Maximum Power Point Tracking (MPPT). Basically MPPT controller is DC to DC converter which converts the variable DC Voltage into a fixed DC to exactly match load requirements.

MPPT is most effective under following conditions:

• Cold weather, cloudy or hazy days: Normally, PV module works better at cold temperatures and MPPT is utilized to extract maximum power available from them.

• During peak load: MPPT can extract more current and deliver the peak load current requirements.

Over the past decades many MPPT techniques have been studied. The three most suitable algorithms for large and medium size photovoltaic (PV) applications are, Hill climbing algorithms (perturb and observe), Incremental conductance and Fuzzy logic control.

The voltage generated at the terminals of a photovoltaic panel can feed directly DC loads through MPPT converter. But for AC loads and grid tie renewable energy resources along with the tracking of Maximum Power Point (MPP) of the modules, Inverters are employed to convert direct current produced by solar panels, into the alternating current at required voltage level and frequency requirements of the load, typically in standalone applications where utility power is not available. In case of grid connected Solar or commonly, renewable energy resources dedicated grid tie inverter is used to control the power flow and as well as grid integration. A solar grid tie inverter is a special type of synchronous inverter that feeds to an existing electrical grid.

A. Problems in Grid Tied Solar System

The major problems in Grid Tied Solar System are frequent tripping due to harmonic distortion. Maximum total harmonic distortion is mainly due to the exceeded maximum voltage levels. These increased voltages are due to the increased voltage distortion and double zero crossings in the voltage waveforms [3].

It was also found that the topology of an inverter has a large influence on the anticipated distortion in the network. In the conventional inverters the use of PWM modulation provide less distorted current and voltage but at the cost of higher switching losses due to high switching frequencies. So it becomes vital to design and develop a new inverter technique with improved power quality and reduced losses modified. The new Inverter will play an important role in distributed generation with renewable energy resources in terms of power availability and Quality.

IV. PROPOSED MULTI LEVEL INVERTER

The Multi Level technique synthesizes the AC output terminal voltage with low harmonic distortion, thus reducing filter requirements. In particular, Multi Level Inverters are emerging as a visible alternative for high power, medium voltage applications. One of the significant advantages of Multi Level configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output as in [4].

The output voltage waveform of a Multi Level Inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources starting from three levels. As the number of levels reach infinity, the output is a pure sinusoidal. The number of achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints. Three capacitor voltage synthesis based Multi Level Inverters are

1) Diode-Clamped Multilevel Inverter
2) Flying-Capacitor Multilevel Inverter
3) Cascaded-Inverters with Separated DC Source

In all these configurations of Multi Level Inverter, the important issue about is the voltage balance of the DC link capacitor. The voltage of capacitor C_1, C_2 should be equally balanced to V/2 which is very much suitable for solar system. However the midpoint voltage fluctuates when C_1,, C_2 charge and discharge continuously. If the capacitor voltage is unbalanced, the output voltage becomes unsymmetrical and it results in a high harmonic content in the load current.

From simulation studies, here an optimized switching frequency has been obtained for a lower level of total harmonic distortion and switching losses. Flying-Capacitor type, single phase topology Multilevel Inverter is considered for initial studies.

A. Multi Level Inverter

The Multi Level Inverter is shown in fig 8 which is composed of two DC link capacitors (C_1,C_2) and four switching devices (TA+, TA-, TB+, TB-) comprising a H-bridge, and four DC link switches (TP+, TP-, TN+, TN-) located between DC link and H-bridge. The voltage across the switching devices in the DC link is $V_{DC}/2$ and operated at a switching frequency of 1 kHz and 3 kHz. The voltage across the switching devices in the H-bridge is V_{DC} and operated at a frequency of the fundamental component of output voltage.

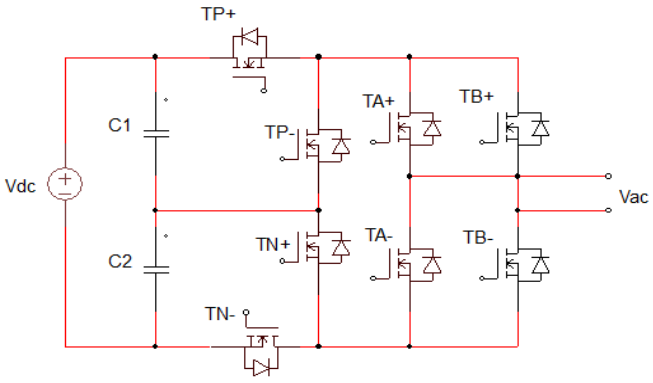

Fig 8. Circuit Diagram of Multi Level Inverter

B. Filter

The filter consists of L-C circuit where inductor L is connected in series with the load and capacitor across the load. It is inserted between the output of the inverter and the load. It is used to remove harmonics where inductor L blocks the dominant harmonics and capacitor C provides an easy path to the n^{th} harmonic ripple current. In practice it has been found that, capacitor provides effective filtering if load consists of R and L in series.

C. Load

Multi Level Inverters can be connected to higher level Loads like Grid, Motors etc. In this paper Multi Level Inverters are connected to R Load for simulation purpose,

where R load gives unity power factor.

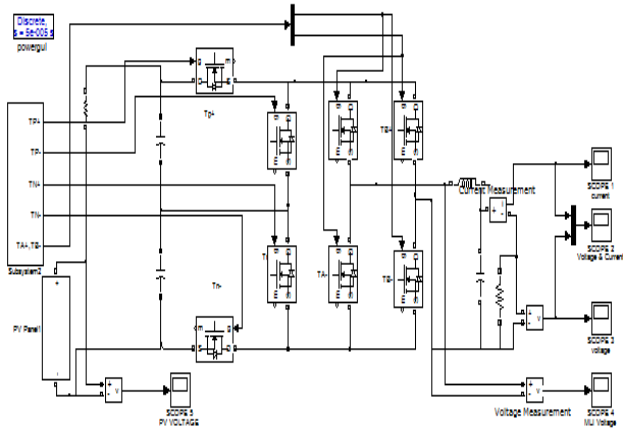

Fig 9. Simulation Circuit of Multi Level Inverter

V. PWM CONTROLLER

PWM Controller is used to produce PWM pulses to operate the switches and also to reduce the Total Harmonic Distortion of the current [2]. Conventionally for a five level inverter four carriers are required to achieve symmetrical Multi Level Inverter. Three dispositions of the carrier signal considered to generate the PWM signals are Phase Disposition (PD), Alternative Phase Opposition Disposition (APOD), and Phase Opposition Disposition (POD). A new PWM strategy based on modulation which requires only a single carrier at 3 kHz and two reference signals is proposed which is used to generate eight PWM signals in PWM method as shown in fig 10. If V_{ref1} exceeds the peak amplitude of the carrier signal $V_{carrier}$, V_{ref2} is compared with the carrier signal until it reaches zero. At this point onward,

V_{ref1} takes over the comparison process until it exceeds $V_{carrier}$.

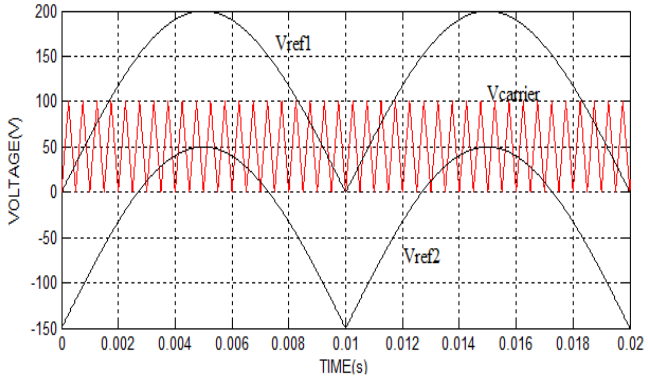

Fig 10. Single Carrier POD Technique

A. *Modes of Operation*

Mode 1: A signal is subtracted from the reference signal by Vc and is compared with the carrier signal. If V_{ref}– V_c>$V_{carrier}$, then all switches TP+ and TN- are turned on. If V_{ref} –V_c<$V_{carrier}$, then the switch TP+ or TN- is turned off alternately.

Mode 2: The reference signal is directly compared with a carrier signal. If V_{ref}>$V_{carrier}$, then the switch TP+ or TN- is turned on alternately. If V_{ref}<$V_{carrier}$, then all switches TP+ and TN- are turned off.

Mode 3: -V_{ref} is directly compared with a carrier signal. If -V_{ref}>$V_{carrier}$ then the switch TP+ or TN- is turned on alternately. If -V_{ref}<$V_{carrier}$, then all switches TP+ and TN- are turned off.

Mode 4: a signal subtracted from -V_{ref} by V_c is compared with the carrier signal. If -V_{ref} –V_c>$V_{carrier}$, then all switches TP+ and TN- are turned on. If -V_{ref} -Vc<$V_{carrier}$, then the switches TP+ and TN- are turned off alternately.

B. *Switching Sequence*

The switching states of various switches are given in table 1.

Table.1 Switching State

Output Voltage Level	Switching Conditions					
	TP+	TP-	TN+	TN-	TA+ TB-	TA- TB+
V_{DC}	ON	OFF	OFF	ON	ON	OFF
$\frac{V_{DC}}{2}$	OFF	ON	OFF	ON	ON	OFF
	ON	OFF	ON	OFF	ON	OFF
0	OFF	ON	ON	OFF	ON	OFF
	OFF	ON	ON	OFF	OFF	ON
$-\frac{V_{DC}}{2}$	OFF	ON	OFF	ON	OFF	ON
	ON	OFF	ON	OFF	OFF	ON
$-V_{DC}$	ON	OFF	OFF	ON	OFF	ON

VI. SIMULATION RESULTS

A. *Five level output voltage*

The output voltage wave of the proposed five level inverter for five cycles with a switching frequency of 3 kHz is shown in fig 11.

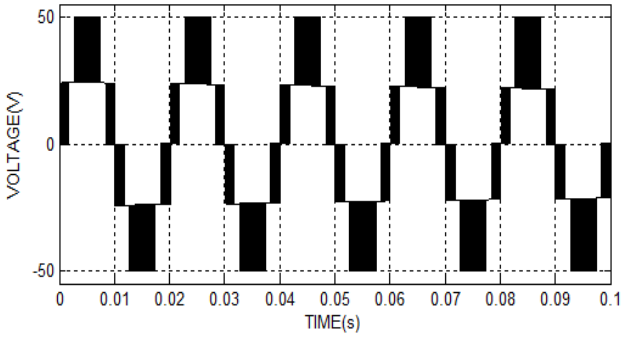

Fig 11. Five Level output of Multi Level Inverter

B. *Output Voltage*

The load voltage of a five level inverter at a switching frequency of 3 kHz is shown in fig 12.

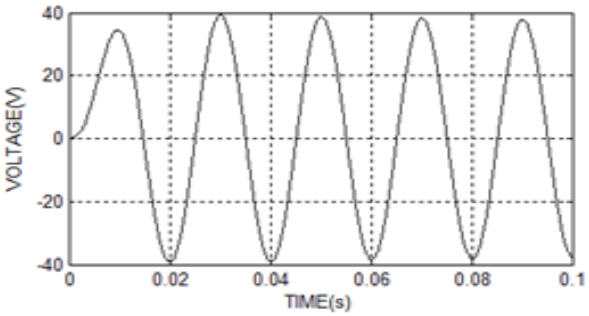

Fig 12. Simulation Output of Load Voltage

C. Load Current

The load current of a five level inverter with R Load at a switching frequency of 3 kHz is shown in fig 13.

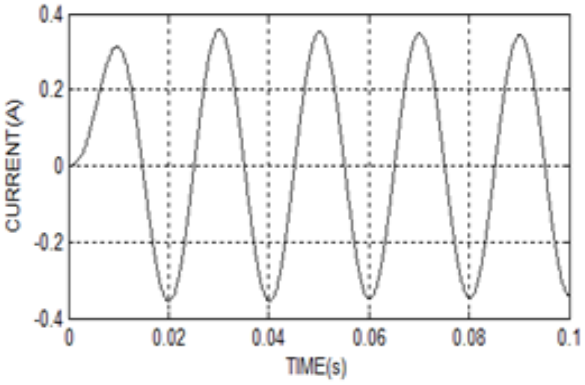

Fig 13. Simulation Output of Load Current

VII. TOTAL HARMONIC DISTORTION

The most widely used measure to indicate the quantity of harmonics contents is the Total Harmonics Distortion (THD), which is defined in terms of the amplitudes of the harmonics, H_n, at frequency $n\omega_0$, where ω_0 is the frequency of fundamental component whose amplitude of H_1 and n is the integer. The THD is mathematically given by

$$THD = \frac{\sqrt{\sum_{n=2}^{\pi} H_{(n)}{}^2}}{H_1}$$

The THD is mathematically given by the system performance of five level inverter and is further improved in terms of the THD for switching frequency of 3kHz.

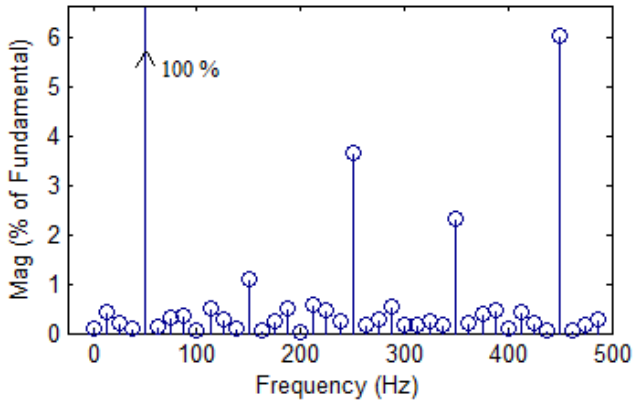

Fig 14. FFT Analysis of Multi Level Inverter

Fig 14 Shows the Fast Fourier Analysis for the output voltage which predicts the Total Harmonic Distortion as 14.17% for the fundamental frequency spectrum considering upto 10th harmonic.

VIII. SWITCHING LOSS

Multi Level Inverter have found better counterparts to the conventional two-level pulse width modulated inverters to overcome switching losses, requirement of switches with low turn-on and turn-off times. In addition they offer the advantage of less switching stress on each device for high voltage, high power applications with reduced harmonic content at low switching frequency. Here in this paper, switching loss are directly calculated from the performance analysis of simple MOSFET model simulated in PSIM software.

A. Switching Loss Calculation

A single MOSFET switch is connected across a DC voltage of value V_{DC}. Current through switch during 'on' time is considered as I_{DC} .

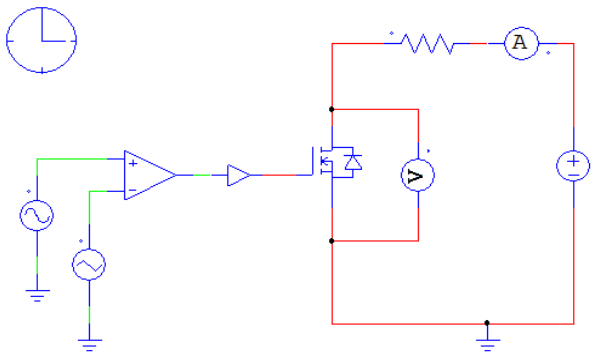

Fig 15. PSIM Simulation Circuit for Switching Loss Calculation of MOSFET

Fig 16 shows the waveforms of the voltage across and the current through the switch when it is operated at a switching frequency of $F_s = 1/T_s$, where T_s is the switching period.

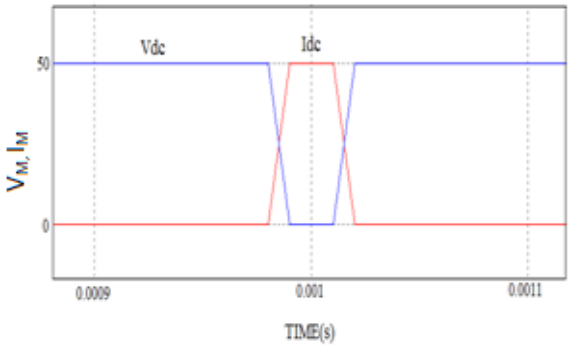

Fig 16.Transient Response of MOSFET Switches

Switching Losses can be calculated from the turn-on and turn-off characteristics of the devices. The average switching loss P_{SW} in the switch is given by equation as in [10] .

$$P_{SW} = \left[\left(\frac{1}{6}\right) \times V_{DC} \times I_{DC} \times \frac{\left(t_{c(on)} + t_{c(off)}\right)}{T_s}\right] + \left[\left(\frac{1}{3}\right) \times V_{DC} \times I_{DC} \times \frac{\left(t_{c(on)} + t_{c(off)}\right)}{T_s}\right]$$

Where

V_{DC} - Voltage across switch when turned off

I_{DC} - Voltage across switch when turned on

$t_{c(on)}$ - Turn-on cross over terminal

$t_{c(off)}$ - Turn-off cross over terminal

T_s - Sampling time in seconds

The switching loss for the MOSFET switch is calculated from turn-on and turn-off characteristics of the devices. The Total Switching Loss can be given as in [10].

Total Switching Loss = (No of switching devices × P_{SW} of switching devices) + (No of active devices × P_{SW} of active devices)

Table.2 Performance of Multi Level Inverter

Switching Frequency	Total Harmonic Distortion (%)	Total Switching Loss (mJ)
1kHz	31.16	0.0171
3kHz	14.17	0.0170

IX. CONCLUSION

The Performance analysis of proposed Multi Level Inverter was successfully carried out using MATLAB Simulink and PSIM software. Practically in a PV generation system, the output power delivered to a load can be maximized using MPPT control algorithm. The proposed cascaded H bridge multi level inverter using single carrier based open loop PWM switching technique proves improved power quality and reduced losses. The switching loss of the four switches is (TA+, TA-, TB+, TB-) almost negligible. The development of economic power conversion for solar energy will have high impact in the future. More than that, the proposed topology can be easily extended to higher level with introduction of less number of switching devices. The simulation results were sine waves and had fewer ripples and have low switching losses. This system would show its feasibility in practice.

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Karthika N received B.E. degree in Electrical and Electronics Engineering in C. Abdul Hakeem College of Engineering and Technology and pursuing M.E. degree in Rajalakshmi Engineering College, Anna University, Chennai. She has presented one International Conference and one National Conference.

Asst.Prof. Sangari A received B.E. degree in Electrical and Electronics Engineering in Sri Venkateswara College of Engineering and M.E. degree in Rajalakshmi Engineering College, Anna University, Chennai. Currently working as Assistant Professor, EEE, Rajalakshmi Engineering College, Chennai. Her research interest includes Multi Level Inverter. She has presented two International Conference and four National Conference

Dr. R. Umamaheswari did her BE in Electrical and Electronics Engineering and ME in Applied Electronics from PSG College of Technology, Coimbatore and PhD in High Voltage Engineering from IIT Madras. Currently working as Professor, EEE, Rajalakshmi Engineering College, Chennai. Her current field of research is High Voltage Technology and Industrial Electronics. She has published five papers in various Journals and has presented six International Conferences.