Implementation of Multiplier using Vedic Algorithm

Poornima M, Shivaraj Kumar Patil, Shivukumar , Shridhar K P , Sanjay H

Abstract :- Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in the early twentieth century from ancient Indian sculptures (Vedas). This paper proposes the design of high speed Vedic Multiplier using the techniques of Vedic Mathematics that have been modified to improve performance. A high speed processor depends greatly on the multiplier as it is one of the key hardware blocks in most digital signal processing systems as well as in general processors. Vedic Mathematics has a unique technique of calculations based on 16 Sutras. This paper presents study on high speed 8x8 bit Vedic multiplier architecture which is quite different from the Conventional method of multiplication like add and shift. Further, the Verilog HDL coding of Urdhva tiryakbhyam Sutra for 8x8 bits multiplication and their FPGA implementation by Xilinx Synthesis Tool on Spartan 3 kit have been done and output has been displayed on LED's of Spartan 3 kit .

Index Terms:- Architecture, Ripple Carry (RC) Adder, Multiplication, Vedic Mathematics, Vedic Multiplier (VM), Urdhava Tiryakbhyam Sutra

I. INTRODUCTION

. Vedic mathematics is the name given to the ancient Indian system of mathematics that was rediscovered in early twentieth century. Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as Sutras. We discuss a possible application of Vedic mathematics to digital signal processing in the light of application of Vedic multiplication algorithm to digital multipliers. A simple digital multiplier (referred henceforth as Vedic multiplier) architecture based on the Urdhva Triyakbhyam (Vertically and Cross wise) Sutra is presented. This Sutra was traditionally used in ancient India for the multiplication of two decimal numbers in relatively less time. In this paper, after a gentle introduction of this Sutra, it is applied to the binary number system to make it useful in the digital hardware. The hardware architecture of the Vedic multiplier is presented and is shown to be very similar to that of the popular array multiplier. It is also equally likely that many such similar technical applications might come up from the storehouse of knowledge, Veda, if investigated properly [1-3].

Pipeline architecture based on the constant geometry radix-2 FFT algorithm, which uses log2N complex-number multipliers (more precisely butterfly units) and is capable of computing a full N-point FFT in N/2 clock cycles, has been proposed by J.Choi and V.Boriakoff.

However, this architecture requires a large amount of delay elements (memory size of N.log2N samples) and a quite complicated switching mechanism for the routing of the data [4].

In the present age of digital communication various audio visual or any other perception signals are sampled on time [i.e. axis] and are quantized on amplitude [y- axis], to produce discrete version of the continuous signal .This results in the corresponding information being contained in a series of binary (0 & 1) sequence. Hence any processing or transformation of original signal boils down to suitable discrete mathematical operation applied to binary sequences [5-6]. Different algorithms exist to accomplish each of these tasks. The task themselves may include basic arithmetic operations like addition, subtraction, multiplication, division, matrix, squaring, exponential operations etc. While implementing these algorithms on digital computer, the prevalent VAN-NEUMAN architecture uses registers operations like shift, move, Compliment, add etc. to accomplish these basic arithmetic tasks. The actual CPU implementation of these operations is through suitable amalgamation of algorithm and implementing architecture. Though there are many algorithms for the same task only VAN-NEUMAN architectural implementation of classical method is found to be used in present day digital computers. The Vedic mathematical methods suggested by Shankaracharya Sri. Bharti Krishna Tirtha through his book offer efficient alternatives.

II. VEDIC MATHEMATICS (VM)

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda.

It covers explanation of several modern mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus. His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884-1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swamhiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae) after extensive research in Atharva Veda. The very word 'Veda' has the derivational meaning i.e. the fountainhead and illimitable storehouse of all knowledge. Vedic mathematics is the name given to the ancient system of mathematics or, to be precise a unique technique of calculations based on simple rules and principles with which many mathematical problems can be solved, be it arithmetic, algebra, geometry or trigonometry. The system is based on 16 Vedic sutras or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems. The beauty of Vedic mathematics lies in the fact that it reduces the otherwise cumbersome-looking calculations in conventional mathematics to a very simple one. This is so because the Vedic formulae are claimed to be

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based on the natural principles on which the human mind works. This is a very interesting field and presents some effective algorithms which can be applied to various branches of engineering such as computing and digital signal processing.

A. *These Sutras along with their brief meanings are enlisted below alphabetically*.

1) (Anurupye) Shunyamanyat -If one is in ratio, the other is zero.
2) ChalanaKalanabyham -Differences and similarities.
3) Ekadhikina Purvena- By one more than the previous One.
4) Ekanyunena Purvena -By one less than the previous one.
5) Gunakasamuchyah-Factors of the sum is equal to the sum of factors.
6) Gunitasamuchyah-The product of sum is equal to sum of the product.
7) Nikhilam Navatashcaramam Dashatah -All from 9 and last from 10.
8) Paraavartya Yojayet-Transpose and adjust.
9) Puranapuranabyham -By the completion or noncompletion.
10) Sankalana- vyavakalanabhyam -By addition and by subtraction.
11) Shesanyankena Charamena- The remainders by the last digit.
12) Shunyam Saamyasamuccaye -When the sum is same then sum is zero.
13) Sopaantyadvayamantyam -The ultimate and twice the penultimate.
14) Urdhva-tiryakbhyam -Vertically and crosswise.
15) Vyashtisamanstih -Part and Whole.
16) Yaavadunam- Whatever the extent of its deficiency.

Sub sutras or Corollaries

Proportionately

7) The remainder remains constant
8) The first by the first and the last by the last

For 7 the multiplicand is 143

- By osculation
- Lessen by the deficiency
- Whatever the deficiency lessen by that amount and Set up the square of the deficiency
- Last Totaling 10
- Only the last terms
- The sum of the products
- By alternative elimination and retention
- By mere observation
- The POS is the sum of the Products

On the flag [1]

III. IMPLEMENTATION OF MULTIPLIER USING VM ALGORITHM

Multiplication methods are extensively discussed in Vedic mathematics. Various tricks and short cuts are suggested by VM to optimize the process. These methods are based on concept of

1 Multiplication using deficits and excess

2 Changing the base to simplify the operation. Various methods of multiplication proposed in VM

a) UrdhvaTiryagBhyam - vertically and crosswise

b) Nikhilam navatashcharamam Dashatah: All from nine and last from ten

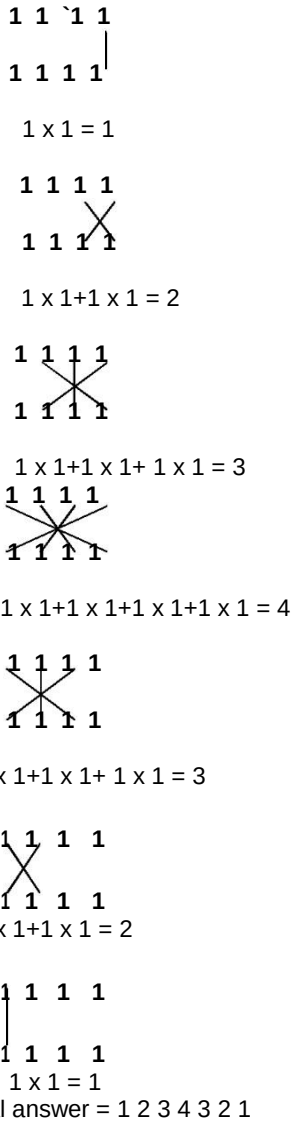
c) Anurupyena: Proportionately Vinculum

IV. URDHVA TIRYAGBHYAM

Urdhva – Triyakbhyam is the general formula applicable to all cases of multiplication and also in the division of a large number by another large number. It means vertically and crosswise. We discuss multiplication of two, 4 digit numbers with this method [8-9].

Ex.1. the product of 1111 and 1111 using *Triyakbhyam* (vertically and crosswise) is given below.

Methodology of Parallel Calculation



Final answer = 1 2 3 4 3 2 1

V. MULTIPLIER ARCHITECTURE

The hardware architecture of 2X2, 4x4 and 8x8 bit Vedic multiplier module are displayed in the below sections. Here, "Urdhva-Tiryagbhyam" (*Vertically and Crosswise*) sutra is used to propose such architecture for the multiplication of two binary numbers. The beauty of Vedic multiplier is that here partial product generation and additions are done concurrently. Hence, it is well adapted to parallel processing. The feature makes it more attractive for binary multiplications. This in turn reduces delay, which is the primary motivation behind this work.

A. Vedic Multiplier for 2x2 bit Module

The method is explained below for two, 2 bit numbers *A* and *B* where *A* = *a*1*a*0 and *B* = *b*1*b*0 as shown in Fig. 2. Firstly, the least significant bits are multiplied which gives the least significant bit of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. The sum is the third corresponding bit and carry becomes the fourth bit Of the finel product.

The 2X2 Vedic multiplier module is implemented using four input AND gates & two half-adders which is displayed in its block diagram in Fig. 3. It is found that the hardware architecture of 2x2 bit Vedic multiplier is same as the hardware architecture of 2x2 bit conventional Array Multiplier [2]. Hence it is concluded that multiplication of 2 bit binary numbers by Vedic method does not made significant effect in improvement of the multiplier's efficiency. Very precisely we can state that the total delay is only 2-half adder delays, after final bit products are generated, which is very similar to Array multiplier. So we switch over to the implementation of 4x4 bit Vedic multiplier which uses the 2x2 bit multiplier as a basic building block. The same method can be extended for input bits 4 & 8. But for higher no. of bits in input, little modification is required.

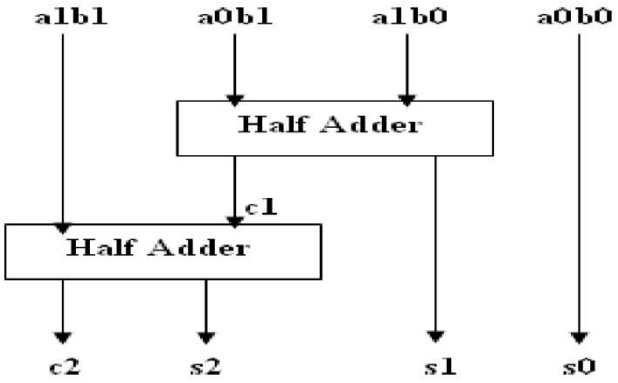
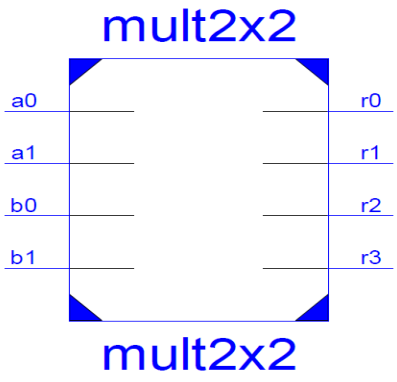


Fig. 3 Block Diagram of 2x2 bit Vedic Multiplier



Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	2	5888	0%
Number of 4 input LUTs	4	11776	0%
Number of bonded IOBs	8	372	2%

B. Vedic Multiplier for 4x4 bit Module

The 4x4 bit Vedic multiplier module is implemented using four 2x2 bit Vedic multiplier modules as discussed in Fig. 3. Let's analyze 4x4 multiplications, say A= A_3 A_2 A_1 A_0 and B= B_3 B_2 B_1 B_0. The output line for the multiplication result is – $S_7S_6S_5S_4$ S_3 S_2 S_1 S_0 .Let's divide A and B into two parts, say A_3A_2 & A_1 A_0 for A and B_3 B_2 & B_1B_0 for B. Using the fundamental of Vedic multiplication, taking two bit at a timeand using 2 bit multiplier block, we can have the following structure for multiplication as shown in Fig. 4.

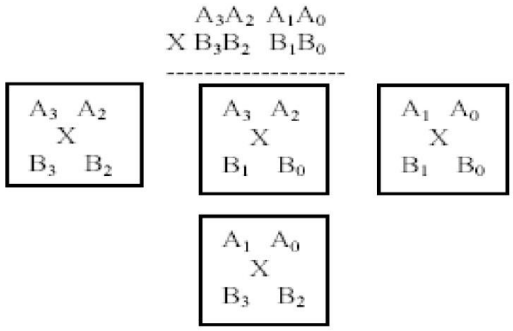


Fig. 4 Sample Presentation for 4x4 bit Vedic Multiplication

Each block as shown above is 2x2 bit Vedic multiplier. First 2x2 bit multiplier inputs are A_1A_0 and B_1B_0. The last block is 2x2 bit multiplier with inputs A_3 A_2 and B_3 B_2. The middle one shows two 2x2 bit multiplier with inputs A_3 A_2 & B_1B_0 and A_1A_0 & B_3 B_2. So the final result of multiplication, which is of 8 bit, S_7 $S_6S_5S_4$ S_3 S_2 S_1 S_0. To understand the concept, the Block diagram of 4x4 bit Vedic multiplier is shown in Fig. 5. To get final product (S_7 S_6 S_5 S_4 S_3 S_2 S_1 S_0), four 2x2 bit Vedic multiplier (Fig. 3) and three 4-bit Ripple-Carry (RC) Adders are required.

The proposed Vedic multiplier can be used to reduce delay. Early literature speaks about Vedic multipliers based on array multiplier structures. On the other hand, we proposed a new architecture, which is efficient in terms of speed. The arrangements of RC Adders shown in Fig. 5, helps us to reduce delay. Interestingly, 8x8 Vedic multiplier modules are implemented easily by using four 4x4 multiplier modules

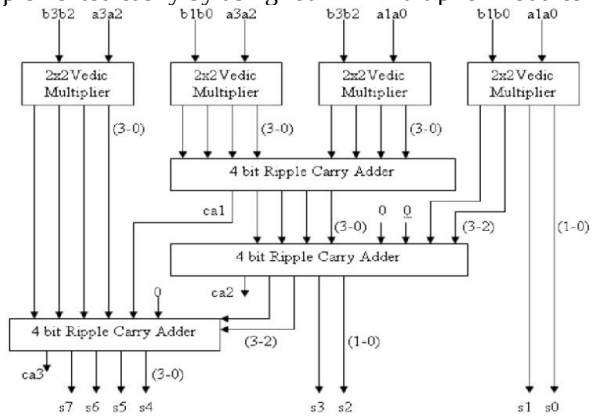
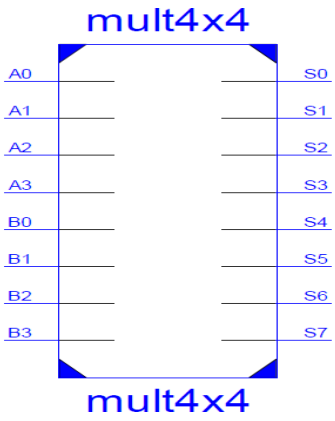


Fig. 5 Block Diagram of 4x4 bit Vedic Multiplier



Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	18	5888	0%
Number of 4 input LUTs	32	11776	0%
Number of bonded IOBs	16	372	4%

C. Vedic Multiplier for 8x8 bit Module

The 8x8 bit Vedic multiplier module as shown in the block diagram in Fig. 6 can be easily implemented by using four 4x4 bit Vedic multiplier modules as discussed in the previous section

Let's analyze 8x8 multiplications, say A= A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0 and B= B_7 B_6 $B5B_4$ B_3 B_2 B_1B_0. The output line for the multiplication result will be of 16 bits as – S_{15} S_{14} S_{13} S_{12} S_{11} S_{10} S_9 S_8 S_7 $S_{6b}S_5S_4$ S_3 S_2 S_1 S_0. Let's divide A and B into two parts, say the 8 bit multiplicand A can be decomposed into pair of 4 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL. The 16 bit product can be written as:

Using the fundamental of Vedic multiplication, taking four bits at a time and using 4 bit multiplier block as discussed we can perform the multiplication. The outputs of 4x4 bit multipliers are added accordingly to obtain the final product. Here total three 8 bit Ripple-Carry Adders are required as shown in Fig. 6.

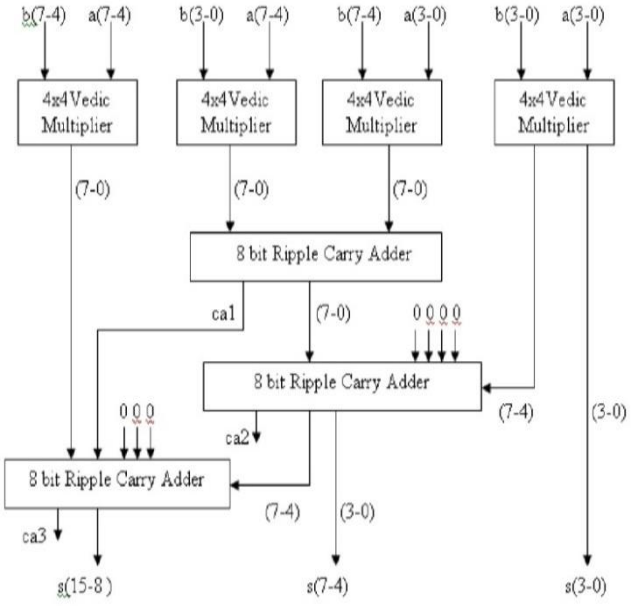
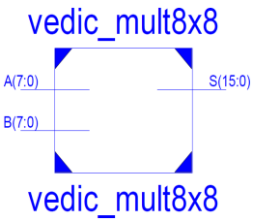


Fig. 6 Block Diagram of 8x8 bit Vedic Multiplier



Implimentation Design for 8x8

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	101	5888	1%
Number of 4 input LUTs	176	11776	1%
Number of bonded IOBs	32	372	8%

Simulation output of the 8x8 Multiplier
For the value 8h and 7h gives a result in hexadecimal 38 .

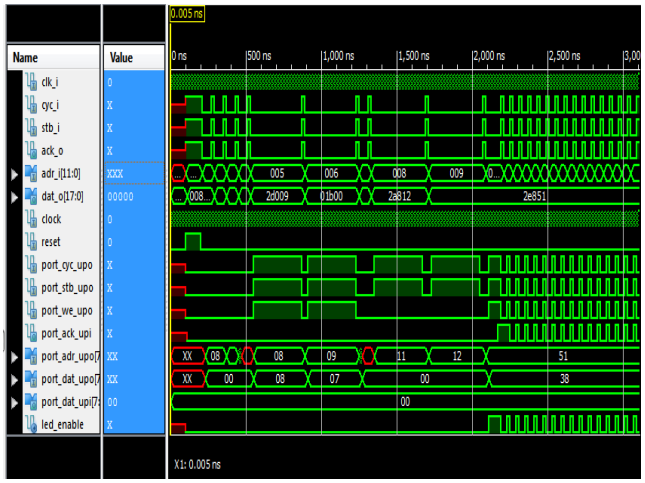


Table 1 Comparison of 8x8 bit Multipliers (in ns)

D. Generalized Algorithm for N x N bit Vedic Multiplier

We can generalize the method as discussed in the previous sections for any number of bits in input. Let, the multiplication of two N-bit binary numbers (where N = 1, 2, 3…N, must be in the form of 2^N) *A* and *B* where A = A_N.....A_3 A_2 A_1 and B = B_N….B_3 B_2 B_1. The final multiplication result will be of (N + N) bits as S = $S_{(N+N)}$....S_3 S_2 S_1.

Step 1: Divide the multiplicand A and multiplier B into two equal parts, each consisting of [N to (N/2)+1] bits and [N/2 to 1] bits respectively, where first part indicates the MSB and other represents LSB.

Step 2: Represent the parts of A as A_M and A_L, and parts of B as B_M and B_L. Now represent A and B as A_M A_L and B_M B_L respectively.

Step 3: For A X B, we have general format as shown in Fig.7

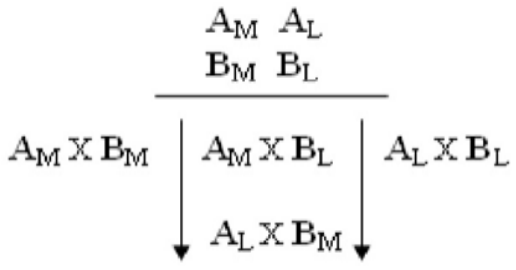


Fig. 7 General Representation for vedic multiplication

VI. CONCLUSION AND FUTURE WORK

This paper presents a highly efficient method of multiplication – "Urdhva Tiryakbhyam Sutra" based on Vedic mathematics. It is a method for hierarchical multiplier design which clearly indicates the computational advantages offered by Vedic methods. Authors implemented the code on Xilinx FPGA Spartan 3 board . The computational path delay for proposed 8x8 bit Vedic multiplier is found to be 28.27 ns. It is observed that the Vedic multiplier is much more efficient than Array and Booth multiplier in terms of execution time (speed). An awareness of Vedic mathematics can be effectively increased if it is included in engineering education.

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