8 Bit Second-Order Continuous-Time Band-Pass Sigma-Delta ADC

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Abstract*— In this paper, a technique to design the 8 bit continuous-time band-pass Sigma-Delta converters for 70 MHz is presented. The conversion from discrete-time (z-domain) loop-filter transfer function into continuous-time (s-domain) is done by using Impulse-invariant-transformation. The transconductor-capacitor filter is used to implement continuous-time loop-filter. A latched-type comparator and a TSPC D Flip-flop are being used as the quantizer of the Sigma-Delta converter. The decimation filter is designed by a CIC Filter and an FIR filter of high-speed digital. A full adder cell and a TSPC D Flip-flop are used as basic building blocks of CIC Filter and FIR Filter. The 8 bit second-order continuous Sigma-Delta converter circuit has been implemented in Cadence using 180nm CMOS technology and the total power consumption is 57.9 mW. At a supply voltage of 3 V, the maximum SNDR is measured to be 35.13 dB, which corresponds to a resolution of 8 bits.

Index Terms*— Analog-to-digital converter, Continuous Sigma-Delta ADC, Decimation Filter, Sigma-Delta modulator.

I. INTRODUCTION

Architecture for Radio communication receiver has been proposed in literature [1] and its block diagram is shown in Figure 1.The information in real world is inherently analog. The digital form of analog signals can be processed using robust, flexible and reliable digital-signal-processing (DSP) hence the ADC is required to convert analog signal to digital signal. The most optimal converter for a narrow-band signal at 70MHz is a Sigma-Delta ADC. A band-pass Sigma-Delta ADC is more desirable because it can achieve higher resolution while consuming less power.

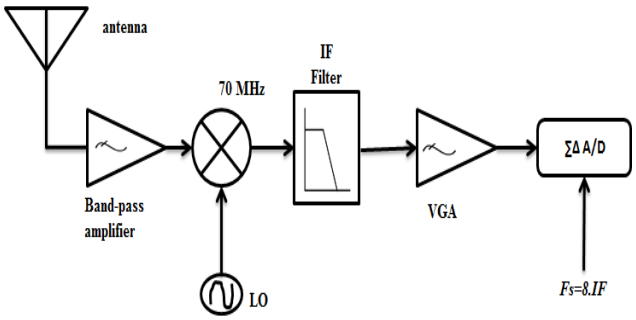

Fig. 1: Block diagram of the Single high-IF receiver architecture. [1]

The Band-pass Sigma-Delta ADC are usually implemented by switched-capacitor (SC) [2] technique. However, SC implementations is limited in that the sampling frequency of the modulators cannot be too high (below 50MHz).

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Even using the double-sampling technique [3] or 2-path technique [4], the center frequency of the band-pass signal is still limited to below 50 MHz. The multi bit Digital Decimation filter [5], [6] is used to genrate the 8 bit output. This paper presents the design and measurement of a 8 bit Second-order Continuous-time band-pass Sigma-Delta ADC for the reciver shown in figure 1.

As the design targets, the converter needs to have at least eight bits of resolution, which is equivalent to a signal-to-noise and distortion ratio (SNDR) of better than 35 dB for a 200 kHz bandwidth. For a 3V supply voltage, the total power consumption is desired to be less than 75 mW .

The transformation from discrete-time to continuous-time for the design of the band-pass Sigma-Delta ADC [7] is described in section II. The circuit designs for the implementation of the Sigma-Delta modulator is described in section III. The circuit designs for Decimation Filter are described in section IV. The experimental results of the sigma–delta ADC are presented in Section V. Finally, we summarize and conclude our work.

II. TRANSFORMATION FROM DISCRETE-TIME SIGMA-DELTA ADC TO CONTINUOUS-TIME SIGMA-DELTA ADC

The block diagram of the band-pass Sigma-Delta modulator is shown in Figure 2[1]. H(z) or H(s) are the transfer function of loop-filter depending on whether the modulator is discrete-time or continuous-time, respectively. The second-order discrete-time band-pass Sigma-Delta modulator implemented with a transfer function $H(z) = z^{-2}/(1+z^{-2})$.

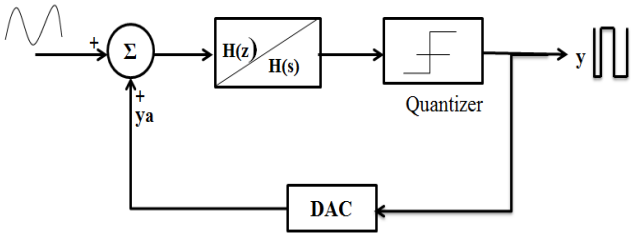

Fig. 2: Block diagram of a band-pass Sigma-Delta ADC [1]

As mentioned in section I, discrete-time system or switched-capacitor band-pass Sigma-Delta modulator cannot operate above 50MHz, due to the discrete-time nature of the modulator design, the DAC output waveform in the feedback loop of the ΣΔ modulator does not have much effect on the modulator performance. The variations of the digital-to-analog signal during the clock period φ and φ' are not seen by a switched-capacitor filter. Hence a continuous-time filter is needed to operate at 70MHz. The continuous-time filter responds to an input signal continuously, unlike the switched-capacitor filter that is discrete in nature. Therefore, a continuous-time ΣΔ loop-filter has to be designed according to the DAC output waveform.

There are differences between a continuous-time modulator and a discrete-time modulator are, Firstly, the loop-filter of the continuous-time modulator is a transconductor-capacitor filter or a LC filter, not a switched-capacitor filter or a switched-current filter in discrete-time modulator. Secondly, a sample-and-hold circuitry should be added in a continuous-time modulator, which in practice can simply be combined with the quantizer in the loop. To design a continuous-time modulator, the DAC transfer function should be defined and its waveform should be considered. A good performance 1-bit DAC can be implemented using a zero-order-hold circuitry with a transfer function of ZOH(s) $=1-e^{-sT}/s$ where T is the sampling period. Afterwards, a discrete-time Z-domain to continuous-time S-domain transformation should be done in order to implement a continuous-time band-pass ΣΔ modulator. Two common transformation scan be considered: bilinear transformation and impulse-invariant-transformation.

Bilinear transformation maps all frequencies in the S-domain to the Z-domain and vice versa, but the frequencies are non-linearly mapped. Impulse-invariant-transformation maps the frequencies linearly from –πfs/2 to πfs/2 while other frequencies will be aliased into the transformed band; therefore, anti-aliasing the signal is important when using this transformation. There is a 70 MHz band-pass IF filter before the modulator that served the anti-aliasing filter purpose for Single high-IF receiver. Therefore, for design simplicity, the impulse-invariant-transformation was chosen for modulator:

$$Z^{-1}[H(Z)] = L^{-1}\left[\frac{1-e^{-\Delta T}}{s} H(s)\right] \quad (1)$$

where *H(z)* is the discrete-time transfer function of the loop-filter in the modulator, *H(s)* is the continuous-time transfer function for the loop-filter, and $1\text{-}e^{-sT}/s$ is the transfer function of the DAC in the loop where T=1/*fs*.

In practical implementation, the quantizer is not delay-free. With an extra one delay, the discrete-time and continuous-time transfer function become:

$$H(z) = \frac{z^{-1}}{1+z^{-2}} \rightarrow H(s) = \frac{\pi}{4T}\left[\frac{s-\frac{\pi}{2T}}{s^2+\left(\frac{\pi}{2T}\right)^2}\right] \quad (2)$$

III. CIRCUIT DESIGN FOR THE IMPLEMENTATION OF SIGMA-DELTA MODULATOR.

A. Gm-C loop filter

A transconductor-capacitor (Gm-C) filter is used to implement the continuous-time loop-filter. Figure 3 shows the block diagram of the loop-filter, and Eq. (3) shows the corresponding transfer function implemented.

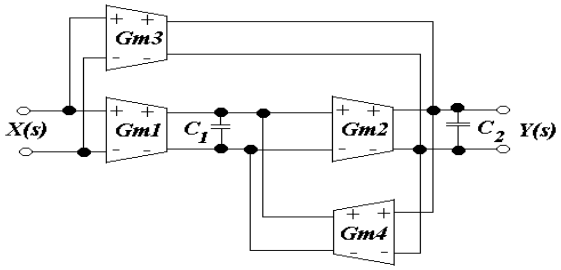

Fig. 3: Block diagram of the loop-filter.

$$H(s) = \frac{Y(s)}{X(s)} = \frac{\frac{Gm3}{C_2}s + \frac{Gm1.Gm2}{C_1.C_2}}{s^2 - \frac{Gm2.Gm4}{C_1.C_2}} \quad (3)$$

The basic block of the loop-filter are Gm-cell and capacitor. The Source degeneration Gm-cell with negative-impedance-compensation(NIC) technique is used to design loop-filter. The output impedance is in the order of tens of kΩ for normal Source degeneration Gm-cell. Hence NIC technique is used to increase the outpu impdence to MΩ.the Figure 4 shows the schematic of the CMOS source-degeneration Gm-cell with the NIC circuit implementation in cadence.

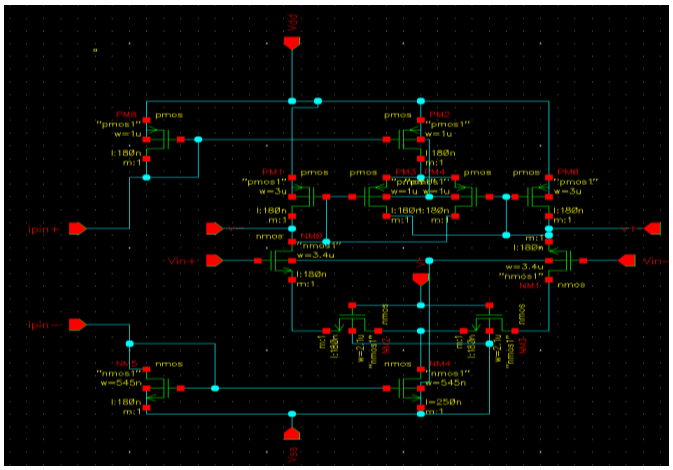

Fig.4: Schematic of the CMOS Source-degeneration Gm-cell with NIC circuit.

B. Quantizer design

To combine the sample-and-hold function and the comparator function in a quantizer, the latched-type comparator is the best choice. Figure 5 depicts the Schematic of the CMOS latched-type Comparator in the quantizer design.

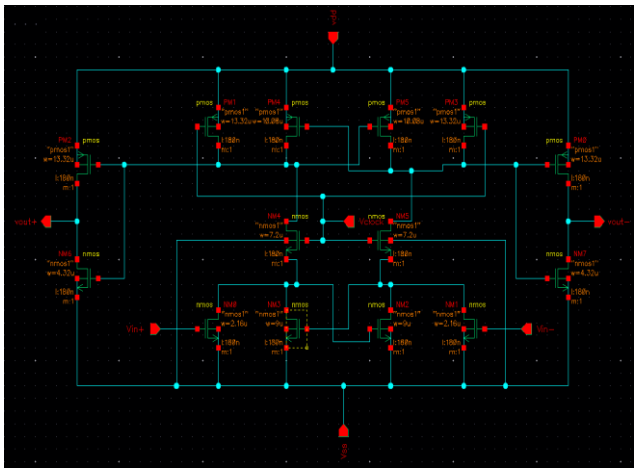

Fig. 5: Schematic of the CMOS latched-type Comparator.

In order to convert the return-to-zero (RZ) output of the comparator to a NRZ output, a D flip-flop is added after the latched-type comparator. It is too slow for usual static D flip-flop to be used in a 560 MHz sampling system, therefore, a TSPC D flip-flop is chosen. Figure 6 shows the schematic of the design of the TSPC D flip-flop.

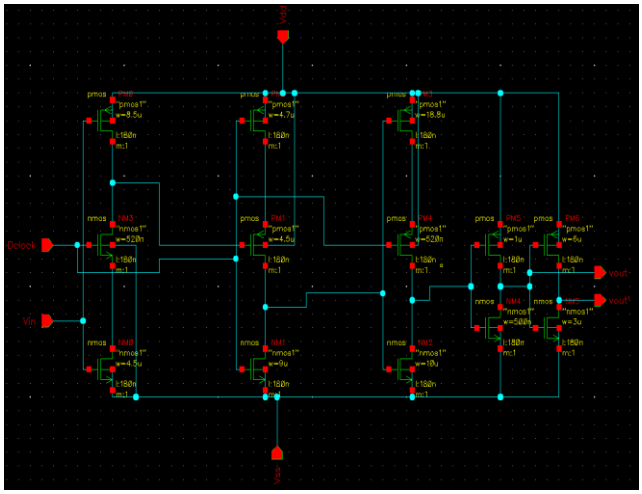

Fig. 6: Schematic of the TSPC D flip-flop.

This D Flip-flop design also using in designing of Decimation Filter there we using Vout as output but in Quantizer Design in order to convert the return-to-zero (RZ) output of the comparator to the NRZ output we considering Vout' as output.

A feedback DAC is required for continuous-time Gm-C implementation of the ΣΔ modulator. The DAC should be linear and fast, therefore, 1-bit quantizer architecture is chosen and hence a 1-bit DAC are designed. The feedback DAC for the ΣΔ modulator using *180nm* is implemented by a simple differential-pair to convert the output voltage to a current level. The adder is done by current addition of the Gm-cell current output and the current output of the DAC. Figure 7 shows the circuit of the Gm-C loop-filter with the feedback DAC. Figure 8 shows the schematic of CMOS current steering feedback DAC

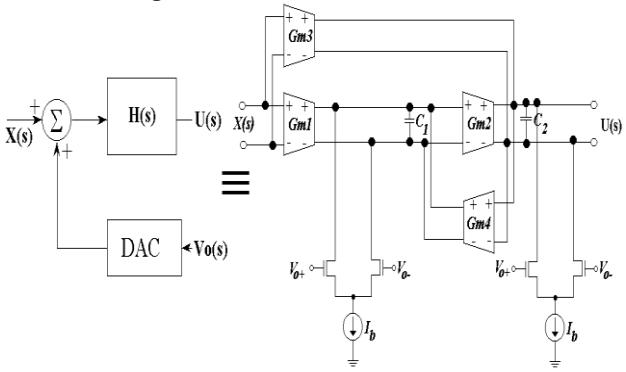

Fig. 7: The circuit of the Gm-C loop-filter with the feedback DAC.

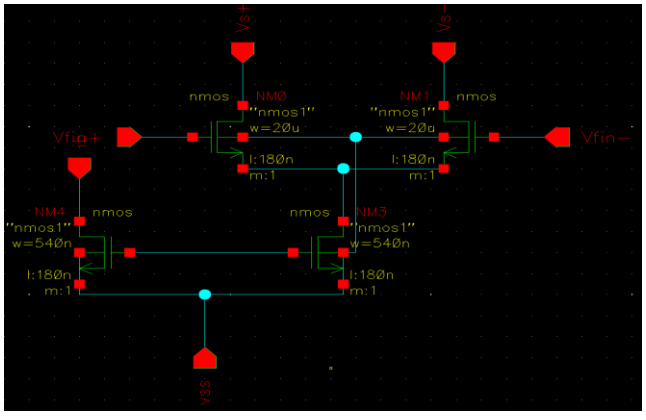

Fig. 8: Schematic of the current steering feedback DAC.

IV. CIRCUIT DESIGN FOR DECIMATION FILTER

The Decimation filter for the delta-sigma modulator output is implemented as a Complex low pass filter (LPF), i.e., the input stream of band pass signal is modulated into two low pass streams and filtered separately. This low pass filter has as its first stage a CIC filter followed by FIR filters for compensation and band limitation to eliminate aliasing caused by down sampling. The realization of the filter using full adder and the D flip-flop is presented in the following sections.

A. Full Adder

Pass transistor logic has high logic functionality. Hence Full adder designed with a 16 transistors in pass-transistor style. Figure 9 shows the 16-Transistor Full Adder Cell implementation in Cadence tool.

The same Quantizer design TSPC D flip-flop is used for Digital Decimation filter design.

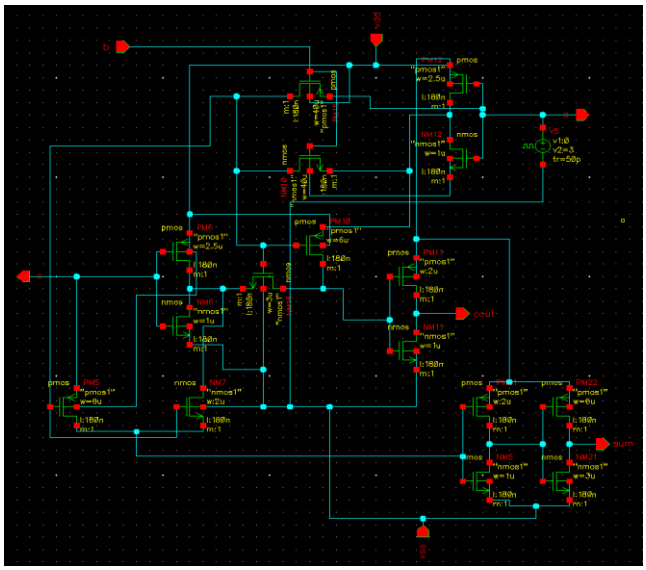

Fig. 9: The Schematic of 16-Transistor Full Adder Cell implementation in Cadence tool.

B. CIC Filter

The CIC filter receives the samples from the modulator and operates at the highest sampling frequency of the filter. This filter needs to attenuate the quantization noise that aliases into the desired band of the modulator and hence needs to be of a greater order than the modulator. The sigma-delta modulator whose output serves as the input to the filter is of third order. For a decimation factor of 2, the transfer function

$$H(z) = (1 + Z^{-1})^{k} \quad (4)$$

where k is the order of the filter.

The presence of integrators in the filter transfer function leads to the filter output word length being greater than that of the input. This bit growth is given as,

$$B_0 = k.\log_2 (N) + B_i \quad (5)$$

Where k is the filter order, N is the decimation ratio, B_i is the input word length and B_o is the output word length.

Figure 10 illustrates the schematic of the basic computational element of CIC Filter. And the realization of the third order filter using a cascade of the computational element is shown in Figure 11.

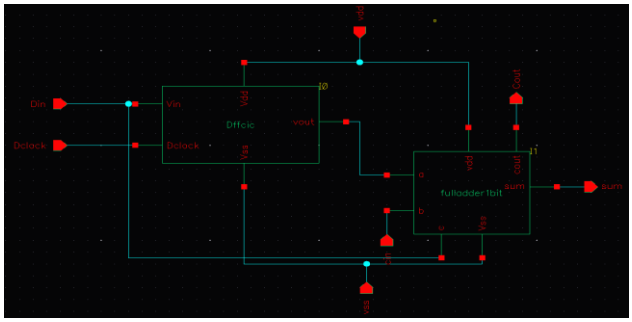

Fig. 10: Basic computational element of CIC filters.

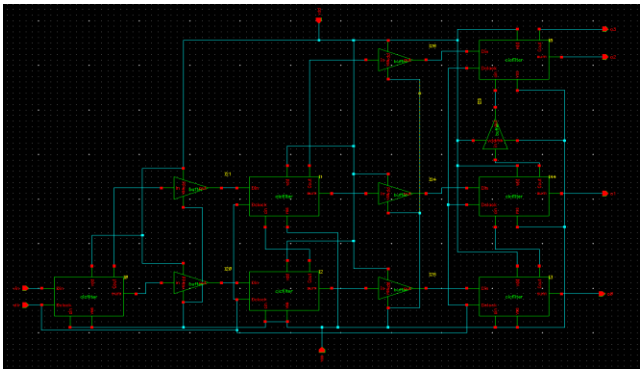

Fig. 11: Schematic of third Order CIC Filter

C. FIR Filter

The FIR filter following the CIC filter is used to remove the ripples caused by the CIC filter in the frequency response in the desired band. The CIC filter does not have a flat pass band response. The magnitude response droops slightly toward the edge of the pass band. The transition from the pass band to the stop band for the CIC filter is not smooth and sharp. The FIR filter with a linear response is used to compensate for these shortcomings of the CIC filter. It is also used to limit the bandwidth so that the high frequency components do not alias into the pass band.

The 1-bit FIR implementation is shown in Figure 12. It realization with the full adder cells acting as 3-2 compressors. The flip-flops serve as delay elements as their output appears one clock cycle after the input is latched. The delayed outputs are added with the current value of the input and the resulting output is fed to the next delay stage. The final output has a two bit output for each bit of input. These are added together using a ripple carry adder (RCA) and the final output generated. The schematic of the ripple carry adder is shown in Figure 13. From this FIR Filter we can achieve the decimation ratio 2. The output word length is limited to 4 bits. The schematic of the 4-bit filter is shown in Figure 14.

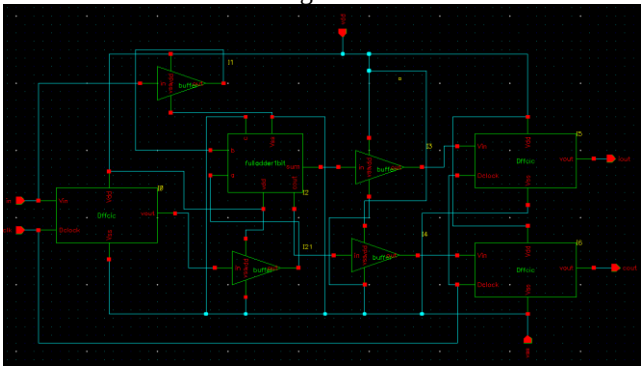

Fig. 12: Schematic of the 1-bit FIR filter

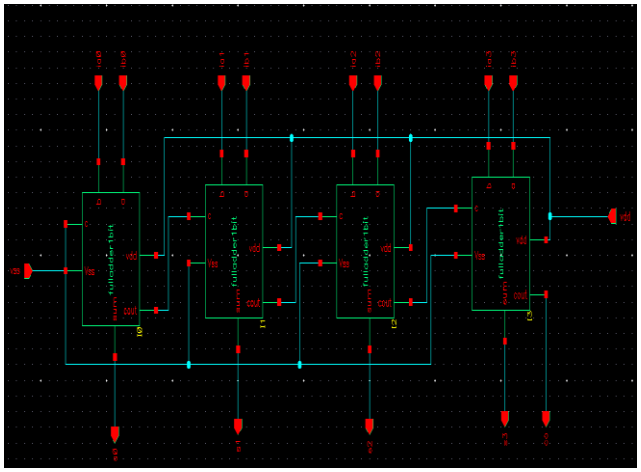

Fig.13: Schematic of the Ripple Carry Adder (RCA)

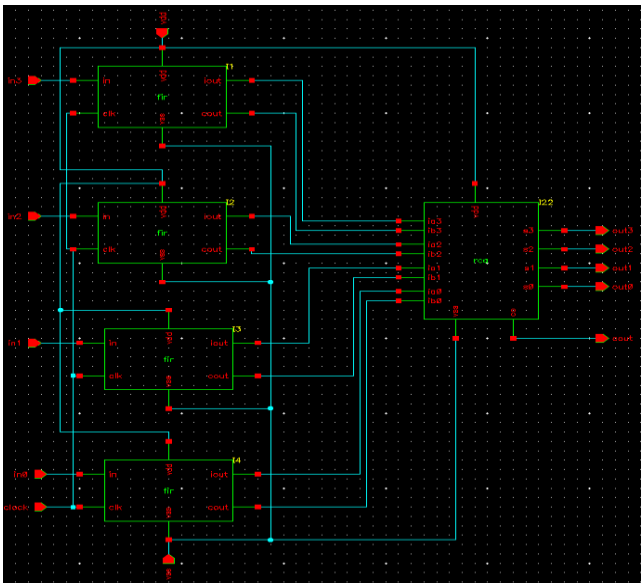

Fig. 14: Schematic of the 4-bit fir filter

V. EXPERIMENTAL RESULTS

The Figure 15 shows the test circuit of 8 bit Sigma-delta ADC Circuit design. The transient simulation results of the circuit are shown in Figures 16 for a time interval 30 ns.

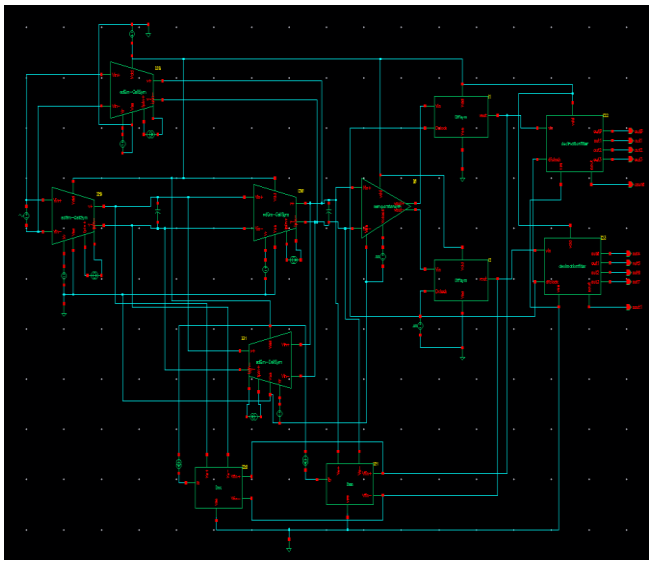

Fig. 15: Test circuit of 8 bit Sigma-delta ADC Circuit

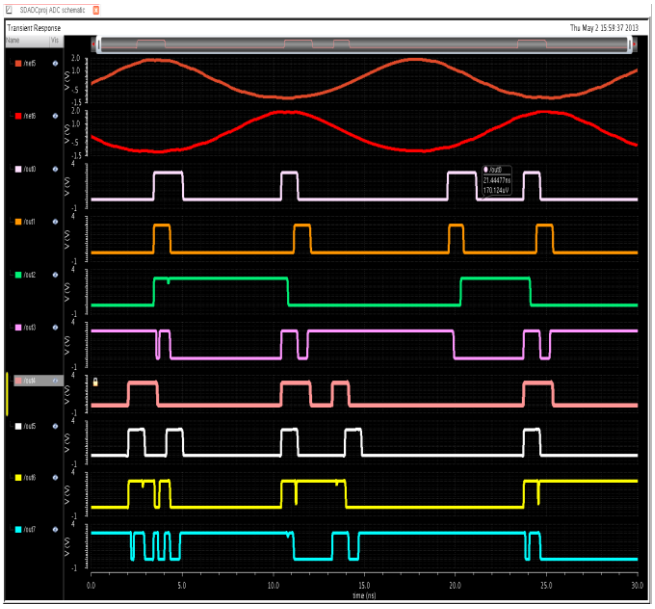

Fig. 16: Test circuit of 8 bit Sigma-delta ADC Circuit

The below Figure 17 shows power simulation result of 8 bit Sigma-delta ADC. The corresponding power value of the result waveform is 57.9e-3 (57.9 mW).

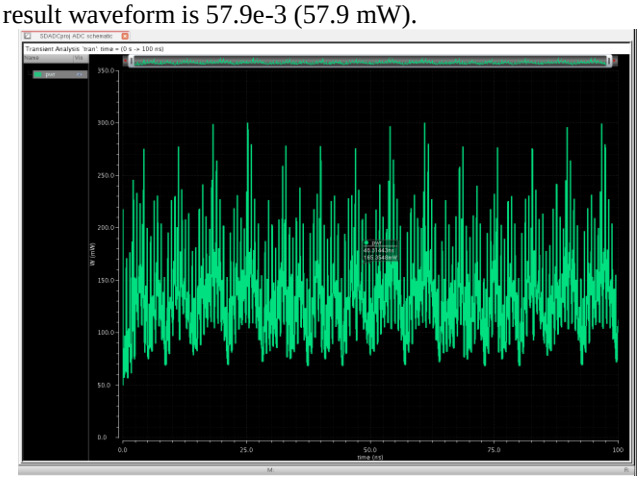

Figure 17 Power simulation result of 8 bit Sigma-delta ADC

The below Figure 18 shows spectrum result of Sigma-delta modulator which gives the values of SNDR, SNR, and ENOB.

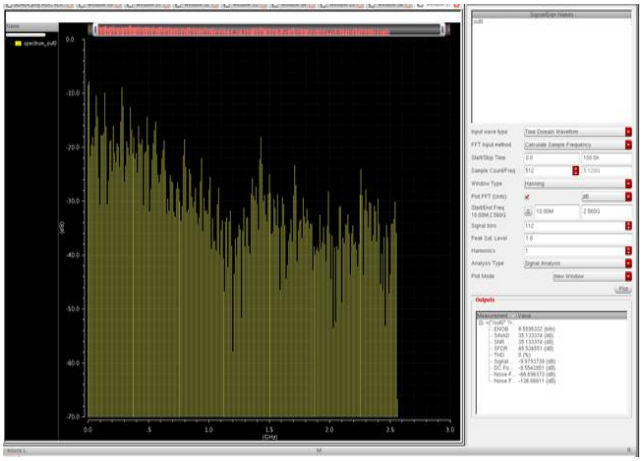

Fig. 18: Spectrum result of 8-bit Sigma-Delta ADC

The Table 1 shows the summarized simulation results of the 8 bit Sigma-delta ADC.

Table 1: Summarized simulation results of the 8-bit Sigma-delta ADC.

Parameter	**Specification**
Technology	CMOS 180nm
Operation frequency	560 MHz
Input frequency	560 MHz
Output Frequency	140 MHz
Decimation factor	4
ENOB	8.56 bites
SNDR	35.13 dB
Rise time	25.64 ps
Fall time	19.69 ps
Propagation delay	3.09 ns
Power	57.9 mW
Power supply	3v

VI. CONCLUSION

The design and experimental results of a 8-bit continuous-time band-pass Sigma-Delta ADC has been presented. This ADC suitable for Single high-IF receivers. It has been shown that the continuous-time Sigma-Delta ADC contains an implicit anti-alias filtering in comparison to the discrete-time (switched-C) ADC, which is a significant advantage for band-pass ADC's.

The proposed Sigma-Delta ADC can achieve a maximum SNDR of 35.13 dB, while operating at 3 V and consuming only 57.9 mW, which is at least 3 times smaller than the others.

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