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FPGA Implementation of MPLS

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***Abstract*— This paper presents a hardware architecture of Multi-Protocol Label Switching (MPLS). MPLS is a protocol used primarily to prioritize internet traffic and improve bandwidth utilization. MPLS solutions are meant to be used with Layer 2 or Layer 3 protocols. This paper presents hardware architecture to implement MPLS on FPGA.**

***Index Terms*— Bandwidth, FPGA, Internet traffic, MPLS.**

I. INTRODUCTION

Today's Internet applications like Voice over Internet Protocol (VoIP), real-time video streaming, video calling requires very high data-rates. If the resources are limited then the network gets congested and high speed applications perform poorly. Increasing bandwidth is one of the options for these networks. However increasing bandwidth alone is not sufficient and there is a need for efficient prioritization of traffic and network resources.

Traffic Engineering (TE) and Quality of Service (QoS) is used to prioritize internet traffic and use network resources efficiently to provide services for Internet applications. TE and QoS is used to create Virtual Private Networks (VPN) services which are dynamically defined, created and activated to satisfy QoS parameters.

MPLS is a protocol framework which is defined and created for efficient and faster packet processing. MPLS implementations exist today are mostly software based due to its complexity. But software implementations tend to reduce overall performance of the network since packet processing can take the order of milliseconds and that kind of delay can reduce the performance of the network and also cause loss of data in high speed networks. Hence hardware implementations have been researched.

This paper is organized into the following sections. The second section gives the brief description of related work done in this area. The third section provides an overview of MPLS and explains its basic characteristics including the techniques used and the protocols necessary. In fourth section hardware architecture is proposed and last section gives the conclusion and future works of this project.

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II. RELATED WORK

MPLS is comprised of different protocols, each performing a different task in the MPLS work flow. Each protocol have been researched differently with respect to hardware implementation.

The work in [2] describes hardware implementation of IS-IS protocol. In [3] research on hardware implementation of OSPF protocol is discussed. Research in [4] and [5] discuss the hardware implementation of subset of RSVP-TE and CR-LDP protocols respectively. The work in [7] describes the hardware implementation of reconfigurable MPLS router.

The work in [6] has introduced a hardware processor for the implementation of MPLS using RSVP-TE as its signaling protocol. In [8], an embedded architecture for the MPLS protocol was proposed. The design uses both hardware and software to implement different aspects of MPLS. The architecture proposed implementing routing functionality in software, label switching functionality in hardware.

III. MPLS OVERVIEW

In MPLS, data transmission is performed on two types of routers. Label Edge Router (LER) is a device that operates at the edge of the access network and MPLS network. An LER typically contain interfaces to dissimilar networks (such as ATM, Frame Relay or Ethernet) and perform the task of assigning or removing the label from the packet as the traffic enters or exits an MPLS network.

An LER that forwards traffic onto the MPLS network from the access network is called Ingress LER and an LER that distributes traffic back to access network from the MPLS network is called Egress LER. When Ingress LER receives a packet, a label is attached to that packet and forward onto MPLS network and when Egress LER receives packet, label is removed from the packet and traffic is distributed back to the access network.

An Label Switch Router (LSR) receives packet from the LSR or an LER. When LSR receives packets, it analyses the label and forward the packet to an LER or LSR depending on the label contents. LSRs form the core of the MPLS network.

LSR is connected to another LSR or an LER. Packets are received through an access network and forwarded to and LER, this LER forward the packets to next LSR depending upon the Label Switched Patch (LSP) established. The packets travels through different LSRs before reaching the Egress LER which forward the packet back onto the access network.

A typical MPLS router is shown in fig 1[8]. Each LER is connected to different access network and MPLS network.

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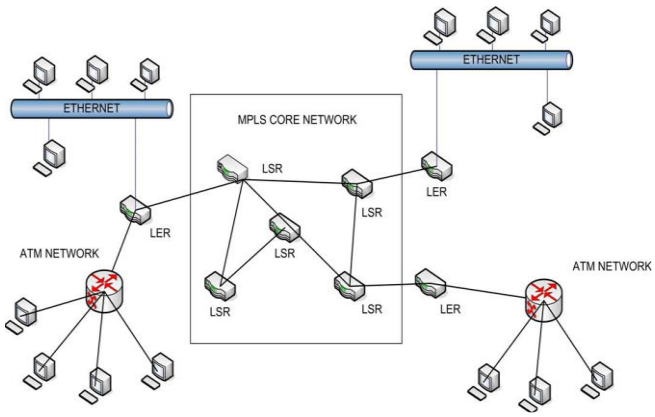

Fig 1. MPLS Network

Fig 2 shows a set of packet exchanges when a packet travels through the MPLS network [8]. When the ingress LER receives packet from the access network, it is analyzed and a label is added to the packet. The new packet is then forwarded to the next LSR. Subsequent LSRs analyze the label, remove it and attach a new label so the next MPLS router can correctly interpret the label information. When the packet reaches the egress LER, the label is removed and the packet is forwarded to the appropriate access network.

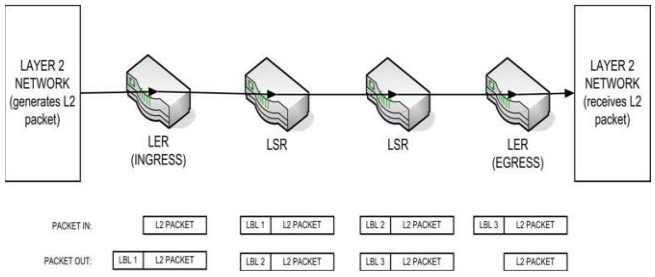

Fig 2. MPLS Packet Exchange

Figure 3 illustrates the generic label format as described in [1]. Each MPLS label is 32 bits long with components for the label, Class of Service (denoted as 'CoS'), a bit to denote the bottom of the stack (denoted as 'S') and a time to live (TTL) field. The label gives information needed to forward the packet and is the basis upon which MPLS switching operations occur.

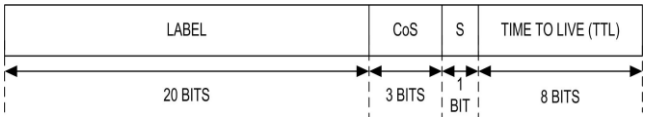

Fig 3. MPLS Label

The CoS bits affect the scheduling and or discard algorithms applied to the packet as it is transmitted through the network. The S bit is set to one for the last entry in the label stack and zero for all other label stack entries. As described in [1], the TTL is decremented by one each time the packet passes through a router. The packet is discarded when the TTL reaches zero.

IV. HARDWARE DESIGN

Fig 4 illustrated a high level description of the MPLS architecture. The architecture consists of the label remove module, label bind module and look-up table module.

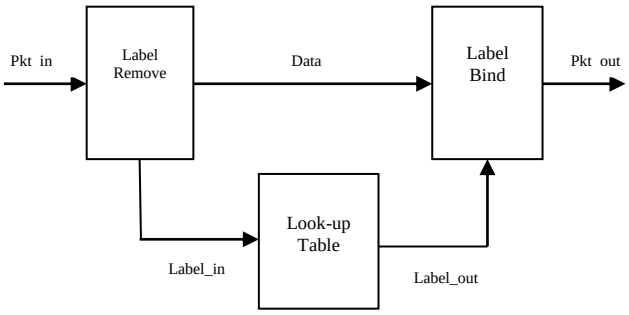

Fig 4. MPLS architecture

The packet coming from input port is sent to label remove Module. The label remove module strips off the label from the packets and checks the control information obtained from the label such as TTL and CoS and identifies modification that has to be performed to the packet whether to forward, discard or modify the packet and then send the label to the Look-up Table Module.

The Look-up Table stores and retrieves the label pairs. For each input label a corresponding output label is fetched from the look-up table. An Ingress LER does not have an incoming label and an Egress LER has not outgoing label. Those values are presumed to be zero.

The Label Bind Module gets the new label from the look-up table and other control information such as TTL, CoS from the label remove module. The label bind module constructs the 32-bit label and binds with the packet data. After constructing the complete packet they are forwarded to output port.

V. RESULTS

The MPLS architecture was implemented using Verilog hardware description language. These descriptions were then processed by standard Xilinx ISE 10.1 design tool suite, which performed synthesis, placement, routing, and bitstream (FPGA physical programming information) generation.

The bitstream generated was dumped onto XC2VP30 device of Xilinx Virtex 2 pro family. The number of slice flip flops used was 2396 and the number of 4 inputs LUT's used was 965, representing 8% and 3% of the total resources available.

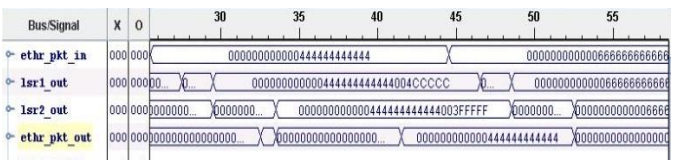

Fig 5.FPGA output

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Fig 5 shows the FPGA output of the implemented design. The figure shows the label attached to the output of LSR1 and LSR2 output shows the new label replaced with LSR1 label.

VI. CONCLUSION

In this paper, MPLS hardware architecture was proposed. The design was focused on MPLS hardware realization and the advantages of packet forwarding on hardware. The design was completely implemented on hardware. This prototype implementation of MPLS on FPGA hardware has demonstrated the potential for 100x speedup when compared to software implementations.

The architecture presented here satisfies the space requirements of most reconfiguration computing environments and can be implemented to achieve efficient performance of MPLS.

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