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On-Chip High Speed Optical Interconnect with RLCG Electrical Interconnect: Challenges and Dimensions

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Abstract*—Intrachip optical interconnects(OIs) have the potential to outperform electrical wires and to ultimately solve the communication bottleneck in high-performance integrated circuits. Performance targets and critical directions for Ics progress are yet to be fully explored. In this paper, the International Technology Roadmap for Semiconductors (ITRS) is used as a reference to explore the requirements that silicon-based Ics must satisfy to successfully outperform copper electrical interconnects (IEs). Consiering the state-of-art devices, these requirements are extended to specific IC components.

***Index Terms*-Integrated optoelectronic circuits, optoelectronics, optical interconnects(ICs), silicon photonics.**

I. INTRODUCTION

The communications bottleneck is identified as one of the grand challenges in the progress of silicon computation[1]. While individual logic elements have become significantly faster, computational speed is limited by the communication between different parts of a processor. Optical interconnects(OIs)can provide a solution to the communication bottleneck by replaci-ng electrical wires with faster optical waveguide[1].

Three levels of interconnects can be identified: 1) board-to-board; 2) chip-to-chip; 3) intrachip. While OIs on the backpla-ne and interchip levels are actively under development now [2], wheather intrachip OIs are feasible remains an open question. To support the sufficient density of interconnections and integ-ration with CMOS processing, OIs should be monolithically fabricated using CMOS compatible silicon-based materials and processes. Until recently, such device did not exist.

Over the past few years, significant progress has been made in the development of silicon-based building blocks for on-chip OIs, including light sources[3], [4], [5], waveguides[6], modul-ators[7], [8], and detectors[9], [10]. While some predictions have been made[11], [12], there is as yet no clear performance specifications for intrachip optical components to effectively replace electrical interconnects(EIs) [13]. In this paper the International Technology Roadmap for Se-miconductors (ITRS) is used to predict the EI performance, Manuscipt received December 24, 2005; revised May 30, 2006. This work was supported by the National Science Foundation under Grant CCR-0304574.

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Digital object identifier 10.1109/JSTQE.2006.880615
[Online]. Available: http/public.itrs.net/ as a target for OI requirements[1]. From an analysis of parameters such as delay, bandwidth density, and power consuption, the requirements for individual OI components are identified. While the delay is an important metric for interconnect performance, the power and area budgets are as important for determining system performance. Our paper also identifies OI weaknesses and missing components.

Finally it is important to differentiate between local and global intrachip interconnects. Local interconnects have a delay of less than one clock cycle, while global interconnects typically take longer than one or two clock cycles. Local interconnects are used for short-distance communication and comprise the majority of on-chip wires. While there are fewer global interconnects, these links are no less important. Improving the performance of a small number of critical global links can significantly enhance the total system performance. Section II shows that OIs are better suited for long-distance communications. Therefore, a comparison between electrical and optical global interconnects is the primary focus of this paper.

The rest of the paper is organized as follows: basic theory of transmission line when considered as a distributed RLCG model is discussed in section 2. Section 3, discusses unit impulse function which is consider as an input for delay calculation. Proposed model of RLCG interconnection network is given in section 4, Simulation results are given in section 5 and finally section 6 concludes the paper.

II. EIS ROADMAP

Modern on-chip EIs utilize copper wires surrounded by a low-k dielectric to transmit a signal[14]. Long wires used for global interconnects tend to exhibit higher RC time constants, which increases the interconnect delay, transition time, and crosstalk noise. In submicrometer CMOS technologies, repeaters [15] (or electrical signal amplifiers) are widely used to break long wires into smaller parts, as shown in Fig. 1(a). Repeaters drive smaller individual wires segments, thereby reducing the overall interconnect delay and making the overall delay linear with line length rather than quadratic.

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The delay due to the wires becomes smaller when the number of repeaters increases, but there is a delay and power supply associated with the repeater circuitry. Therefore for a fixed interconnect geo-metry, there exists an optimal repeater size and spacing to achieve a minimum delay[16]. In the following discussion, only Eis with optimized repeaters are considered.

When modeling metal wire interconnects operating at mul-ti gigaheartz clock rates, it is important to consider three impedance characteristics of the wire-resistance, capacitance, and inductance. In this paper, an RLC interconnect with equa-lly spaced repeaters is examined for different technology nodes.[1] Three degrees of freedom-the wire width, and the number and size of the repeaters-are explored to determine the minimum signal propagation delay. The delay model for the interconnect is an Extension of work described in[17] and includes the effects of repeater output capacitance and input signal transition time.

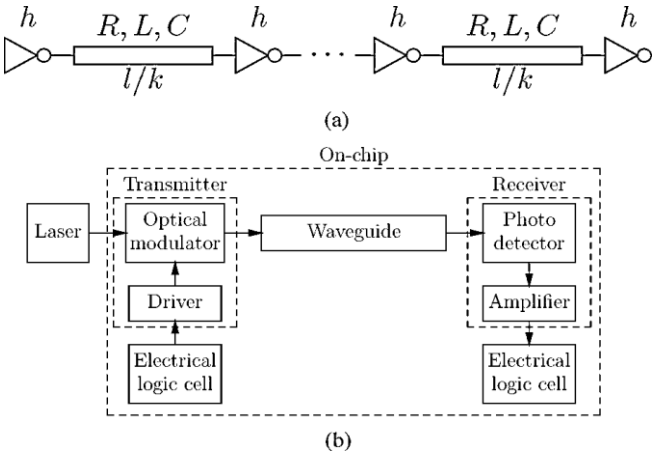

Fig. 1. (a) Circuit schematic of the EI system (b) Block dia-gram of the OI system.

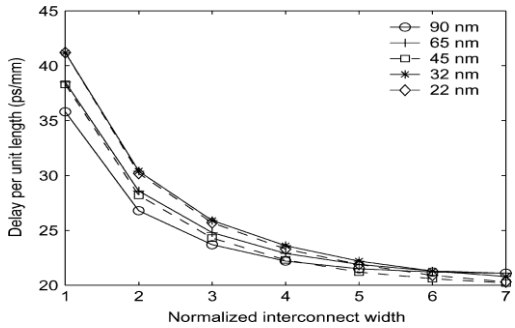

Fig. 2. Propagation delay of EI at different technology nodes versus normalized interconnect width.

Two of the main parameters characterizing on-chip interco-nnects are the propagation delay and the interconnect band-width density. The EI delay can be reduced by increasing the interconnect width at the expense of a smaller bandwidth density. In Fig. 2, the minimum EI delay per unit length is plotted as a function of wire width for different technology nodes. Note that technology scaling has insignificant effect on the delay of an interconnect with an optimal number of repeaters. The minimum achievable interconnect delay remains effectively fixed at approximately 20 ps/mm when technology scales from 90nm(year2004) to 22nm(year2016). Here, the maximum bit rate for a single interconnect is assumed to be the clock rate. With this assumption, the bandwidth density increases due to the smaller wire pitch and higher clock rate.

There are two major strategies for designing interconnects. Bandwidth density optimized interconnects utilize minimum-sized wires but exhibit a large RC impedance. Delay optimized interconnects sacrifice bandwidth density in favor of lower del-ay by using wider wire. OIs are likely to initially benefit global interconnectons, as EI-based global interconnects are typically delay-limited. Therefore, only elay-optimized Eis are consider-ed for comparision with OIs. The estimated power consump-tion per unit length for delay-optimized Eis with optimal repea-ters is of the order of 1 mW/mm and is expected to slowly increase[12].

From this analysis, technology scaling is not expected to significantly change the EI delay; however, the EI bandwidth density is expected to increase with time. Therefore, progress in OIs must recognize that the performance of intrachip Eis is a moving(and improving) target.

III. OIs: Configuration and Advantages

A. *Monolithic VLSI Technology: Advantages and Limitations*

The introduction of OIs into high-performance, high-complexity integrated circuits requires monolithic integration with standard electronic logic circuits. Microelectronics mono-lithic fabrication is perhaps one of the most robust and high-yield technologies in modern industry, resulting in low cost and ultrahigh levels of device integration. The number of materials and processes available for OI fabrication, however, is limited to those technologies that are compatible with microelectronics.

An important consequence of these limitations is the absence of efficient monolithic on-chip light sources. While a number of exciting scientific achievements have recently been published in the area of optical gain in silicon[3], [18], [19], high-speed, electrically driven, monolithic light sources are far from reality. It is, therefore, assumed that the most likely optimal transmitter configuration is a silicon-compatible electro-optic modulator with an external laser light source. In this paper, an OI system that consists of three main parts is considered: 1) an on-chip light modulator for signal switching; 2) a waveguide to guide thelight, and 3) a photodetectoras areceiver. This system is illustrated in Fig. 1(b). An off-chip laser is assumed to be the light source for the OI system.

The modulator and detector have conflicting requirements with respect to light absorption. The modulator material should be transparent to minimize insertion losses, while the detector material must absorb light to generate charge carriers. Thus, different materials should be used as detector and modulator, e.g., germanium and silicon. As a result, the wavelength range between the absorption edges in silicon and germanium defines the available wavelengths for signal modulation and detection.

B. *Optical Waveguides: Delay Advantages*

Minimizing the signal propagation delay is the primary interconnect requirement for the majority of very large scale integration (VLSI) architectures. In this respect, OIs process the intrinsic advantage of high signal propagation speed in optical waveguides, especially when the signal dispersion is negligible.

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A comparison of signal propagation delays in EI and the two common types of optical waveguides- a polymer waveguide and a silicon waveguide- is shown in Fig. 3. Low refractive index polymer and high refractive index silicon waveguides are chosen for comparison with EIs, as these structures represent

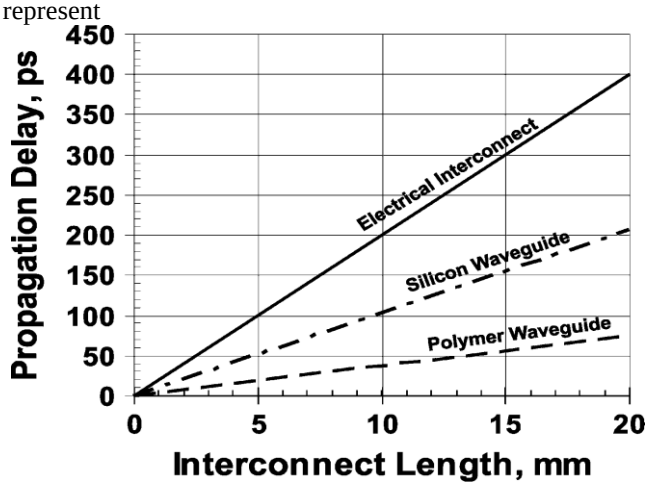

Figure 3.Propagation delay of silicon and polymer wave-guides as compared to EIs. The R-Soft full-vectorial finite-difference time-domain (FDTD) solver has been used to determine the waveguide properties. Both types of optical waveguides have a square cross section and are assumed to be surrounded by a cladding with a refractive index of 1.1. The core of the silicon waveguide is 0.34μm wide and has a refractive index of 3.4. The core of the polymer waveguide is 1.36 μm wide and has a refractive index of 1.3.two opposite types of optical waveguides in terms of signal propagation delay and crosstalk. Note that optical waveguides provide a significant advantage in propagation delay over electrical wires regardless of the waveguide material. Optical signal propagation is intrinsically faster than electrical propagation due to the absence of *RLC* impedances. While the majority of VLSI architectures are delay-limited, an effective choice for intrachip interconnects is low-delay polymer waveguides that can be realized, e.g., with low-loss optical polymers [20].

In order to exploit the propagation delay advantage offeredby optical waveguides, it is necessary to first convert the electricalsignal into light and then back into an electrical signal.This conversion has a fixed delay, which is nearly independentof the interconnect length for a given technology. Hence, OIstend to have a delay advantage in longer connections, when thewaveguide propagation delay dominates the overall delay.

IV. OIS VERSUS EIS

A. Transmitter and Receiver: Conversion Cost and Power-Delay Product

To be considered as a candidate for replacing EIs, OIs should exhibit advantages in both delay and power for critical long-distance intrachip interconnections. If the average length of the global interconnects in a target architecture is known, it is possible to extract the conversion cost (i.e., delay and power) requirement for OIs. As an example, the OI conversion requirements for an interconnect length equal to the ITRS projected chip edge length of 17.6 mm for both polymer-core and silicon-core waveguides are shown in Fig. 4. In this figure, the EI delay is plotted as a function of distance. The optical waveguide delay is then projected back from the 17.6-mm EI delay to the *y*-axis as indicated by the arrow. The *y*-intercept of the optical waveguide delay curve indicates the maximum allowed conversion delay τ in the chip edge length OI. As illustrated in Fig. 4, the combined transmitter and receiver delay should be lower than 280–370 ps for polymer waveguides and 180–270 ps for silicon waveguides.

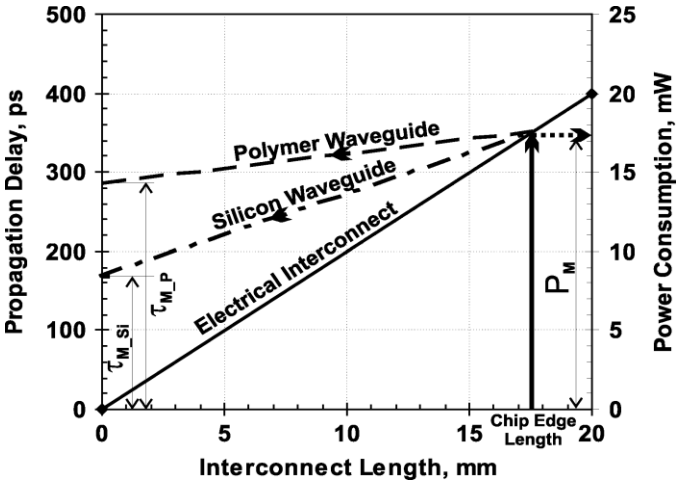

Fig. 4. Maximum conversion cost for an on-chip OI. Left axis shows the signal propagation delay and right axis the power consumption in the interconnect. τM P is the maximum allowed electrical–optical–electrical conversion delay in the chip edge length polymer waveguide OI, τM Si is the maximum allowed conversion delay in the chip edge length silicon waveguide OI, and *P*M is the maximum allowed conversion power consumption in the chip edge length OI.

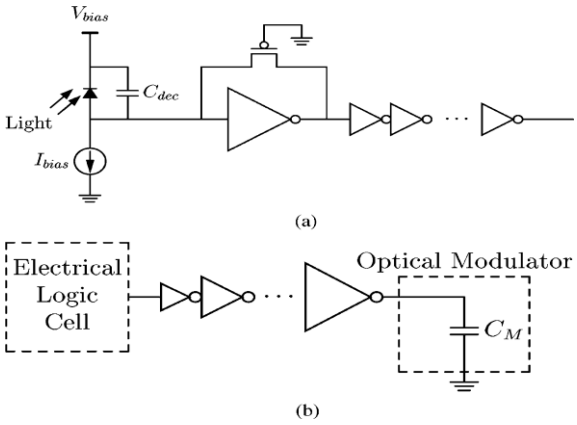

Fig. 5. Circuit schematic of (a) waveguide receiver and (b) modulator driver

Using the second y-axis in a similar way, the total power cons-umption should be less than 17–18 mW for chip-length OI.

The conversion penalty consists of two parts—the transmitter and receiver. The receiver consists of a photo detector that converts light into electricity and receiver circuitry that amplifies and converts the analog electrical signal into a digital voltage signal [see Fig. 5(a)].

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The key issue to be addressed in the design of a photo detector is the tradeoff between detector speed and quantum efficiency (or sensitivity of the detector). Interdigitated metal–semiconductor–metal (MSM) receivers have attracted attention due to the fast response and excellent quantum efficiency. Recently, there have been a number of reports on high-speed, low-power interdigitated MSM Ge and SiGe photo detectors operating at telecommunication wavelengths [9], [10].As compared to other Si-based photonic components, the reported perfor-mances already satisfy the requirements of on-chip global

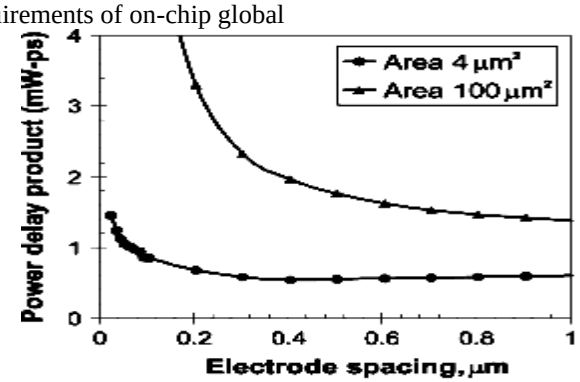

Fig. 6.Combined power-delay product for interdigitated MSM photodetector and receiver circuits.

interconnect. By optimizing the interdigitated electrode width, the detector bandwidth can be further increased.

The power and delay product (PDP) is routinely used in the technology design process to evaluate circuit performance. Simulations of the PDP of a Ge MSM detector and receiver circuits are illustrated in Fig. 6. Note that there exists an electrode spacing at which the PDP is lowest. This minimum is a compromise between the longer carrier transit time for larger electrode spacings and the increase in the *RC* impedance for small electrode spacings [21]. Also note that the optimum electrode spacing differs, depending upon the detector size. Both the delay and power consumption can be further reduced by decreasing the size of the detector.

The current state of electro-optic transmitters suitable for intrachip OIs is much less advanced. A transmitter consists of a modulator and driver circuits [see Fig. 5(b)]. A series of tapered inverters is used to drive the modulator [12]. Although significant progress has recently been made [7], [8] in silicon based modulators, these modulators do not currently provide the necessary performance to replace EIs. The main parameter for a modulator is an effective refractive index change Δn_{eff} in the active area, or the phase shifter of the modulator. The higherΔn_{eff} , the more compact the modulator, thereby reducing the propagation delay and power consumption. The two main types of modulators are Mach–Zehnder interferometer-based modulators [7] and microresonator-based modulators [8] (see Fig. 7). For modulators with a Mach–Zehnder interferometer structure, Δn_{eff} determines the length of the phase shifters. For microresonator-based modulators, Δn_{eff} determines the value of the resonance wavelength shift and therefore the extinction ratio, or the on/off contrast.

The dependence of the PDP of the modulator and driver circuits on Δn_{eff} for both Mach–Zehnder interferometers- and microresonator-based modulators with driver circuits is shown in Fig. 8. The modulator load is modeled as a simple capacitor and is assumed to scale linearly with the modulator length at the rate of 1.7 pF/mm. Both the length and delay of a Mach–Zehnder modulator are determined by Δn_{eff} . The length of the active region of a microresonator-based modulator is assumed to be constant; therefore, Δn_{eff} only affects the delay.

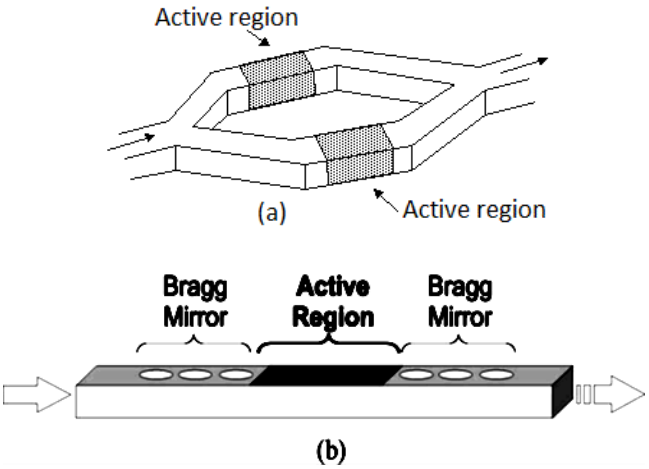

Fig. 7. Schematic of a mach-zehnder modulator. (a) Interfero-meter based (b) microresonator based.

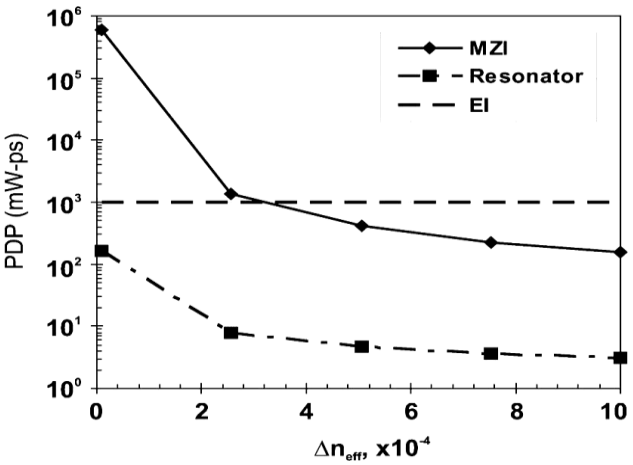

Fig. 8. Combined power-delay product of transmitter as a function of Δ*n*eff for the 90 nm technology node. Delay and power consumption of both the modulator and receiver circuits are included in the PDP. A series of optimized tapered inverters [15] is used to drive the modulator. The transimpedance amplifier is used to amplify the photocurrent from the detector. Additional minimum-sized inverters are used to amplify the signal to a digital level. For comparison, the dashed line describes the PDP of a 10-mm-long EI. The structure of a microresonator-based modulator is a generalized Fabry–Perot cavity, with the dimensions of the phase shifter limited by the cavity size. The PDP model is valid for any resonant structure, including two-dimensional (2-D) photonic bandgap microcavities and microring resonators as long as the active region is no larger than the cavity size. The PDP of a delay-optimized EI for a 90 nm technology node is also shown for comparison. Fig. 8 shows that the PDP of a microresonator-based modulator is significantly better than that of a Mach–Zehnder interferometer.

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Microresonator-based modulators can effectively fold the active device region, thereby significantly reducing the power consumption and the driver delay. Resonant structures should easily exceed EIs in terms of the PDP, as shown in Fig. 8. While microresonators are superior to Mach–Zehnder interferometers, there are two problems that should be solved before resonant-based structures can be successfully used for intrachip applications. First, microresonators have a low fabrication tolerance. This factor may become less important as lithographic techniques improve. Second, unlike Mach–Zehnder interferometers, microresonators are susceptible to temperature fluctuations due to the dn/dT of the cavity material. While the introduction of OIs may help manage the thermal budget in multi-core processor architectures [13], OIs remain susceptible to temperature variations. Either an active or passive optical control method similar to that published in [22] is required to maintain stable device operation.

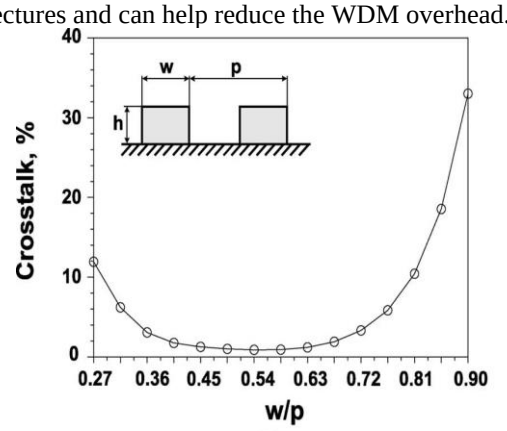
B. Bandwidth Density Comparison

Bandwidth density is a metric that characterizes information throughput through a unit cross section of an interconnect. Generally, it is defined by the pitch of the electrical wires in EIs or optical waveguides in OIs. Optical waveguides can be reliably compared to EIs, since the size and propagation delay can be straightforwardly determined. Each type of optical waveguide produces a different propagation delay and bandwidth density, both of which are determined by the waveguide geometry and the index contrast between thewaveguide core and cladding. The minimum pitch between two adjacent waveguides is determined by the crosstalk considerations. For a particular waveguide material, an optimum ratio exists between the waveguide width w and pitch p. With a fixed pitch, if a waveguide is too wide, the crosstalk is high due to the proximity between the sides of adjacent waveguides. If the waveguide is too narrow, the optical mode becomes less confined, causing a higher crosstalk due to a larger overlap between adjacent optical modes. This tradeoff for polymer waveguides is illustrated in Fig. 9(a).

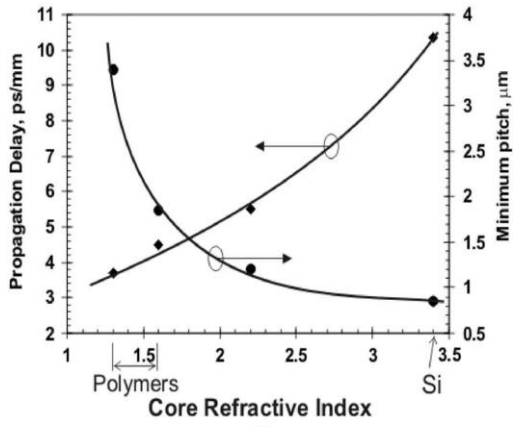
To estimate the maximum bandwidth density, the minimum waveguide pitch is determined by setting the crosstalk limit to 20% in a 10-mm long interconnect. The optical signal propagation delay is determined from the n_{eff} of the simulated optical mode. The resulting tradeoff is depicted in Fig. 9(b), where the waveguide delay and minimum pitch are plotted versus the refractive index of the core. A general trend is that a high-index core offers a smaller waveguide pitch, while a low-index core offers a lower propagation delay. This graph can be used to evaluate the two essential interconnect requirements—propagation delay and bandwidth density.

As illustrated in Fig. 10, optical waveguides should be spaced approximately 0.5–3 μm from each other to avoid significant crosstalk. In contrast, a delay-optimized pitch for electrical wires is around five to seven node sizes, providing a significant advantage in bandwidth density. A comparison of the bandwidth density for delay-optimized EIs and optical waveguides is illustrated in Fig. 10. The increase in optical bandwidth density shown in the graph is due solely to the higher bit rate through the waveguides with a fixed pitch. EIs can also exploit more efficient repeaters, resulting in a higher growth in bandwidth density. Therefore, a single wavelength optical link is inferior to a delay-optimized electrical wire in terms of bandwidth density.

A viable solution to the bandwidth density problem in OIs is to use wavelength division multiplexing (WDM) to enhance the OI bandwidth density. The number of WDM channels required to match the EI bandwidth density for both SOI and polymer waveguides is shown in Fig. 11. Two types of tradeoffs can be identified from this graph. Polymer-core waveguides require higher WDM to match the bandwidth density but allow for a larger conversion delay overhead. Silicon-core waveguides, however, permit lower WDM but require faster transmitters and receivers. Note that while only a moderate number of WDM channels is required to match the EI bandwidth density, there is an area and delay penalty associated with addition of eachWDM channel. Resonant structures are naturally suited for WDM architectures and can help reduce the WDM overhead.



(a)



(b)

Fig. 9.Optical waveguide analysis. (a) Sketch of the modeled waveguides (inset) and the crosstalk as a function of the *w/p* ratio for a 10-mm polymercore waveguide interconnect. When *w/p* is too small, the crosstalk is high due to a smaller mode confinement, whereas when *w/p* is too large, the crosstalk is high because the waveguide walls are too close. (b) The tradeoff between waveguide density and propagation delay per unit length. The graph is plotted for a 10 l,mm interconnect and a maximum allowed crosstalk of 20%. The height *h* and width *w* of all of the waveguides are set equal. The cladding material is assumed to have a refractive index of 1.1, and the wavelength of light is 1.3 μm. The optimum *w/p* ratio for each data point is determined separately.

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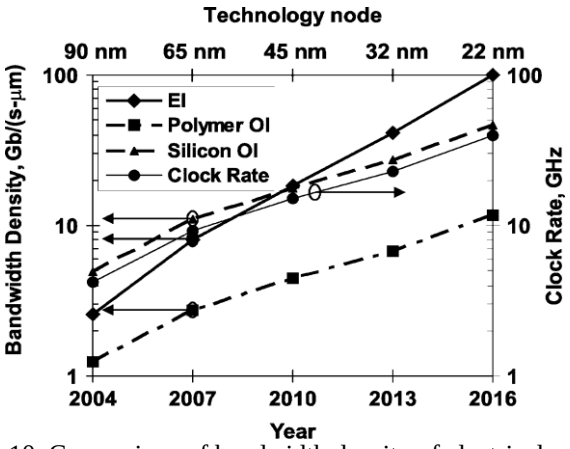

Fig. 10. Comparison of bandwidth density of electrical wires and OIs as a function of year and technology node. For reference, the thin solid line illustrates the ITRS prediction for the clock rate. Bandwidth density is an important metric, defining the information throughput of an interconnect through a unit cross section.

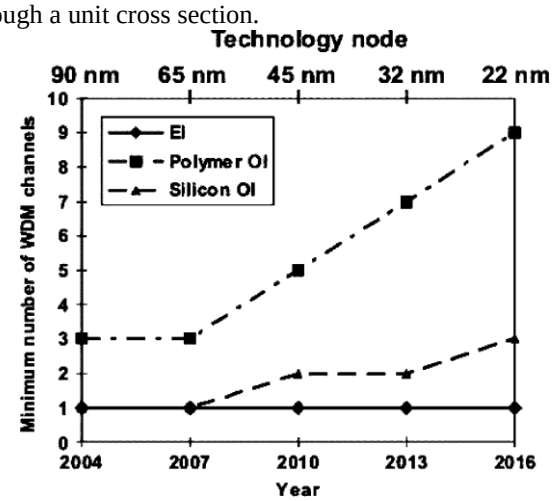

Fig. 11. Number of OI WDM channels required to exceed the EI bandwidth density as a function of year.

V. CONCLUSION AND UPCOMING CHALLENGES

Based on the semiconductor technology roadmap, requirements and critical directions are presented for intrachip OIs. From this discussion, the following requirements should be satisfied for OIs to be competitive with EIs for intrachip global interconnects.

1) The combined transmitter and receiver delays should be lower than 280–370 ps for polymer waveguides and lower than 180–270 ps for silicon waveguides for chip-length global interconnect.
2) The total power consumption should be comparable to that of EI (~18 mW) for chip-length global interconnect.
3) The maximum bandwidth, or bit rate, should exceed the ITRS prediction for the clock rate.
4) Since the bandwidth density is expected to growfor EIs, an increasing number ofWDMchannels is necessary for OIs to exceed EI performance, up to nine in the case of lowindex waveguides and three for high-index waveguides by the year 2016.
5) General CMOS requirements, most significantly technology compatibility and temperature stability, should be satisfied.

This discussion has identified the primary challenges for intrachip OIs to successfully compete with EIs. First, the size, delay, and power consumption of silicon-compatible modulators should be significantly reduced before any state-of-the-art modulator can be considered for on-chip applications. Second, the introduction of WDM requires the development of ultra compact integrated wavelength-selective components and efficient broadband external lasers. Finally, passive or active temperature drift compensation is necessary to ensure reliable operation of OIs.

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