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Reconfigurable Down Sampling Channelizer for SDR Receiver Using FPGA

Majid S. Naghmash, Hazim Salah Abdulsatar, Tahseen Flaih Hasan

Abstract*—This paper presents, the design and implementation of reconfigurable down sampling the IF band frequency to baseband in Software Defined Radio (SDR) receiver. To enhance both the integration and adaptation of multiple communication standards like GSM, CDMA and WCDM systems, the selection of channel in SDR technology require to achieve relaxing on chip at baseband. The wireless and mobile systems classically utilize a channelizer to extract the desired band for more processing in baseband. Down conversion in frequency domain requires less computation and complexity to provide the idea of minimum power consumption as current user demand. In the low power design and efficient FPGA area implementation, the cascaded digital filter structure is required to convene multi standards specifications in wide and narrow band systems. Many type of digital filter has been decomposition to implement this filter as well as a lot of software from Mathworks and Xilinx is used. A number of experiments and investigation are given to estimate the results of FPGA design for filter structure. The nonappearance of error in the design steps shows an important improvements in the filter implementation results to enhance the conventional design.

***Index Terms*— Reconfigurable filter, Down Sampling, SDR Receiver, FPGA.**

I. INTRODUCTION

The technology of Software Defined Radio (SDR) offer software manage for diversity of modulation techniques in wide or narrowband process [1]. In addition, SDR is provide flexibility and permit to multiple communication protocols to animatedly perform on the same hardware, thus dropping the cost. The filtering, demodulation and decoding processes in the receivers could be reconfigured adaptively at run time which will reduce the cost and power consumption for end user [2]. The analogue to digital converter (A/D) in SDR receivers is moved as closed as possible to antenna and all functions are realized by digital signal processing (DSP) to offer small size device as well as low power. The narrow and wide band architectures in wireless communications systems are always suffer from interfere phenomena due to nearest channel. The narrowband systems practically support only a single carrier channel while wideband will support multiple channel. Hence, the reconfiguration idea in the IF band required to be efficient in term of selectivity and adaptively to overcome the interference [3]. In the cellular handset and tactical communications systems, the narrowband architectures is presents and the interference rejection inherently founded [4].

Thus, the interference in the adjacent band rejection is required to overcome and process carefully as illustrated in Figure 1.

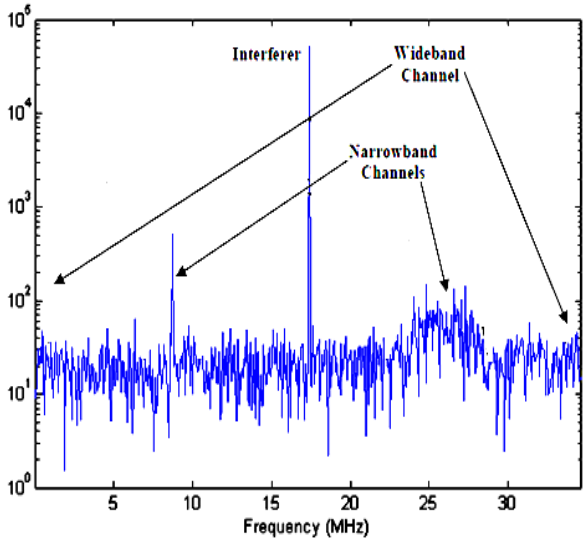

Figure 1: Channel interferer in Narrowband and wideband frequency.

Therefore, at any time, many simultaneous carrier channel might be activated in wideband architectures like satellite communications and cellular base station making big problems and this phenomena required to break in and process properly. Hence, the channelization in wideband receiver systems is a key elements which is used to isolate the independent communication channel restricted in the wideband signals [5]. The theory of decimation or down sampling process is to reduce the sample rate of incoming signal after D/A converter. The down sampling theory could be expressed as:

$$y(n) = x(Mn), \qquad n = \pm\infty \tag{1}$$

$$Y(e^{j\omega}) = \frac{1}{M}\sum_{k=0}^{M-1} X\left(e^{j(\omega-2\pi k)/M}\right) \tag{2}$$

Where $x(n)$ is the decimator input signals, M is decimation factor, $y(n)$ is the decimator output signal

In frequency domain after the signal is moved from time domain by A/D converter, the process could be expressed as:

$$\cos(\omega_c t) = \frac{1}{2}X(\omega - \omega_c) + \frac{1}{2}X(\omega + \omega_c) \tag{3}$$

$$\sin(\omega_c t) = \frac{1}{2}X(\omega - \omega_c) + \frac{1}{2}X(\omega + \omega_c) \tag{4}$$

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Then the decimator output has kept all the data in the desired frequency band with down convert to baseband to permit the sample frequency to be reduced. The advantage of this process is to simplify the additional processing and FPGA functioning due to lowest clock frequency , therefore allowing more processing to be fitted into hardware implementation. Additionally, the low clock frequency could reduce the power required in FPGA.

Numerous researchers are investigate in this field which propose efficient implementation of multi-stage digital filter bank [6-9]. An independent channel filter approach is proposed by [10] which complexity is directly proportional with number of received channels. Consequently, this approach is efficient if the number of channels is small. Capable implementation of channelized filter by using discrete Fourier transform filter bank is projected in [11-12]. Based on combination of polyphase filter design modules, a hybrid filter bank has been targeted by [13] with less computation corresponding to conventional design associated by some limitations. Efficient sample rate converter with two stages filter bank and multi-mode channelizer has been proposed by [14]. In this paper, a novel reconfigurable channelization techniques utilize in wideband design are examine and investigated to produce software channel filter capable to isolate triple channel in most popular protocols systems. The triple - mode channel receiver shown in Figure 2 is investigated properly.

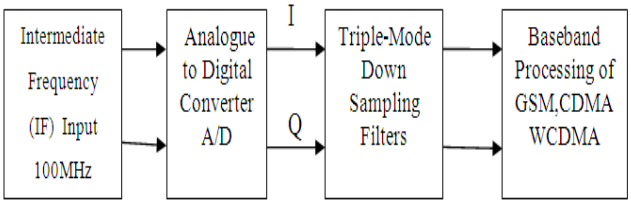

Figure 2: Programmable IF channelize receiver

II. FILTER ARCHITECTURE

To describe and realize the software radio receiver, a capable concept of triple mode down sampling filter for IF band is proposed as illustrated in Figure 3. The filtering process in IF band is the more important stage in signal processing due to size occupied and power consumption spent in the multiplication process. A digital filter like finite impulse response (FIR) required to implement in more than one stage to decrease the circuit complexity and multiplication. Hence, the triple mode down sampling filter could be design to provide the GSM, WCDMA, and CDMA system requirements in the passband, stopband and adjacent band rejection. Consequently, these modes contribute to a common IF front end and could be switched to each other by software design. The bandwidth of 5MHz centered at 100MHz IF signal which contain WCDMA, GSM and CDMA channels. The sample rates selected to be 30.72MHz for three mode. The specifications of three mode is illustrated in Table 1.

Table 1: GSM, CDMA2000 and WCDMA requirements

Parameters	WCDMA	GSM	CDMA
Bit Rate	3.84Mcps	270.833Kbps	1.2288Mbps
Carrier Spacing	5MHz	200kHz	3.75MHz
Chip Rate	4.096MHz	2.5MHz	3.6864MHz
IF Frequency	61.44MHz	69.333284MHz	64.44MHz

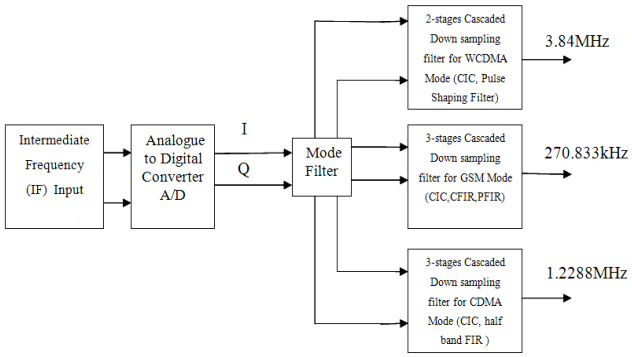

Figure 3: Proposed Filter architecture

Subsequently, the preferred channels will be removed from 5MHz wideband signal by filter realization. The reconfigure ability of channelizer have to talented the same filter hardware for new communication standard with less reconfiguration overhead instead of employing separate filter for each standard. In the conventional filter, the reconfigure ability is achieved by switching between three filters which is not an proficient advance. The reconfigure ability in the filter have to achieved by reconfiguring the same prototype filter to process the signal of new communication standard with less possible overhead.

A. GSM Mode

For GSM processing, the channel bandwidth of 200kHz could be extracted from 5MHz received signal and down samples to the original sample rate of 270.833 Kbps by using decomposition of three stages filter. The first stage in this decomposition is the Cascaded Integrated Comb (CIC) filter with down sampled factor of 64 to introduce 270.833kHz. The GSM requirement will satisfy by adding further filtering stage such as Compensating Finite Impulse Response (CFIR) to attenuate the block signal at 200kHz. Finely, an Programmable Finite Impulse Response (PFIR) in order to shape the GSM mask frequency. The filter structure shown in Figure 4 represent the GSM mode down sampling realization. The GSM spectrum requirement is achieved as illustrated in Figure 5.

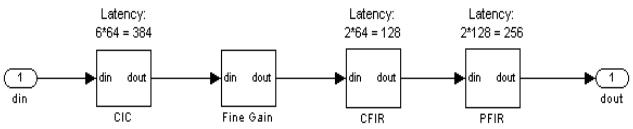

Figure 4: GSM mode down sampling filter

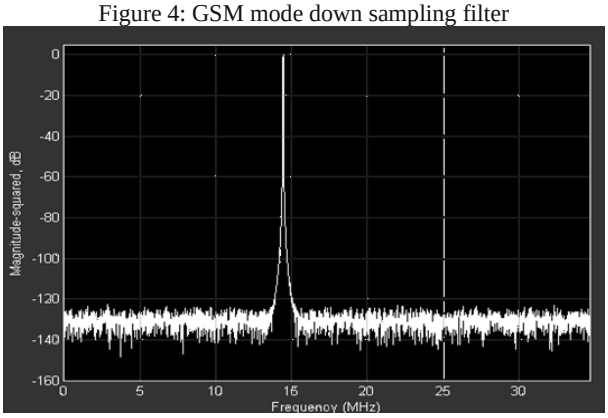

Figure 5: GSM spectrum produce by proposed filter

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B. WCDMA Mode

In WCDMA mode, the filter structure consist of three half band FIR filter is used to decrease the data rate from 4.096MHz down sampled to 3.84Mcps. The WCDMA requirements could be satisfy by using Equiripple half band FIR filter with 10, 18 and 94 filter order for first, second and third stage respectively as shown in Figure 6. The WCDMA spectrum requirement is achieved as illustrated in Figure 7.

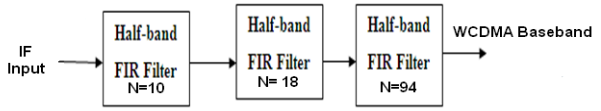

Figure 6: WCDMA Mode Filter structure

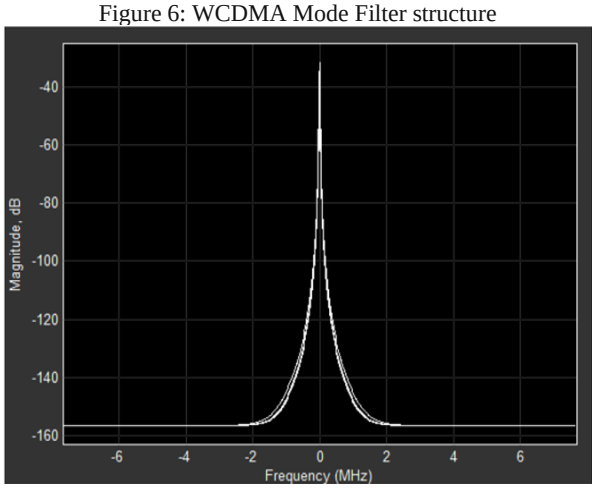

Figure 7: WCDMA spectrum produce by proposed filter

c. CDMA Mode

To extract the 1.25 MHz from 5MHz bandwidth which represents the baseband of CDMA system, an CIC decimator with filter order of 5 and down sampling rate of 25 is used as first stage in the filter structure. The second stage is a half band filter with 25 filter order is used to shape the system requirements and further down sampled filtering using MAC FIR filter decomposition. The filter structure is illustrated in Figure 8 while the filter response which satisfy the CDMA system is shown in Figure 9.

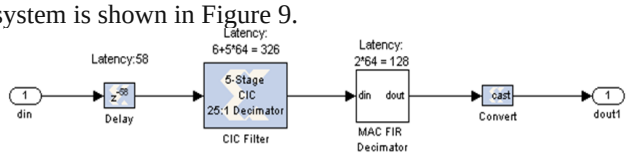

Figure 8: CDMA Mode filter structure

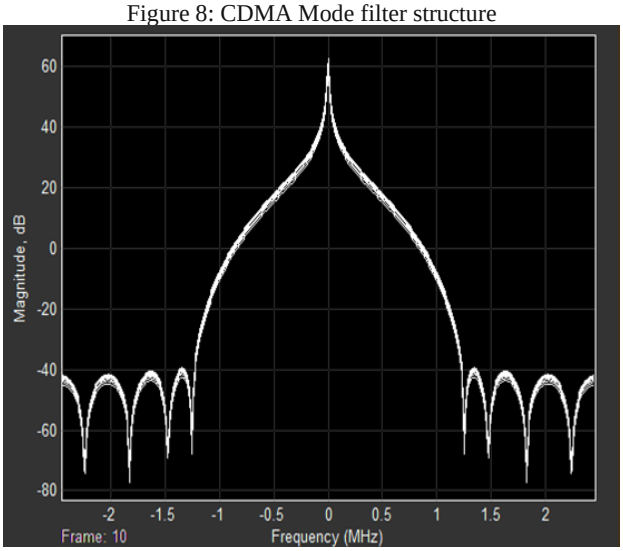

Figure 9: CDMA Mode spectrum response of proposed filter

III. HARDEWARE IMPLEMENTATION

A. Multi-MAC Decomposition

The multi-MAC (Multiply-Accumulate) decomposition based FIR utilizing has been used to introduce the computational efficient implementation of proposed filter as shown in Figure 16. The implementation of single multi-MAC is extensible to achieve higher performance, more channels and high sample rate.

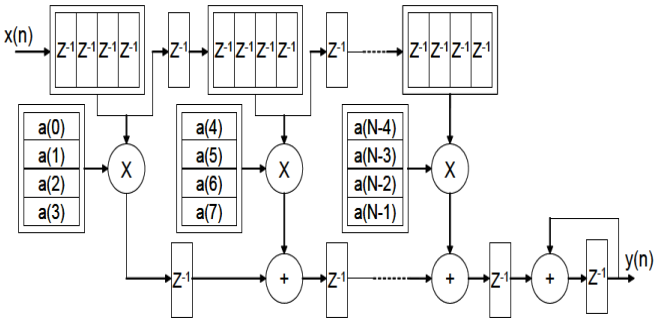

Figure 16: Multi –MAC Implementation decomposition Design

The required multipliers to implement a proposed decimation filter will be determined y calculating the number of necessary multiplies to execute the computation which divided by the number of clocks obtainable to process any input sample. The in hand clock cycle value is forever rounded down and the multiplications numbers rounded up to the nearest integer. However there is non-zero remained , thus, some of the MAC engines calculate fewer coefficients than others. By using multi-MAC decompositions, the core will generate an implementation that meet the defined performance required based on the systems clock rate. In this case, the core will insert one or more multipliers to meet the overall throughput requirements. The FIR compliers consist two MAC architectures to implement the systolic and transpose filter structure.

B. FPGA Design flow

The design flow of proposed decimation filter is illustrated in Figure 17. The signal is down sampled before filtering which reduce the filter coefficients number necessary to implements the preferred filter resulting in speed improvement and power consumption. The whole decimator design is synthesized to create the Verilog Netlist using the output options under System Generator token GUI interface and the results of the performance of map, place and route task done, by using the project navigator tool to implement the design in real time. After the HDL code generation of the Netlist module, the Integrated Software Environment (ISE) software used its own Xilinx Software Technology (XST) environment to convert the HDL code into FPGA based optimized Netlist Electronic Design Interchange Format File (EDIF) and User Constraint File (UCF), and this process called synthesis. In the translate step, the EDIF file will merged with UCF to produce Native Generic Database File (NGD). The logic defined by NGD file will mapped into FPGA elements by so called NCD file (Native Circuit Description). Finally, the NCD file has place and route to FPGA with time constraint to generate PAR report (Place and Rout Report) from ISE project navigator and produce the Bit stream into FPGA via JTAG programs.

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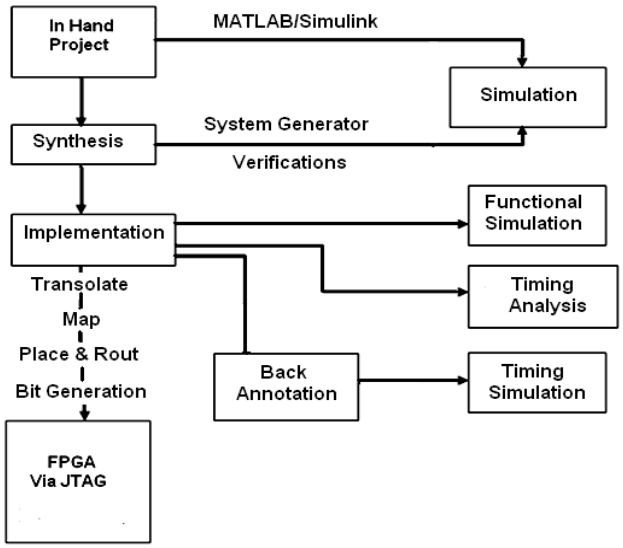

Figure 17: FPGA Design Flow

C. Fixed Point Design

Before FPGA designs steps, the fixed point values of proposed module has been designed and simulated using system generator block set from Xilinx and this module should verify with MATLAB simulation for accuracy as shown in Figure 18. The input and output gate way in system generator is used to change the floating point arithmetic values for all parameter to fixed point arithmetic values. Therefore, a low quantization errors will happen nevertheless it's still acceptable.

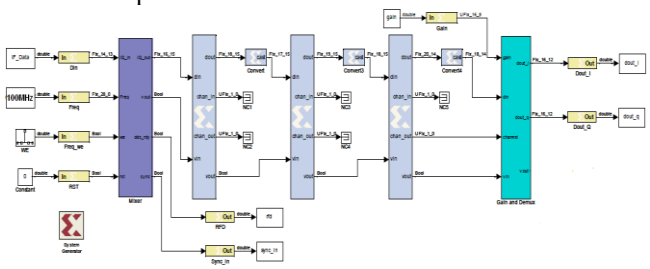

Figure 18: Filter implementation using System Generator

In the Netlist directory specified in system generator token GUI, the ISE project report file is generated along with the design timing constraints. The HDL code has been developed and synthesis on Xilinx Vertix-4 using Integrated software environments (ISE). The maximum frequency of the proposed filter is 100MHz. The project status of ISE software generates the decimation utilizing summary as shown in Table 3. The table lists the total number of slices and look-up tables (LUTs) used in this design. In each slice they are two LUTs and two FFs, during the PAR, the ISE software put all necessary LUTs close to each other for minimum propagation of data, for that some LUT inside slice not used and in some slice only FFs is used without LUT so, the number of LUTs cannot be calculated manually, therefore the LUTs could be less or more than Slices depend on software optimization. The device utilization summary generated by ISE software represents the available logic elements in FPGA and logic elements used by the in hand project been designed. The used logic elements to the available logic elements could be determined by below formula.

$$\text{utilization\%} = \frac{\text{used logic elements}}{\text{available logic elements}} X\ 100 \quad (5)$$

Then, the utilization number of slices flip flop, 4-input LUTs and bonded IOBs could be calculated and compared with other designs and conventional model as illustrated in Table 3.

Utilized number of Slice Flip Flop = (2451/30720) x 100 = 8% (6)

Utilized number 4-input LUTs = (921/30720) x 100 = 4% (7)

Utilized number of occupied Slices = (600/15360) x 100 = 4% (8)

Utilized number of bonded IOBs = (30/448) x 100 = 6% (9)

Comparing with conventional design, the proposed filter appear more efficient and less FPGA area and this will reduce the power consumption. Consequently, reduce the computation and complexity of the circuit to offer more flexibility in the user demand. The memory size of the filter is increase as the complexity decrease. An comparison of slices and LUTs is illustrated in Table 4.

Table 3: decimation project device utilization summary

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	2451	30,720	8%	
Number of 4 input LUTs	921	30,720	4%	
Logic Distribution				
Number of occupied Slices	600	15,360	4%	
Number of Slices containing only related logic	600	661	100%	
Number of Slices containing unrelated logic	0	661	0%	
Total Number of 4 input LUTs	755	30,720	2%	
Number used as logic	430			
Number used as a route-thru	8			
Number used as Shift registers	218			
Number of bonded IOBs	30	448	6%	
Number of BUFG/BUFGCTRLs	2	32	3%	
Number used as BUFGs	2			
Number used as BUFGCTRLs	0			
Number of FIFO16/RAMB16s	2	192	1%	
Number used as FIFO16s	0			
Number used as RAMB16s	2			
Number of DSP48s	2	192	1%	
Total equivalent gate count for design	158,984			
Additional JTAG gate count for IOBs	1,488			

Table 4: FPGA Slices and LUTs comparison

Resource	Utilization % Santhosh Y. N., et al IEEE 2010	Utilization% Rajesh & Pattnaik 2013	Utilization% Proposed Filter 2013
Slices	30	11	8
LUTs	20	7	4

IV. CONCLUSION

The hardware proficient techniques has been used to implement the reconfigurable down sampling filter for wireless systems based SDR knowledge is presented in this paper. The Equiripple FIR digital filter algorithms and multistage half band FIR filter decomposition is proposed for less filter length and enhanced computational complexity to improved the filter rate.

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The Multiply-Accumulate (MAC) decomposition based FIR architecture is used in hardware implementation to optimize the speed and area together which resulting in power consumption reduction. The FPGA vertix-4 and DSP48E blocks from Xilinx are used which contains multiplierless MAC filter. The proposed down sampling filter could be used at maximum frequency of 100MHz with minimum power and FPGA area efficient. Consequently, the implementation of down ampling filter on specific target FPGA Vertix-4 resulting in cost effective solution for SDR technology which is capable to maintain the current and future generation of wireless and mobile systems.

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