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Design of Op-amp, Comparator and D Flip-Flop for Fifth Order Continuous-Time Sigma-Delta Modulator

Sunita Arvind Rathod, Siva Yellampalli

Abstract*—This paper explains the design of two stage operational amplifier, single bit comparator and D flip- flop best suited for the fifth order continuous-time sigma-delta modulator. A fifth order continuous time sigma delta modulator is chosen for 40MHz Signal Bandwidth with an nyquist frequency of 150MHz. Two stage opamp is used to provide the high gain to the modulator. A single quantizer is used to maintain linearity in the modulator. D flip-flop is used for the sampling of the analog signal with the clock frequency of 300MHz. All the three components are designed and implemented in 180nm CMOS technology

***Index Terms*— Operational-amplifier, Comparator, D flip-flop**

I. INTRODUCTION

Mixed signal circuits are removing the gap between analog and digital circuits by reducing the size of system and by increasing speed of operation with less power dissipation and more design flexibility. ADCs are the core components of mixed signal circuits. Sigma delta modulator is one of the attractive mixed signal systems, which has gained importance because of the compatibility with VLSI technology and monolithic integration of both the analog and digital sections on single die [1]. In sigma delta modulation, sigma signifies a summing operation and delta signifies the process of quantization of the signal from sample to sample in spite of the absolute value of the signal at each sample [2]. In this paper components of fifth order continuous time sigma delta modulator are designed. First two stage op-amp is designed for gain, second comparator is designed to provide high gain and high speed and D flip-flop is used for the sampling the analog signal. The frequency for D flip-flop chosen will be in the mega-hertz range.

II. DESIGN OF TWO STAGE OPAMP

Two-stage circuit is the most popular approach for both bipolar and CMOS op-amps, where complementary both n-type and p-type devices are available. Properly designed, two-stage op-amp have very performance close to more modern designs and is more suitable when resistive loads needs to be driven. The two stage op-amp is shown in the Fig.1,The first gain stage is a differential input single ended output stage and the second is gain stage normally a common source gain stage with an active load.

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*****Correspondence Author(s)
Ms. Sunita Arvind Rathod, Dept. of VLSI Design and Embedded Systems, VTU Extension Center, UTL Technologies Ltd, Bangalore, India.
Dr. Siva Yellampalli, Dept. of Electronics and Communication Engineering, VTU Extension Center, UTL Technologies Ltd, Bangalore, India.

Capacitor Cc ensures stability when the op-amp is used with feedback. Because of presence of Cc in between the input and the output of the high gain second stage, it is called a Miller capacitance. The first stage has a p-channel differential input pair with an n-channel current mirror active load [3].

1) First assume *VSG*4 = *VSG*6. This will provide "proper mirroring" in the M3-M4. The drain and gate of M4 transistor are at the same voltage potential so M4 is "guaranteed" in saturation.

2) *If VSG*4 = *VSG*6, then *I*6 = (S6/S4)(I4).

3) *I*7 = (*S*7/*S*5), *I*5 = (□*S*7/*S*5)(2*I*4).

4) *I*6 = *I*7 => (S6/S4) = (2S7/S5) is called the "balance conditions".

5) When the balance conditions are satisfied, then *VDG*4 = 0 and M4 is saturated.

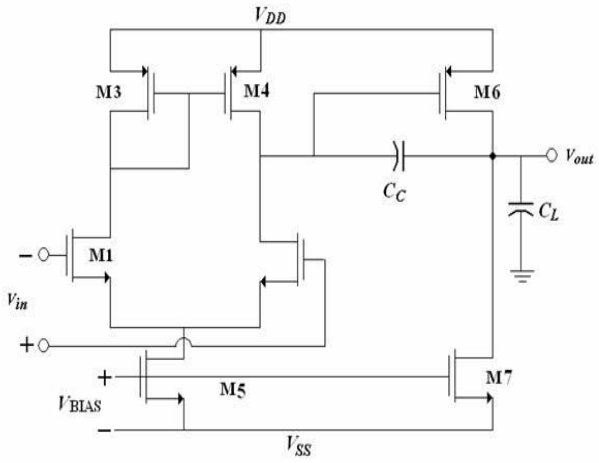

Fig.1 Two Stage Op-Amp [3]

The two stage op-amp is designed with the following specifications:

Table 1. op-amp design specifications

PARAMETER	VALUE
Supply Voltages	Vdd=+2.5V, Vss=-2.5V
Gain	> 5000V/V
Gain Bandwidth	5MHz
Slew Rate	> 10 V/µS
ICMR	-1 to 2V
Output Range	±2 V
Pdiss	≤ 2 Mw

Step 1. at phase margin of 60°, the minimum value for *Cc* is given by

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$$C_C > \left(\frac{2.2\,C_L}{10}\right) \quad (1)$$

$$C_C > \left(\frac{2.2 \times 10pF}{10}\right) = 2.2\text{pF} \simeq 3\text{pF} \quad (2)$$

Step 2. The minimum value of the "tail current" (*I*5) is given by

$$I_5 = SR \times C_C \quad (3)$$

$$I_5 = 3 \times 10^{-12} \times 10 \times 10^6 = 30\mu A \quad (4)$$

Step 3. (W/L) ratio for transistor M3 (*S*3) from the maximum input voltage specifications is given by

$$S_3 = \left(\frac{W}{L}\right)3 = \frac{I_5}{(K_3')(V_{DD} - V_{in(MAX)} - |V_{TO3(MAX)}| + V_{T1(MIN)})^2} \quad (5)$$

$$S_3 = \left(\frac{W}{L}\right)3 = \frac{3 \times 10^{-6}}{(50 \times 10^{-6})(2.5 - 2 - 0.85 + 0.55)^2} = 15 \quad (6)$$

$$\frac{W_3}{L_3} = \frac{W_4}{L_4} = 15 \quad (7)$$

Step 4. (W/L) ratio for transistor M1 (*S*1) and M2 (S2) to achieve the desired *GB* is

$$gm1 = GB \times C_C \quad (8)$$

$$gm1 = 5 \times 10^6 \times 3 \times 10^{-12} \times 3\Pi = 94.25\mu S \quad (9)$$

$$\frac{W_1}{L_1} = \frac{W_2}{L_2} = \frac{gm1^2}{(K_1')(I_5)} = \frac{94.25^2}{2 \times 110 \times 15} = 2.79 \simeq 3.0 \quad (10)$$

Step 5. (W/L) ratio for transistor M5 (*S*5) from the minimum input voltage is calculated by first calculating *VDS*5(sat)

$$V_{DS5} = V_{in(MIN)} - V_{Ss} - \left(\frac{I_5}{\beta 1}\right)^{1/2} - V_{T1(MAX)} \quad (11)$$

$$V_{DS5} = -1 - 2.5 - \left(\frac{30 \times 10^{-6}}{110 \times 10^{-6} \times 3}\right)^{\frac{1}{2}} - 0.85 = 0.35V \quad (12)$$

$$\frac{W_5}{L_5} = \frac{2I_5}{(K_5')(V_{DS5})^2} = \frac{2(30 \times 10^{-6})}{(110 \times 10^{-6})(0.35)^2} = 4.49 \simeq 4.5 \quad (13)$$

Step 6. (W/L) ratio for transistor M6 (*S*6) is calculated in this step with assumption of *VSG*4 = *VSG*6.

$$gm6 = (2.2)(gm2)\left(\frac{C_L}{C_C}\right) \quad (14)$$

$$gm6 \geq (10)(94.25 \times 10^{-6}) \geq 942.5\mu S \quad (15)$$

$$S_6 = \frac{W_6}{L_6} = S_4 \frac{gm6}{gm4} = \frac{(15)(942.5\mu)}{150\mu} = 94.25 \simeq 94 \quad (16)$$

Step 7. Current *I*6 is given by

$$I_6 = \frac{(gm6)^2}{(2)(K_6')(\frac{W_6}{L_6})} \quad (17)$$

$$I_6 = \frac{(942.5\mu)^2}{(2)(50 \times 10^{-6})(94)} = 94.5\mu A \simeq 95\mu A \quad (18)$$

Step 8. (W/L) ratio for transistor M7 (*S*7) is calculated by using current ratios of *I*5 and *I*6.

$$S7 = (I6/I5)\,S5 \quad (19)$$

$$S_7 = \frac{W_7}{L_7} = S_5 \frac{I_6}{I_5} = \frac{(4.5)(95\mu)}{(30 \times 10^{-6})} = 14.25 \simeq 14 \quad (20)$$

Step 9. Gain and Power dissipation is given by

$$A_V = \frac{(2)(gm2)(gm6)}{(I_5)(\lambda_2 + \lambda_4)(I_6)(\lambda_6 + \lambda_7)} \quad (21)$$

$$A_V = \frac{(2)(94.25\mu)(942.5\mu)}{(30 \times 10^{-6})(0.04 + 0.05)(95\mu)(0.04 + 0.05)} = 7696 \quad (22)$$

$$Pdiss = (I5 + I6)(VDD + |VSS|) \quad (23)$$

$$Pdiss = (30uA + 95uA)(5V) = 0.625mW \quad (24)$$

Step 10. To meet the gain specification, the currents, *I*5 and *I*6 should be decreased or the W/L ratios of M2 and/or M6 should be increased. If the power dissipation is too high, it can be reduced by reducing *I*5 and *I*6 currents. By reducing the currents values the W/L ratios increased to maintain input and output swings. The transistor version of the two stage CMOS op-amp is shown in the Fig. 2.There are total 7 transistors in the design and using the above design values and standard design equations, the size of each transistor is calculated. The design is implemented in 0.18µm CMOS technology. For each transistor length is taken as 1µm and width is calculated according to the W/L ratio. The summary of W/L ratios for each transistor is given below [4]:

Table 2. Design Summary of Op Amp

	M1	M2	M3	M4	M5	M6	M7
Type	N	N	P	P	N	P	N
W/L	3	3	15	15	4.5	50	14
L(µm)	1	1	1	1	1	1	1

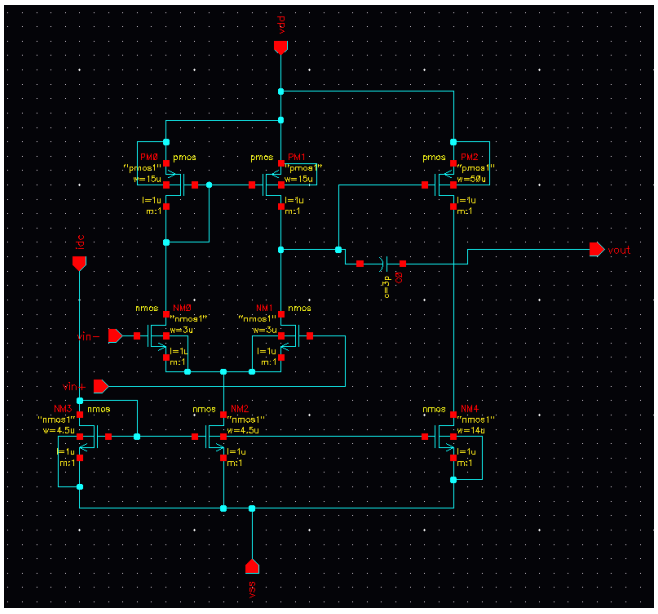

Fig. 2 Schematic of Two-Stage Opamp

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III. COMPARATOR DESIGN

A comparator is a device which compares two inputs i.e. voltages or currents and switches its output to select the larger value. A comparator has binary output i.e. high (1) or (0). Output of the comparator is given by [4] [5]:

$$Vo = \begin{cases} V_{OH} \text{if } V_{in+} - V_{in-} > 0 \\ V_{OL} \text{if } V_{in+} - V_{in-} < 0 \end{cases} \quad (25)$$

In the current paper, a 10mV is an input signal. The power supply range is VDD=2.5V and VSS=-2.5V, i.e. the output swings by 5V (from -2.5V to 2.5V) when the input swing by 10mV (from -5mV to 5mV). The comparator gain is more than or equal to 10,000. The design parameters are shown below.

Table 3. Comparator Design Specifications

PARAMETER	VALUE
Supply Voltages	Vdd=+2.5V,Vss=2.5V
Gain	> 5000V/V
Slew Rate	> 10 V/μS
ICMR	-1 to 2V
Output Range	±2 V

The transistor version of the CMOS comparator implemented with PMOS input drivers and input biasing resistor is as shown in Fig. 3.

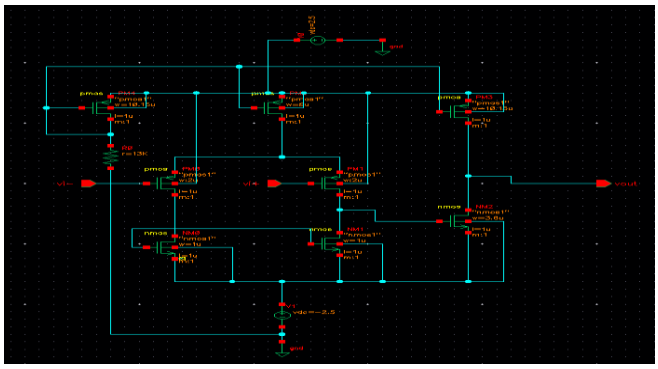

Fig. 3 Schematic of the CMOS Comparator

There are 8 transistors and one resistor in the comparator design and using the above design values and standard design equations the size of each transistor is calculated and are summarized below.

TABLE 4. W/L RATIO OF THE TRANSISTOR OF THE COMPARATOR

	M1	M2	M3	M4	M5	M6	M7	M8
Type	P	P	N	N	P	N	P	P
W/L	2	2	1	1	8	3.6	10.2	10.2
L(μm)	1	1	1	1	1	1	1	1

IV. D FLIP-FLOP DESIGN

In order to clock the Non return-to-zero (NRZ) output of the comparator to a RZ output, a D flip-flop is next block after the comparator. Fig 4, shows the schematic design of the D flip flop [5] [6]. Static D flip-flop is very slow when it has to be used in a MHz frequency range, so to avoid that a TSPC D flip-flop is selected and Fig. 4 shows the schematic of this negative-edge triggered TSPC D flip-flop.

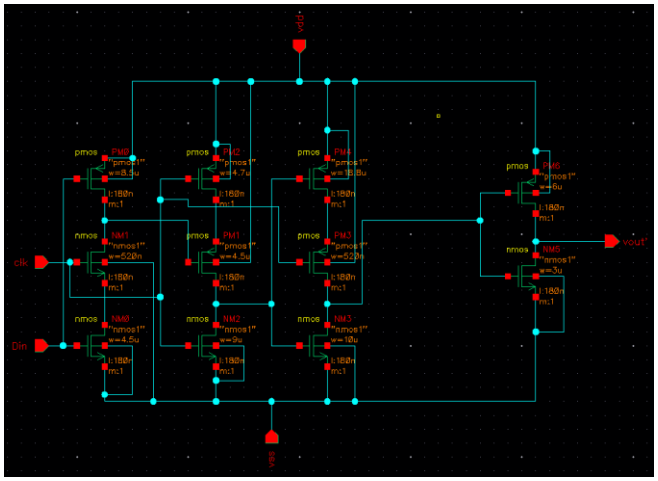

Fig. 4 Schematic of TSPC D Flip-Flop

When the clock signal is high in Fig 5, the transistorM6 and M8 are cut off and the transistors M2 and M4 are turned on. The voltage Vd4 is being pulled to ground and hence forces the transistor M7 cut off. The output therefore is being latched to the previous value. On the other hand, the transistor M1-M3 formed a clock-buffered inverter. When the clock signal is high, the drain voltage of the transistor M2 is the output of this inverter. The output of this inverter connects to the gate of the transistor M5 and the output value of this inverter is being stored in the gate capacitor of the transistor M5. When the clock signal is low in Fig 5, the transistorM2 and M4 are cut off and the transistors M6 and M8 are turned on. The inverter formed by the transistors M1-M3 is being disconnected due to the cut-off of the transistor M2. However, the charges stored in the gate capacitor of the transistor M5 will not be reduced. If the gate voltage of the transistor M5 is zero, the voltage Vd4 will be pulled to positive rail through the transistors M5 and M6. If the gate voltage of the transistor M5 is at positive rail, the voltage Vd4 will remain at ground as it was being pulled to ground when the clock signal is high. The drain voltage of the transistor M5 drives the clock-buffered inverter formed by the transistor M7-M9 and the output of the D flip-flop is the output of this inverter.

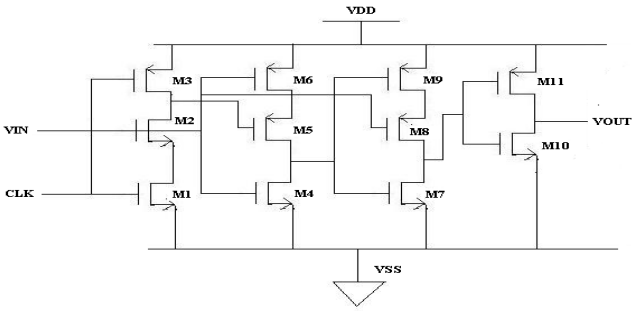

Fig.5 Operations of the TSPC D Flip-Flop [6]

The operation speed of the TSPC D flip-flop is affected by the large RC delay due to the stacked structure. However, the effect of transistor sizing is not evident, because most transistors are drivers and loads concurrently.

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The propagation delay can be reduced by increasing the size of clocked transistors M2, M4, M6 and M8. However, increasing the sizes of those transistors will increase the load capacitance to the clock driver and thus increase the power consumption. The optimize W/L ratios of the transistor of the D flip-flop summarized below.

Table 5. W/L Ratios of the Transistors of the D Flip-Flop

Transistor	W/L ratio
M1,M5	4.5µm/180nm
M2,M8	520nm/180nm
M3	8.5µm/180nm
M4	9µm/180nm
M6	4.7µm/180nm
M7	10µm/180nm
M9	18.8µm/180nm
M10	3µm/180nm
M11	6µm/180nm

V. MEASUREMENT RESULTS

Fig. 6 shows test circuit of the two-stage opamp that is used in the loop filter of the sigma-delta modulator.

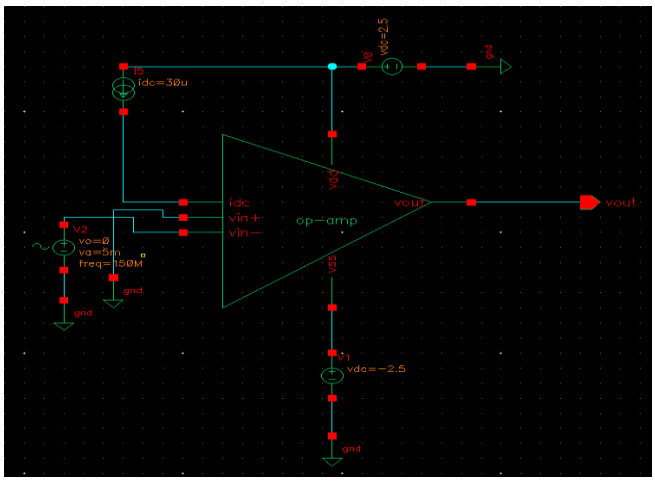

Fig. 6 Test Circuit of Two Stage Opamp

From the transient analysis, we can observe voltage waveform at different nodes for the particular time interval. Fig. 7 shows the transient analysis simulation result of two stage opamp for the time interval 200ns.

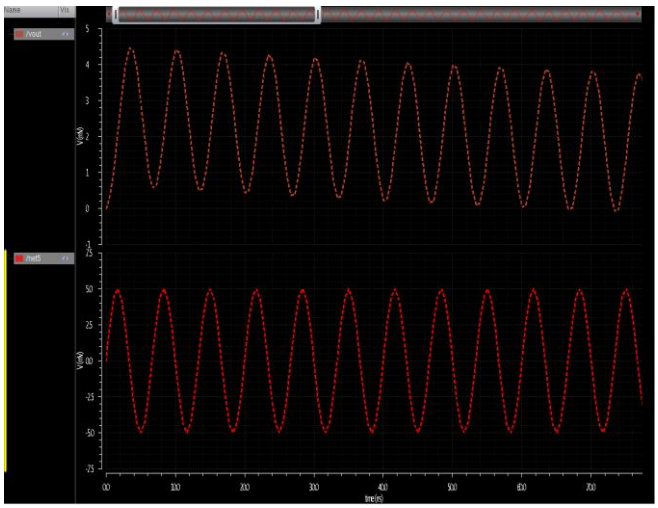

Fig. 7 Cadence Transient Analysis Simulation

From this we calculate the power that consumes to operate for particular power supply. The Fig. 8, shows power measurement waveform of two stage opamp for a power supply 5V. Using calculator in cadence for this waveform the power consumed by two stage opamp is 361.8µW.

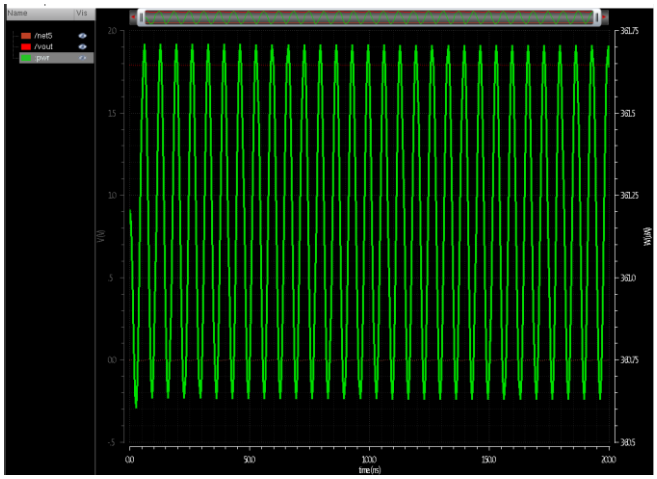

Fig. 8 Power Spectrum of Two Stage Op-Amp

Summary of the simulated results of two stage op-amp is given below.

Table 6. Simulated Result of Two Stage Op-Amp

Parameter	Result Obtained
Operating Frequency	150MHz
Gain	39.785 dB
Phase Margin	56.4
Power	361.8µW

Fig. 9 shows the test circuit of the comparator. 150MHz input frequency and 5V power supply is used for the simulations. The input signal is oversampled wih the clock frequency of 300MHz.

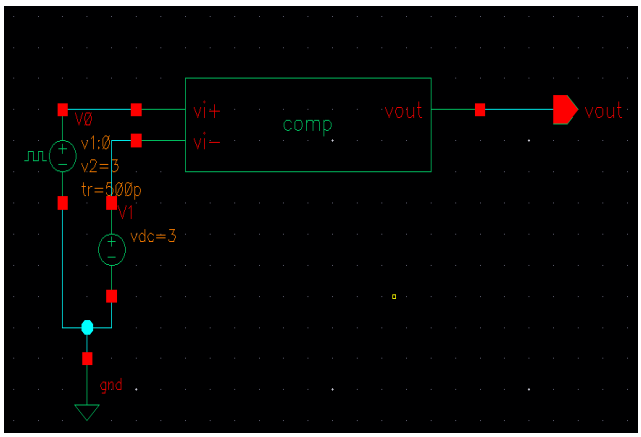

Fig. 9 CMOS Test Circuit of Comparator

Fig. 10 shows the transient analysis simulation result of the comparator for a time interval of 200ns.

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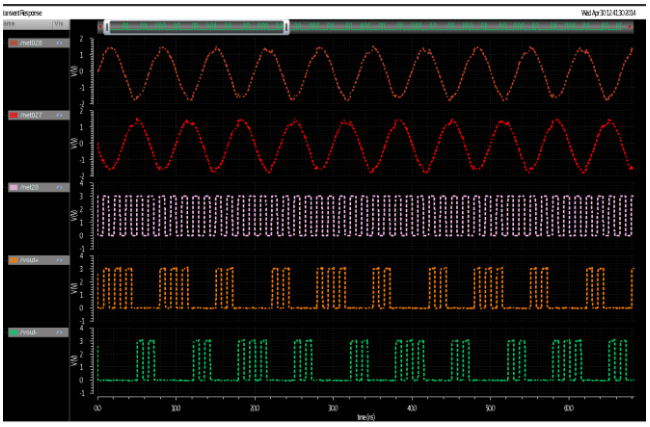

Fig. 10 Transient Analysis of the Comparator

Fig. 11 shows the power measurement waveform of the comparator for a power supply of 5V. Using calculator in cadence for this waveform the power consumed by the comparator is 0.3303mW.

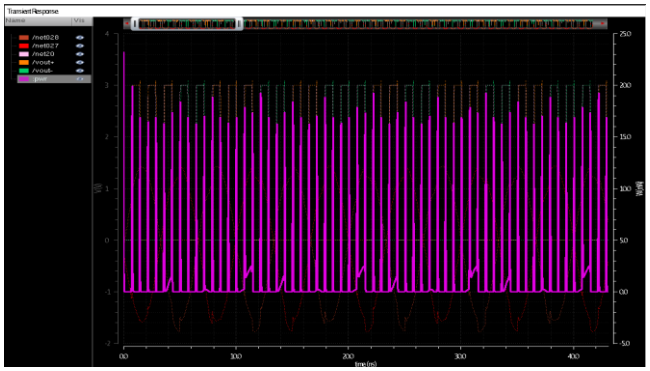

Fig. 11 Transient Analysis Simulation of the Comparator

Summary of the simulated results of the comparator is shown below.

Table 7. Simulated Results of Comparator

Parameter	Result for Schematic
Technology	CMOS 180nm
Operating frequency	150MHz
Power	0.3303mW
Power Supply	5V

Fig. 12 shows the simulation test circuit of the D flip-flop. The input signal frequency is 300MHz with power supply of 5V.

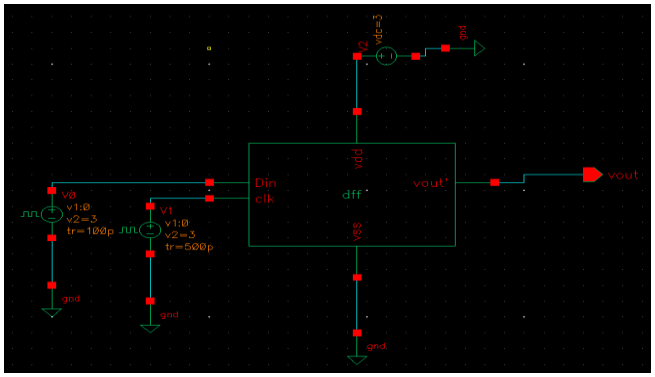

Fig. 12 Test Circuit of the D Flip-Flop

Fig 13 shows the transient analysis simulation result of D flip-flop for a time interval of 200ns.

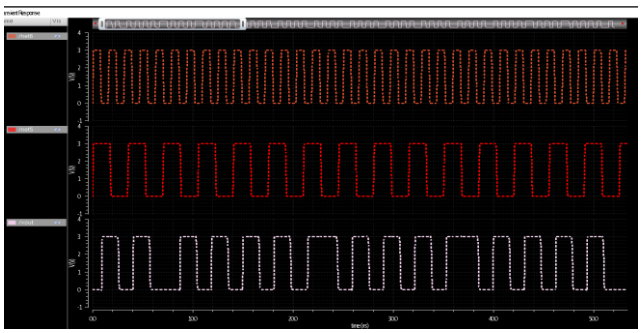

Fig. 13 Transient Analysis Simulation Results

Fig. 14 shows the power measurement waveform of D flip-flop for a power supply 5V. using calculator in cadence for this waveform the power consumed by the D flip-flop is 3.0469µW.

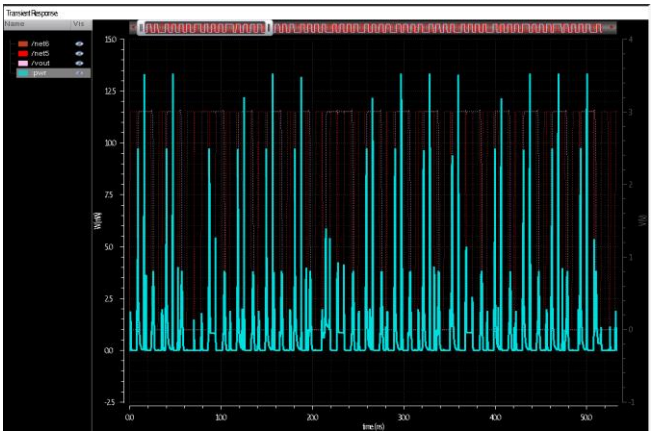

Fig. 14 Power Waveform of D flip-flop

The summarized simulation results of the D flip-flop shown below.

Table 8. Summarized Result of D Flip-Flop

Parameter	Result of Schematic
Technology	CMOS 180nm
Operating Frequency	300MHz
Power	3.0469µW

VI. CONCLUSION

The design and experimental results for two stage op-amp, comparator and D flip-flop as shown which are best suited for the fifth order continuous-time sigma-delta modulator has been presented. This modulator is suitable for the wireless and broadband communications. All the three components all together consumes 0.6951mW while operating at 5V.

VII. ACKNOWLEDGMENT

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Ms. Sunita A Rathod, is Pursuing her Final Year M.Tech Degree in VLSI and Embedded Systems at VTU Extension Center, UTL Technologies Ltd., Bangalore. Her research includes Design of Analog Systems.

Dr. Siva Yellampalli, is Working as a Professor in Dept. of Electronics and Communication Engineering at VTU Extension Center, UTL Technologies Ltd., Bangalore. His research includes Design of RF Communication Systems.

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