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Design of an Error Detection and Correction Architecture for Video Coding Testing Applications

S. Rajasekhara Reddy, P. Surya Prasad

Abstract*— Motion estimation plays a vital role in today's media applications. Hence testing of such a module is a significant concern. Even though several algorithms have been proposed in the past testing of motion estimators are seldom addressed. The proposed system describes an Error Detection and Correction (EDCA) design that detects and recovers data in the motion estimator. The system uses the Sum of the Absolute Difference (SAD) method to compute the difference in the current and reference frames. The architecture comprises of an Error Detection Circuit (EDC) and a Data Recovery Circuit (DRC) to recover the original data. A Residue-Quotient code is used to compute the change in value between the error and expected values. Built-in Self test Technique (BIST) is included in the MECA and in each of Processing Element in MECA. Thus by introducing the BIST Concept the testing can be done internally without connecting outside testing requirements. So the area (number of gates) required and time is also reduces.

Index Terms*—Data recovery, Error detection, Residue quotient, MECA.

I. INTRODUCTION

Multimedia applications are becoming more flexible and reliable with the advancements in semiconductors, Digital Signal Processing and Communication technologies. Some of the Video Compression standards include MPEG-1, MPEG-2, and MPEG-4. The advanced Video Coding standard is MPEG-4.Video compression is essential in various applications to reduce the total amount of data required for transmitting or storing the video data. ME is of priority concern in removing the temporal redundancy between the successive frames in a video coding system and also it consumes more time. ME is considered as the intensive unit in terms of computation [1]. Regular arrangement of PEs with size 4x4 constitutes a ME. Advancements in VLSI technologies facilitate the integration of large number of PEs into a single chip. Large number of PEs arranged as an array helps in accelerating the computation speed. Testing of PEs is essential as an error in PE affects the video quality and signal-to-noise ratio. Numerous PEs in a ME can be tested concurrently using Concurrent Error Detection (CED) methods [5].

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*Correspondence Author(s)
S. Rajasekhara Reddy, Pursuing Masters in VLSI System Design at MVGR College of Engineering Vizianagaram, India.
Mr. P. Surya Prasad, worked as Assoc. Prof., in Electronics & Communications Engineering in MVGR College of Engineering Vizianagaram, India.

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In this method, different operations are performed on the same operand. An error is detected by the conflicting results produced by the operations performed. Concurrent fault simulation is essentially an event-driven simulation with the fault-free circuit and faulty circuits simulated altogether. Design for Testability (DFT) techniques are required in order to improve the quality and reduce the test cost of the digital circuit, while at the same time simplifying the test, debug and diagnose tasks [3].Logic built-in self-test (BIST) is a design for testability technique in which a portion of a circuit on a chip, board, or system is used to test the digital logic circuit itself [4]. BIST technique for testing logic circuits can be online or offline. Online BIST is performed when the functional circuitry is in normal operational mode. In concurrent online BIST, testing is conducted simultaneously during normal functional operation. The functional circuitry is usually implemented with coding techniques [5]. Any input pattern or sequence of input patterns that produces a different output response in a faulty circuit from that of the fault-free circuit is a test vector, or sequence of test vectors, which will detect the faults. The goal of test generation is to find an efficient set of test vectors that detects all faults considered for that circuit. Because a given set of test vectors is usually capable of detecting many faults in a circuit, fault simulation is typically used to evaluate the fault coverage obtained by that set of test vectors. Because of the diversity of VLSI defects, it is difficult to generate tests for real defects. Fault models are necessary for generating and evaluating a set of test vectors.

II. PROPOSED EDCA DESIGN

The proposed EDCA scheme shown in Fig. 1 consists of two major blocks, i.e. error detection circuit (EDC) and data recovery circuit (DRC), to detect the errors and recover the corresponding data in a specific CUT [2]. The test code generator (TCG) in the architecture utilizes the concepts of RQ code to generate the corresponding test codes for error detection and data recovery.

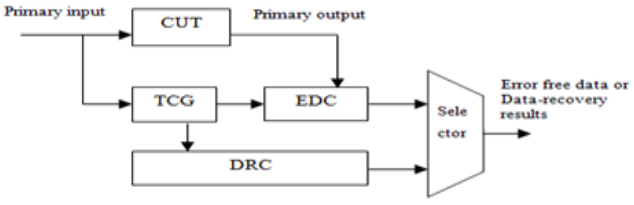

Fig. 1.Conceptual View of the proposed EDCA design

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The output from the circuit under test is compared with the test code values in the EDC. The output of EDC indicates the occurrence of error. DRC is in charge of recovering data from TCG. Additionally, a selector is enabled to select the error free data or data-recovery results.

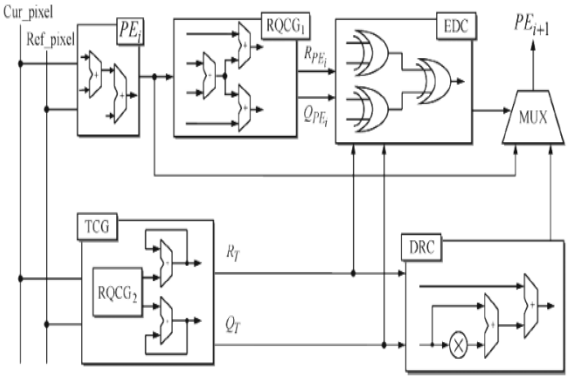

Fig. 2.Proposed EDCA circuit design for a specific PEi of a ME

Additionally, a selector is enabled to export error-free data or data-recovery results. Importantly, an array-based computing structure, such as ME, discrete cosine transform (DCT), iterative logic array (ILA), and finite impulse filter (FIR), is feasible for the proposed EDCA scheme to detect errors and recover the corresponding data.

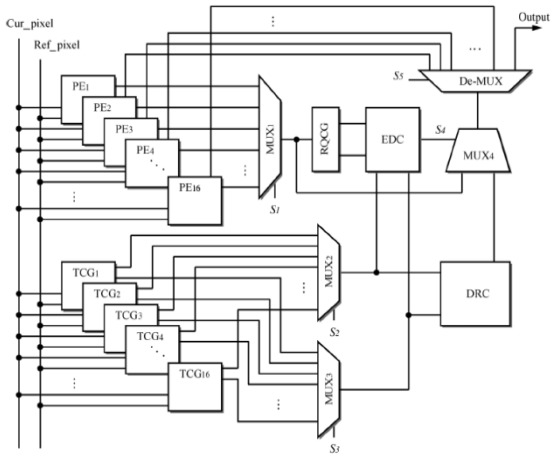

Fig. 3.Proposed EDCA circuit design for a MECA

III. ERROR DETECTION & CORRECTION CODES

Coding approaches such as parity code, Berger code, and residue code have been considered for design applications to detect circuit errors [3],[4]. Residue code is generally separable arithmetic codes by estimating a residue for data and appending it to data. Error detection logic for operations is typically derived by a separate residue code, making the detection logic is simple and easily implemented. For instance, assume that *N* denotes an integer,*N1* and *N2* represent data words, and m refers to the modulus. A separate residue code of interest is one in which *N* is coded as a pair (*N*,|*N* |**m**). Notably, |*N* |**m** is the residue of *N* modulo m. Error detection logic for operations is typically derived using a separate residue code such that detection logic is simply and easily implemented. However, only a bit error can be detected based on the residue code. Additionally, an error cannot be recovered effectively by using the residue codes. Therefore, this work presents a quotient code, which is derived from the residue code, to assist the residue code in detecting multiple errors and recovering errors. The mathematical model of RQ code is simply described as follows. Assume that binary data *X* is expressed as

$$X = \{b_{n-1}, b_{n-2} \ldots\ldots b_2 b_1 b_0\} = \sum_{j=0}^{N-1} b_j 2^j$$

The RQ code of X modulo *m* expressed as R = |X|*m*, Q = X/*m*, respectively. Notably *i* denote the largest integer not exceeding *i*.

In order to simplify the complexity of circuit design, the implementation of the module is generally dependent on the addition operation. Additionally, based on the concept of residue code, the following dentitions shown can be applied to generate the RQ code for design.

IV. FAULT MODEL

A more practical approach is to select specific test patterns based on circuit structural information and a set of fault models. This approach is called structural testing. Structural testing saves time and improves test efficiency. A stuck-at fault affects the state of logic signals on lines in a logic circuit, including primary inputs (PIs), primary outputs (POs), internal gate inputs and outputs, fanout stems (sources), and fanout branches. A stuck-at fault transforms the correct value on the faulty signal line to appear to be stuck at a constant logic value, either logic 0 or logic 1, referred to as stuck-at-0 (SA0) or stuck-at-1 (SA1), respectively. The stuck at fault model can also be applied to sequential circuits; however, high fault coverage test generation for sequential circuits is much more difficult than for combinational circuits. The stuck-at (SA) model, must be adopted to cover actual failures in the interconnect data bus between PEs. The SA fault in a ME architecture can incur errors in computing SAD values [4]. A distorted computational error and the magnitude of *e* are assumed here to be equal to SAD ′- SAD where SAD ′ denotes the computed SAD value with SA faults.

V. TCG MODULE

According to Fig.2, TCG is an important component of the Proposed EDCA design. Notably, TCG design is based on the ability of the RQCG circuit to generate corresponding test codes in order to detect errors and recover data. The specific in Fig. 2 estimates the absolute difference between the Cur_pixel of the search area and the Ref_pixel of the current macroblock. Thus, by utilizing PEs, SAD shown in as follows, in a macroblock with size of *NxN* can be evaluated:

$$\begin{aligned} \mathrm{SAD} &= \sum_{i=0}^{N-1}\sum_{j=0}^{N-1} |X_{ij} - Y_{ij}| \\ &= \sum_{i=0}^{N-1}\sum_{j=0}^{N-1} |(q_{xij}\cdot m + r_{xij}) - (q_{yij}\cdot m + r_{yij})| \end{aligned}$$

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Where Xij and Yij represent the luminance pixel value of Cur_pixel and Ref_pixel, respectively. Based on the residue code, the definitions can be applied to facilitate generation of the RQ code (RT and QT) form TCG. Namely, the circuit design of TCG can be easily achieved (seeFig.4) by using RT and QT.

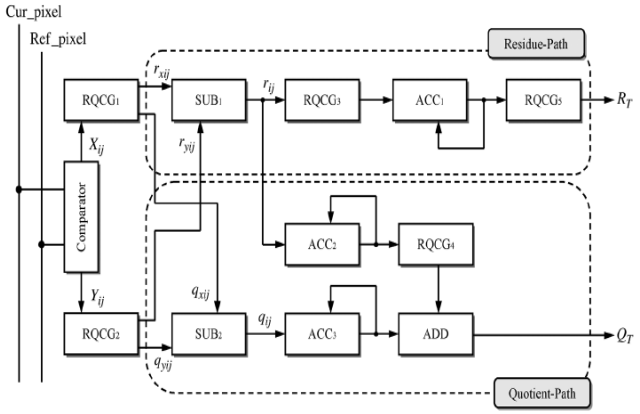


Fig. 4. Circuit Design of the Test Code Generator

VI. ERROR DETECTION CIRCUIT

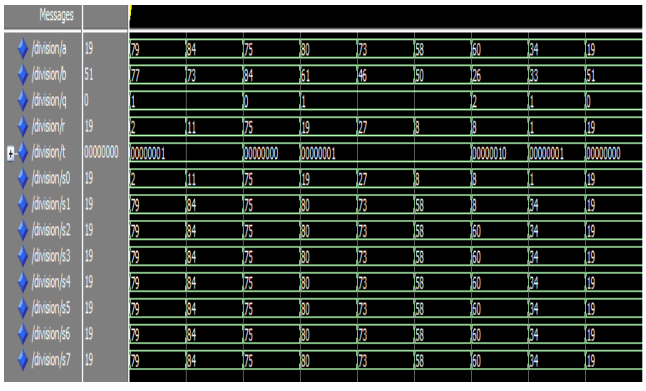
Our proposed EDCA scheme, which comprises two major circuit designs, i.e. error detection circuit (EDC) and data recovery circuit (DRC), to detect errors and recover the corresponding data in a specific CUT. The test code generator (TCG) in utilizes the concepts of RQ code to generate the corresponding test codes for error detection and data recovery. In other words, the test codes from TCG and the primary output from CUT are delivered to EDC to determine whether the CUT has errors. DRC is in charge of recovering data from TCG. Additionally, a selector is enabled to export error-free data or data-recovery results.

Importantly, an array-based computing structure, such as ME, discrete cosine transform (DCT), iterative logic array (ILA), and finite impulse filter (FIR), is feasible for the proposed EDCA scheme to detect errors and recover the corresponding data. This work adopts the systolic ME as a CUT to demonstrate the feasibility of the proposed EDCA design. A ME consists of many PEs incorporated in a 1-D or 2-D array for video encoding applications. A PE generally consists of two ADDs (i.e. an 8-b ADD and a 12-b ADD) and an accumulator (ACC). Next, the 8-b ADD (a pixel has 8- b data) is used to estimate the addition of the current pixel (Cur_pixel) and reference pixel (Ref_pixel). Additionally, a 12-b ADD and an ACC are required to accumulate the results from the 8-b ADD in order to determine the sum of absolute difference (SAD) value for video encoding applications Notably, some registers and latches may exist in ME to complete the data shift and storage. For example of the proposed EDCA circuit design for a specific PEi of a ME. The fault model definition, RQCG-based TCG designs, operations of error detection and data recovery.

VII. DATA RECOVERY CIRCUIT

In this module will be generate error free output by quotient multiply with constant value and add with reminder code. During data recovery, the circuit DRC plays a significant role in recovering RQ code from TCG. Notably, the proposed EDCA design executes the error detection and data recovery operations simultaneously. Additionally, error free data from the tested PEi or data recovery that results from DRC is selected by a multiplexer (MUX) to pass to the next specific PEi+1for subsequent testing. Error concealment in video is intended to recover the loss due to channel noise, e.g., bit-errors in a noisy channel and cell-loss in an ATM network, by utilizing available picture information. The error concealment techniques can be categorized into two classes according to the roles that the encoder and the decoder play in the underlying approaches. Forward error concealment includes methods that add redundancy in the source to enhance error resilience of the coded bit streams. For example, I-picture motion vectors were introduced in MPEG-4 to improve the error concealment. However, a syntax change is required in this scheme. In contrast to this approach, error concealment by post processing refers to operations at the decoder to recover the damaged images based on image and video characteristics. In this way, no syntax is needed to support the recovery of missing data. we have only discussed the case in which one frame has been damaged and we wish to recover damaged blocks using information that is already contained in the bit-stream. The temporal domain techniques that we have considered rely on information in the previous frame to perform the reconstruction. However, if the previous frame is heavily damaged, the prediction of the next frame may also be affected. For this reason, we must consider making the prediction before the errors have occurred. Obviously, if one frame has been heavily damaged, but the frame before that has not been damaged, it makes senses to investigate how the motion vectors can be extrapolated to obtain a reasonable prediction from a past reference frame. In method which reconstructs the frame with the aid of neighbor motion vector is successfully applied to motion estimation. Thus, an error signal “1” is generated from EDC and sent to mux in order to select the recovery results from DRC.

VIII. RESULTS



Simulation Waveform of RQ Code

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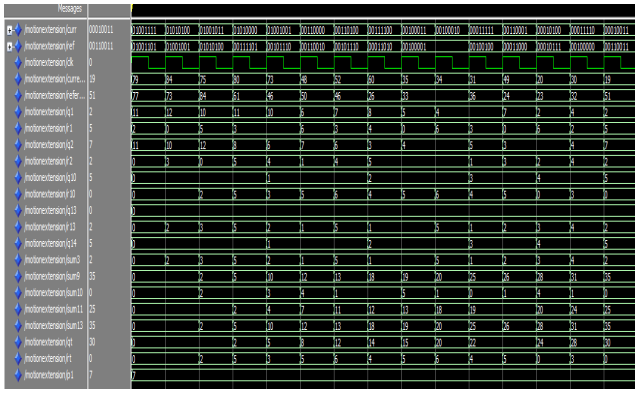
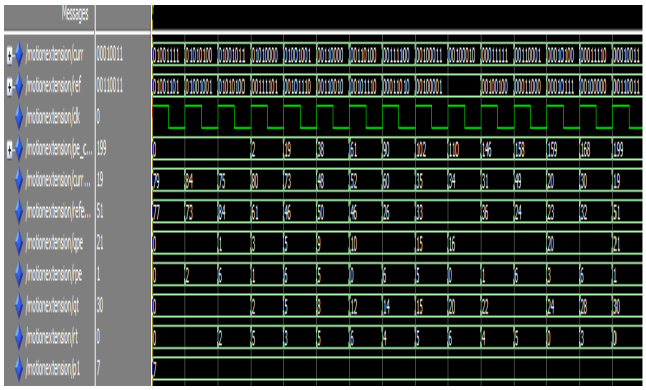
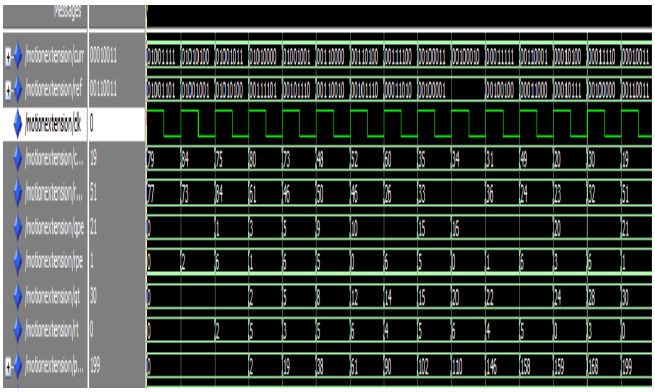


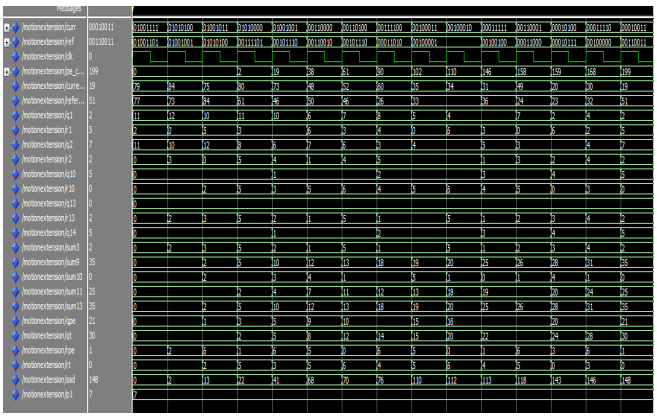
TCG Simulation Waveform



EDC Simulation Waveform



DRC Simulation Waveform



Top Module Simulation Result an MECA

IX. CONCLUSION

This project proposes EDCA design for self-detection and self-correction of errors of PEs in an ME. Based on the Error Detection/Correction Codes, a division-based TCG design is developed to generate the corresponding test codes to detect errors and recover data. Performance evaluation reveals that the proposed EDCA design effectively achieves self-detection and self-correction capabilities with minimal area (LUT). The Functional-simulation has been successfully carried out with the results matching with expected ones. The design functional verification and Synthesis is done by using Xilinx-ISE 12.3.

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AUTHOR PROFILE

S. Rajasekhara Reddy, was born in A.P,India He received his B.Tech degree in Electronics and Communication Engineering from S.V.V.S.N college of Engineering and Technology in the year 2011. He is presently pursuing masters in VLSI system design at MVGR college of Engineering Vizianagaram.

Mr. P. Surya Prasad, was born in India, A.P. He received the B.Tech degree from JNTUK, A.P, and M.Tech degree from IIT Delhi, & pursing Ph.D at JNTUK, A.P. He worked as Associate Professor in Electronics & Communications Engineering in MVGR college of Engineering Vizianagaram.

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