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A Symmetric 9 - Level Multilevel Inverter with Minimum Number of Device

Datar Singh Nathawat, Vishnu Goyal

Abstract - In this paper, an improved technique for Multilevel Inverter. The improved technique using less number of switches than conventional Cascade H- Bridge topology which enhances system performance decreases system complexity and also reduces total cost of the inverter. The main objective of this paper is to increase figure of output level by reducing number of power switches without any complexity in the circuit. The merit of this improved modified technique is to reduce THD and High output voltage level. Multicarrier PWM based techniques used for controlling, firing circuit of switching device. In this paper comparison between proposed improved technique and conventional cascaded H-Bridge inverter done. The number of output voltage level is nine. Simulation is done in MATLAB 2010b environment and the waveforms are obtained. The results are analysed using MATLAB/SIMULINK software.

***Keywords**: Multicarrier PWM (MC-PWM), Cascaded H-Bridge, THD, reduced switches.*

I. INTRODUCTION

This portion, the improved topology for inverters is described, in which working profile explained by using of a single-phase nine-level inverter. In general, *m* figure of input dc battery, Input batteries are referred as E_p (where p = 1 to m). Source current from every battery is referred as $i_p(t)$. Controlling devices can be applied using a switching. In Fig. 1, controlling devices and there complementary pairs are presented as (S_p, S'_p) (where p = 1 to m + 1). Nodal voltages are specified as V_p (t) (where p = 1 to m + 1). Load voltage and load current are displayed as $v_L(t)$ and $i_L(t)$, individually.

The functioning style of the improved topology is explained by the help of a 1-Φ inverter that has four input dc batteries E1, E2, E3 and *E4*, as shown in Fig. 1

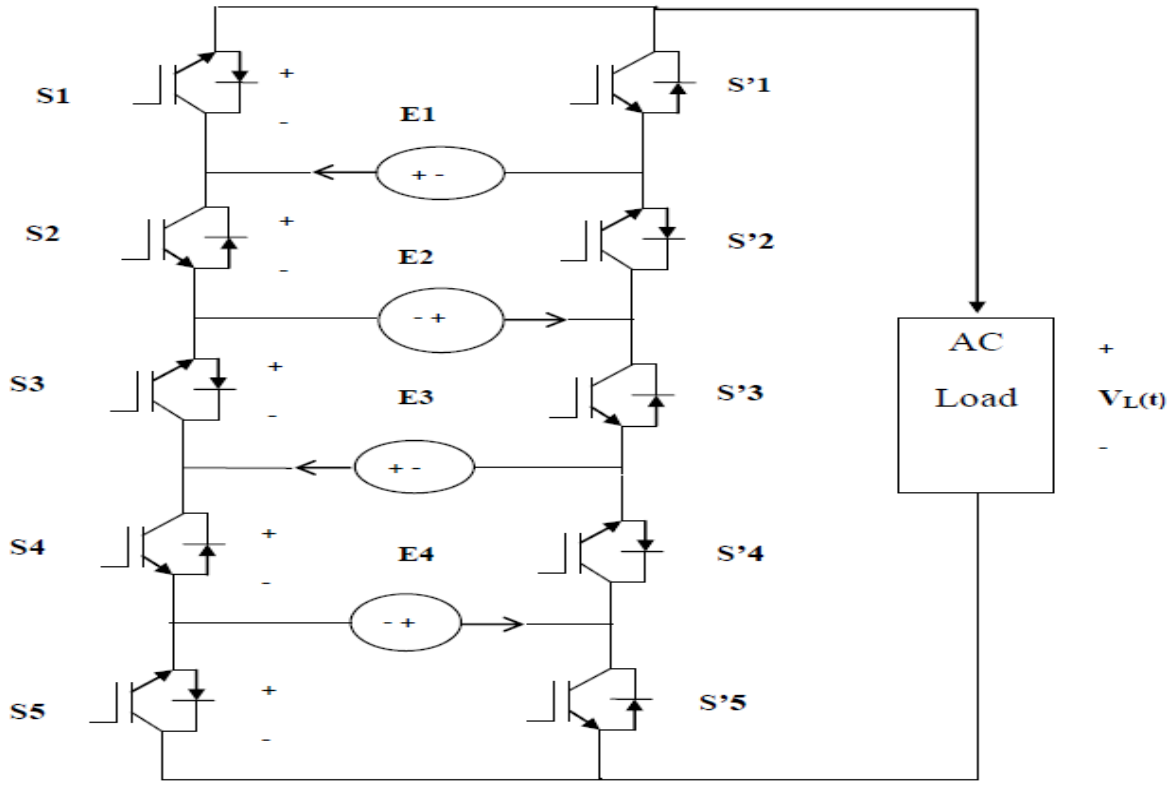

Fig. 1

It has five pairs of switches (S_p, S'_p) (j = 1, 2, 3, 4,5). Meanwhile the elements of controlling device and their complementary are available that has approximately ten operational operating stages. The load is providing with nine levels, viz.,

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*Correspondence Author(s)
Datar Singh Nathawat, Department of Electronics & Communication Engineering, Manipal University Jaipur, Jaipur (Rajasthan). India.
Prof. Vishnu Goyal, Department of Electric and Electronic Engineering, Manipal University Jaipur, Jaipur (Rajasthan). India.

$\mathbf{V_{dc}}$, $\mathbf{2V_{dc}}$, $\mathbf{3V_{dc}}$, $\mathbf{4V_{dc}}$ and **"0"** for $\boldsymbol{E1 = E2 = E3 = E4 = V_{dc}}$, , meant for wholly positive voltage stages and one "0" level, controlling devices S'**2** constantly " ON ", similarly altogether negative voltage stages and additional "0" level controlling device S**2** constantly ON . Thus, this one exists likely to drive these twofold controlling devices at the base frequency to acquire nine output stages. The dc source voltages have been expected to be the same.

In this current effort, the MC- PWM modulation procedure is employed. In a multicarrier PWM procedure, carrier waves are equated with the reference wave, and the controlling signal acquired are employed for controlling of controlling device matching to particular desired output . For improved topology, one device may possibly contribute for clumping or evaluation not only for one stage but involve more stage for required output. Proper used of modes will lead to base switching of S**2** and S'**2** which max voltage pressure of $\mathbf{4V_{dc}}$ every one as matched to the left over switches which max voltage pressure of $\mathbf{V_{dc}}$ each. And so, now the device arrangement is explained wherever all particular or specifies modes are employed to acquire a nine-level output.

The Relative waveforms of the modulation pattern are presented in Fig.2 and Fig.3.Four repeating sequence waveforms of 1-kHz frequency everyone are used as carriers signals. Repeating sequences are designed to use APOD control technique. A sine signal of base frequency is occupied as the reference signal. Carrier overhead the "0 Level" location are indicated as $Z_R^+(t)(R = 1, 2, 3, 4)$, and individuals under the "0 Level" location are indicated as $Z_R^-(t)$ (R = 1, 2, 3, 4). An incessant evaluation of the reference by means of the carriers is executed. If the reference is more than carrier the $Z_R^+(t)$ comparison *provide* "R" else, it produces "R − 1." If the reference is more than carrier $Z_R^-(t)$, the comparison provides "− (R − 1)" else, it produce "−*R*." Signals so acquired are sun so as to acquire a summing measurement value a (*t*). Here, a comparison happened such that involving the pairing of each member of **one** set with only **one** member of another set, without remainder that produce summing measurement value a(*t*) with consistent stages in the required signal is used to acquire firing pulses from summing measurement value a(*t*). To do so, summing measurement value a (*t*) is matched with unremitting levels and the desired firing pulses are used to controlling devices corresponding to the stage consuming the operation table that perform work according a table design and data appearance in table. Here summing measurement value refers as aggregate signal a(t)

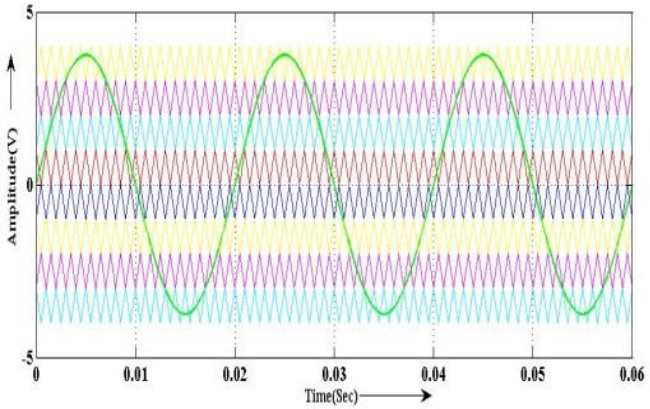

Fig. 2 Reference and Carrier wave forms

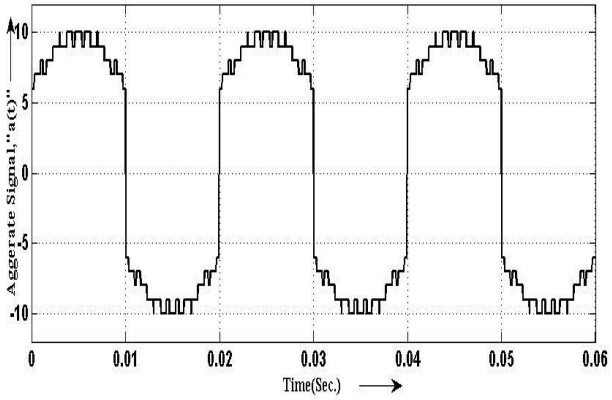

Fig.3. Aggregate Signal

TABLE I: Look Up Table For Nine-Level Inverter (E1 = E2 = E3=E4=24 V)

Value of aggregated signal 'a(t)'	Mode	Load voltage $V_L(t)$ [V]	Switches is ON State
6	1	0	S'1,S'2,S'3,S'4,S'5
7	2	24	S1 , S'2, S'3, S'4, S'5
8	3	48	S1 , S'2, S3, S4, S5
9	4	72	S1, S'2,S3, S'4, S'5
10	5	96	S1, S'2, S3, S'4 ,S5
-6	6	0	S1 , S2, S3, S4 ,S5
-7	7	-24	S'1,S2, S3, S4 ,S5
-8	8	-48	S'1,S2, S'3, S'4, S'5
-9	9	-72	S'1,S2, S'3, S4, S5
-10	10	-96	S'1,S2, S'3,S4, S'5

To evaluate the presentation of improved method and mechanism of control system, also design simulation model for 1-Φ nine-level inverter is designed with MATLAB/Simulink software. Four-dc batteries that is assume equal in value such as showing by E1 = E2 =E3=E4= 24 V are used. The firing pulses are obtained are which shows that switch S2 and S'*2* drive at a base frequency.

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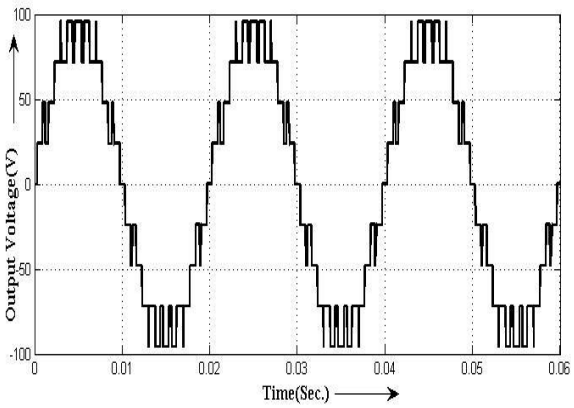
Therefore, lower value voltage evaluated devices drive at upper frequency and allow additional on - off compensations, though higher value voltage evaluated devices drive at base frequency and allow extra conduction sufferers. Here in, the total compensations surrounded by the controlling devices acquire circulated.

Output voltage and frequency are presented in Fig.4 (1) and Fig.4 (2), which indicates, the required voltage waveform has the same stages of 24 V each and a THD of 15.61%. Now, accumulation, using an *R–L* load (R = 3 Ω and L = 2 mH), the Load current and frequency are presented in Fig.5 (1) and Fig. 5(2), correspondingly.



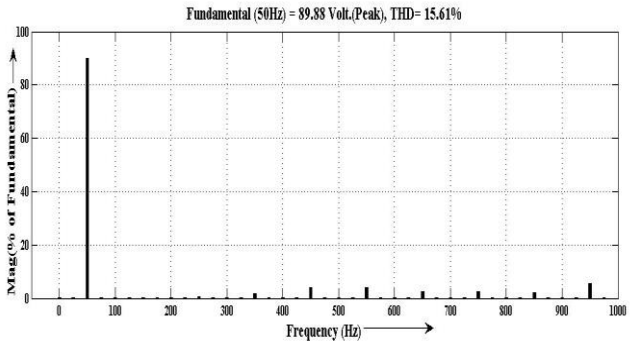
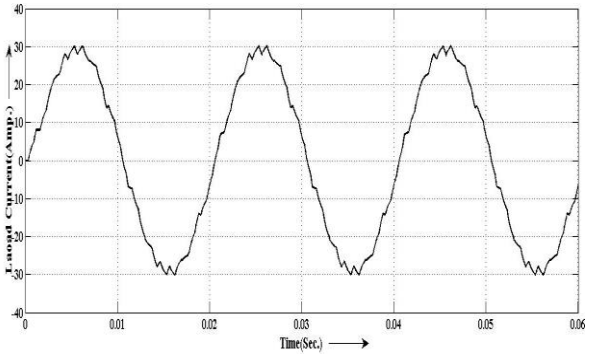


Fig. 4 (1) **Fig. 4(2)**

Fig.4 Simulation Result (1)Nine-Level Output Volatage(V_O) (2) Frequency for V_O.



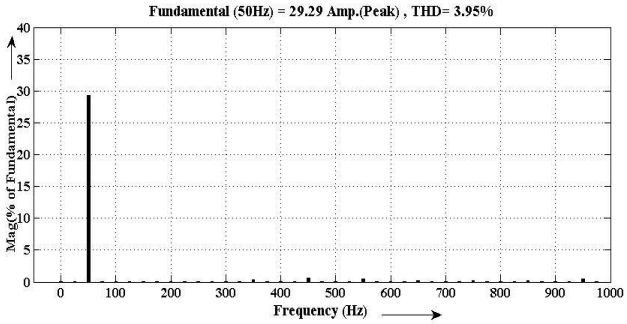


Fig.5 (1) **Fig.5(2)**

Fig.5. Simulation Result (1) Load Current (I_L) (2) Frequency for I_L.

II. Relative Exploration of the Improved Topology done with the Cascade H-Bridge Topology

In this section, an evaluation between the improved inverter method and Cascade H-Bridge inverter is clarifies in expressions of devices requirements, ON-OFF compensations, device budget, and burden accepting competencies. Meant for the determination of evaluation, both topologies are validated in, that mutually have alike figure of equal value dc bases as input. Therefore, by "*m*" figure of bases, every alike to $\mathbf{v_{dc}}$, the figure of stages for both the topologies, and the concentrated output voltage conquered.

TABLE II. Comparison of CHB Inverter and Modified Multilevel Inverter Topology

Topology / Characteristics	Level	Cascade H-Bridge Inverter	Improved Multi-level Inverter
No. of Switches	Five	8	6
	Seven	12	8
	Nine	16	10
Output Voltage (volt.)	Five	42	47.9
	Seven	65	71.88
	Nine	90	89.88
Voltage THD (%)	Five	60.52	31.78
	Seven	45.98	21.63
	Nine	33.20	15.61
Output Current (amp.)	Five	15.80	13.56
	Seven	24.62	20.15
	Nine	38.26	29.24
Current THD (%)	Five	29.07	15.11
	Seven	18.90	6.07
	Nine	14.9	3.95

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1. By “m” figure of dc bases, the Cascade topology have need of “4m” controlling devices , although the improved topology wants “2m + 2” controlling devices. If the evaluation is prepared for a 1-Φ Nine - level voltage, a Cascade H-Bridge inverter necessitates 16 devices, while the improved topology requirements simply 10 devices.
2. For situation of the nine level inverter, the ON-OFF compensations conducted in the improved method are nearly around 50 % ON-OFF compensations conducted in the Cascade topology operative underneath comparable environments.
3. In expressions of control devices budget, the improved Method may well or may well not be reasonable than the Cascade topology subject preceding the presentation wants which point to founded on the collection for devices. Still, improved method suggestions certain improvement in expressions of less figure of devices items and less gathering phases for the reason that of definitely less significant figure of device computation. Mostly for huge figure of output voltage stages.
4. The Cascade topology is extremely flexible, and criticised cells. In adding, the Cascade topology assembly offerings many redundant or undesirable conditions to program an operative burden accepting process .The improved topology, has limited number of repeating or duplicated conditions because of removing the figure of devices , and from now, the opportunity of encoding a burden accepting procedure is poorer than that of the Cascade topology.

III. CONCLUSION

Multilevel Inviters are attainment notice; determinations are presence concentrating in the direction of dropping the device computation aimed at enlarged total of output stages. A improved procedures for novel Multi-Level Inverters has been abridged the device figure.. The functioning of the improved topology has been established, and also Simulation done on a nine -level inverter based on the improved assembly. Evaluation of the modified topology with conventional CHB topologies delights that the modified topology significantly decreases the amount of control devices plus concerned gate driver circuits.

The improved techniques can be effectively engaged for uses wherever quarantined dc bases are existing. By using improved techniques for Nine Level Multilevel Inverter the result improved that is as output voltage V_{output} = 89.88 V with Voltage THD = 15.61 and similar for Load Current = 29.24 A. With Current harmonics order(THD) =3.95 that is showing it has less Voltage THD and Current Harmonics order compare to Cascade H-Bridge Inverter. The benefit of the decrease in the device computation, though, It has two boundaries: 1) requisite of separated dc sources in place of the situation by means of the Cascade topology and 2) moderate modularity and burden accepting proficiencies by means of related toward the Cascade topology.

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AUTHOR PROFILE

Datar Singh Nathawat, has been working as assistant engineer-III (Lab) in manipal university, Jaipur, where he has been working toward the Master degree (M.Tech.) in Power Electronics & System. He obtained his B.Tech. (ECE) from RTU , Kota in 2011. His research interests include multilevel converters, power electronics for renewable energy and electric Vehicles, and distributed generation

Mr. Vishnu Goyal, has been working as Assistant Professor, I in manipal university, Jaipur

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