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Simulation of the Nanoscale Joint Surrounding Gate SOI MOSFET Characteristics

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Abstract. In order to solve the current problem of increasing the efficiency of modern electronic circuits, the applicability of a nanoscale joint surrounding gate MOSFET with oval work area is discussed. The design and principle of its operation are considered. This concept involves of jointing the working areas of n-channel and p-channel MOSFETs. In fact, the JSMOSFET consists of two "glued" along the halves of MOSFETs: one - n-channel and the other - p-channel, but with one common gate. We analyze the applicability of the design of an oval-shaped protected area. In our case, the contact of two heterogeneously doped regions occurs in the plane passing through the small axis of the oval. The main channels are formed in zones associated with the large axis of the oval. This achieves the main goal-increasing the number of charge carriers. At the same time, the efficiency of short-channel effect suppression is maintained and a high current level of the transistor is provided in the strong inversion mode. By the developed TCAD model of a nanoscale joint surrounding gate MOSFET with an oval work area the electrophysical characteristics of several prototypes with different transverse dimensions were numerically calculated at a supply voltage of 0.5 V. From the simulation results, it follows that all prototypes are low-voltage devices that can function at voltages below 0.5 V in the gigahertz frequency range with a high gain. The proposed devices perform the function of inverting the input signal without distortion. From the comparison of modeling data, the scope scaling capabilities are determined. The obtained results create prerequisites for the development of the proposed transistor architecture, since electronic chips created on their basis will differ in low power supply voltage, high performance, and minimal occupied area, which meets modern requirements for transistors for analog and digital applications.

Keyword: nanoscale SOI MOSFET, surrounding gate, short-channel effects, logic gate, low supply voltage

I. INTRODUCTION

Among the variety of architectures of modern field nanotransistors, promising ones are those in which the channel is completely surrounded by a gate, one of which is the architecture with a cylindrical geometry [1-3]. This design is characterized by a two-fold superiority in the suppression of short-channel effects (SCE) compared to traditional transistor architectures [4]. It also has an improved sub-threshold characteristic and increased current density in strong inversion mode. One of the creative extensions of the cylindrical structure is the structure-the joint surrounding gate MOSFET (JSMOSFET) [5, 6]. This concept involves of jointing the working areas of n-channel and p-channel MOSFETs. In fact, the JSMOSFET consists of two "glued" along the halves of MOSFETs: one - n-channel and the other - p-channel, but with one common gate, as shown in Fig. 1. In this case, the transistor structure is placed on a substrate of SOI (silicon on insulator).

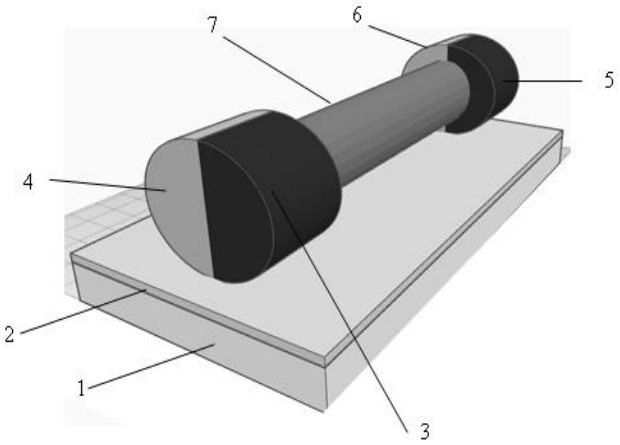

Fig. 1. Block diagram of an JSMOSFET, where 1- silicon substrate, 2- silicon oxide, 3 – n+ - source, 4-p+ - source, 5-n+ - drain, 6-p+ - drain, 7-joint working area

Accordingly, the drain and source of such a structure consists of two highly doping parts with n+ and p+ impurities and in fact represents an ordinary p-n junction. To achieve high efficiency of the protected area, it is necessary that the working area is low doping, ideally its conductivity is close to the intrinsic conductivity of silicon. Then when the power supply voltage (Uds) is applied to the source, it "shifts in the forward direction". The applied offset opens the process of injecting carriers (holes and electrons) into the jointed work area. Their distribution in the channel depends on the gate voltage (Ug). Thus, at Ug>0, the channel is dominated by electrons, and at Ug<0 – holes [7]. In fact, JSMOSFET is a logical gate, whose entrance - gate, the output of the common drain. If Ug $\approx$ 0, then the conductivity of the p-channel transistor is higher. If Ug $\approx$ Uds, then the conductivity of the n-channel transistor is higher [7]. It is obvious that in such a cylindrical structure, the total number of carriers involved in the transfer process is sharply reduced. This will be even more critical when scaling the transistor topology. The direct increase in the core diameter is limited due to the fact that the efficiency of SCE suppression is reduced [8]. The increase in the level of doping of drains and sources is limited by the exponential growth of direct tunnel flow-source currents and a decrease in the breakdown voltage, which is typical for any MOSFET nanotransistor architecture [1, 2]. In this paper, we analyze the applicability of the design of an oval-shaped protected area (JSOMOSFET) for leveling the restrictions discussed above.

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In our case, the contact of two heterogeneously doped regions occurs in the plane passing through the small axis of the oval. The main channels are formed in zones associated with the large axis of the oval. This achieves the main goal-increasing the number of charge carriers. At the same time, the effectiveness of SCE suppression decreases to a lesser extent. Using numerical modeling, the efficiency of the electro physical characteristics of an oval-shaped nanoscale JSOMOSFET was evaluated.

II. JSOMOSFET MODEL

The longitudinal section of the basic structure of the analyzed unit is shown in Fig. 2.

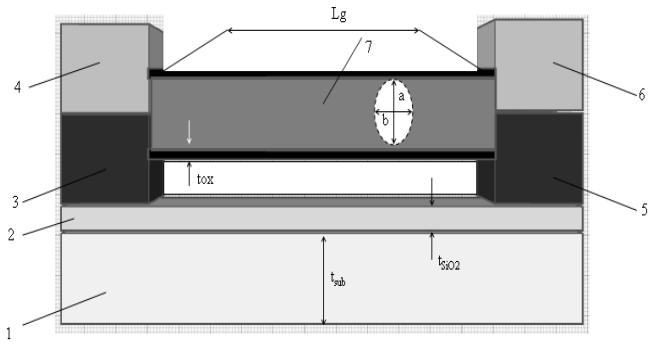

Fig. 2. Block diagram of an JSOMOSFET, where positions 1-6 correspond to figure 1, 7 joint oval working area. Here designations: Lg – gate length, a&b -large and small diameters of the joint working area, tox-thickness of the sub-gate dielectric

For a low doping work area, the parameters of the protected area can vary quite widely by selecting the gate material, actually selecting the desired output operation [2, 3]. Thus, changing the flat band voltage, which allows to control the key transistor characteristics. There are the threshold voltage, the steepness of the sub-threshold characteristic and the DIBL effect [1]. If the gate material is such that the threshold voltages of the n - and p-channel parts of the transistor are approximately the same modulo, then the following scenario is implemented. When Ug =0, only holes are present in the channel, and a high voltage comparable to Uds is set on the drain. When Ug =Uds – only electrons, and the drain is set to a low voltage close to 0 [7]. Thus, when a pulse signal is applied to the gate, its inverted response appears at the output (drain), i.e. the JSOMOSFET operates as an inverter. It should be noted that the considered scenario is implemented for material with a medium-zone output operation [9]. Computer simulation of the electrophysical characteristics of transistor structures was performed using the DESSIS program of the ISE TCAD package [10]. In the course of numerical experiments, devices with different geometric dimensions of the working area were analyzed, the main parameters of which are shown in table 1.

Tabl. 1. Main parameters of the prototype

Parameter	Value
Lg, nm	45
t_{ox}, nm	1.3
t_{SiO2}, nm	50
t_{sub}, mkm	0.6
n_i, cm^{-3}	10^{13}
N_{ds}, cm^{-3}	$3.5x10^{19}$
v_{SRH}, cm/s	$3x10^5$
t_{SRH}, mks	10
A_d, eV	4.65

where: Lg - the length of the working area, tox - the gate oxide thickness (silicon oxide), t_{SiO2} - the silicon oxide thickness, t_{sub} – the thickness of the silicon substrate, n_i – incrustin concentration, Nds – doping concentration of the source and drain, v_{SRH} – speed of surface recombination by the mechanism of Shockley-Read-Hall, t_{SRH} - the lifetime of minority charge carriers for the mechanism of Shockley-Read-Hall, Ad - work function.

In the calculations, the length of the Lg workspace was fixed. The only variation was in the cross-section dimensions, which are shown in table 2.

Tabl. 2. Work area parameters

Prototype number	a, nm	b,nm	l,nm
1	20	5	2.7
2	21	7	3.1
3	22	11	3.7
4	30	15	4.4

where a - large diameter, b – small diameter

When selecting parameters a and b, it is necessary to meet the condition of complete suppression of SCE, which can be represented as $10l < L_g$, where l is the characteristic length [2, 8]. A mathematical expression for the characteristic length can be obtained from solving the Poisson equation in cylindrical coordinates [4, 7]. The value of the l parameter can be calculated using the following expression:

$$l = 2\sqrt{\frac{\varepsilon_S}{2\varepsilon_{ox}}}\frac{ab(\ln(1+\frac{2t_{ox}}{a})\ln(1+\frac{2t_{ox}}{b}))^{\frac{1}{2}}}{a(\ln(1+\frac{2t_{ox}}{a}))^{\frac{1}{2}}+b(\ln(1+\frac{2t_{ox}}{b}))^{\frac{1}{2}}},$$

where $\varepsilon_S, \varepsilon_{ox}$ - the permittivity of the silicon joint work area and the oxide silicon, respectively. For each pair (a and b) the corresponding characteristic length value are also shown in table 2. It is easy to see that the SCE suppression condition holds for all cases. The length of the uniformly doped drain and source was fixed, which was 100 nm. The borders of the working area and the source/drain are sharp. There is no overlap between the gate and the source and drain areas. The thickness of the sub-gate dielectric (t_{ox}) is selected so as to exclude the influence of the direct tunnel current of the gate. Reduction of the sub-gate dielectric thickness will be limited by excessively high tunnel current [2]. When modeling, we assume that the lattice temperature is constant and equal to 300 K.

III. SIMULATION RESULT

Fig. 3 shows the simulation results of I-V data Ids(Ug) at Uds=0.5 V for four prototypes.

The analyzed prototypes operate in the normal mode in accordance with classical concepts.

In this case, the largest current flows in the "thick" prototype (number 4), and the smallest flows in the "thin" prototype (number 1). Maximum current (Ids_max) for each prototype is shown in table 3.

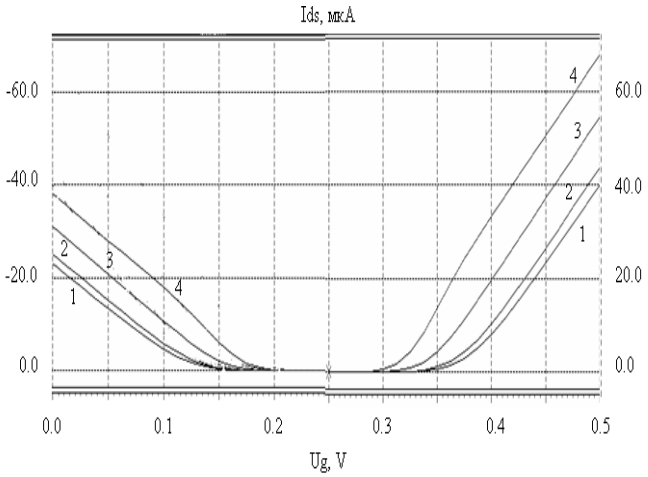

Fig. 3. I-V data Ids(Ug) at Uds=0.5 V. Here the curve number matches the prototype number (see table 2).

Tabl. 3. Maximum current and time delay

Prototype number	Ids max, mkA	τ , ps
1	40,0	2,3
2	42,2	3,2
3	53,4	4,5
4	69,6	6,5

In all prototypes, the current provided by n-type carriers is 1.82 times higher than the current supported by p-type carriers. The value of this ratio does not change from prototype to prototype. It should be noted that the ratio of the maximum currents of different prototypes does not correlate with the ratio of the squats of their cross sections.

Figure 4 shows the dependence of the maximum current on the characteristic length, which characterizes the possibility of scaling the transverse parameters of the working area.

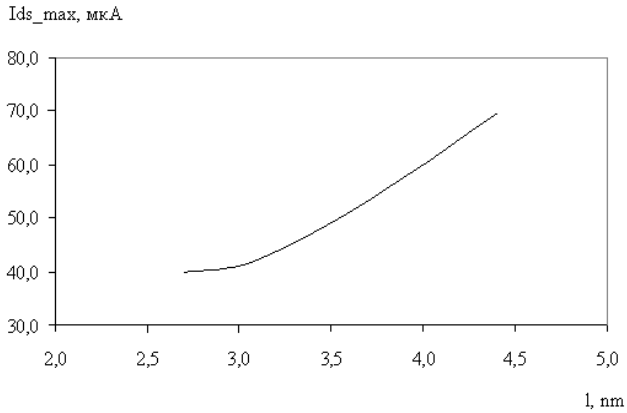

Fig. 4. Dependence Ids_max(l) at Uds=Ug=0.5 V.

When scaling for largest a and b, there will be an almost linear decrease in the maximum current. For "thin" working areas (small a and b), the maximum current of the transistor will be almost constant.

For each prototype, the transfer characteristic for different Uds values is modeled, and for prototype 1, this family is shown in figure 5.

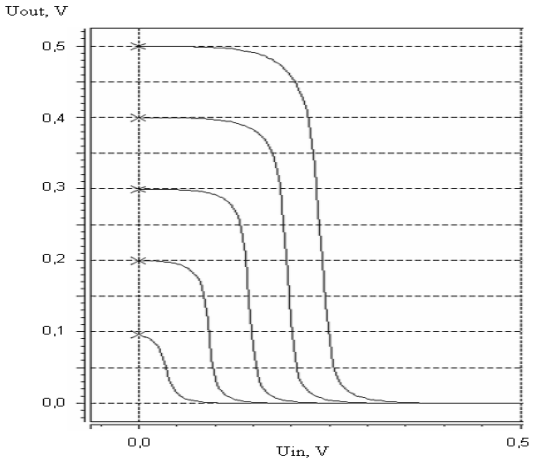

Fig. 5. The family of JSOMOSFET characteristics, where the Uds varies from 0.5 to 0.1

The simulation results show that the performance of all units is preserved in a wide range of Uds. What is noteworthy is that in the area of low applied voltages (less than 0.5 V), they operate close to the ideal inverter with a high voltage gain [5]. At the same time, the sub-threshold current of the transistor is not much, but higher compared to the classic MOSFET. This is the result of a constantly open p-n transition of the combined source. Therefore, the static power of the transistor will be higher. This determines the need to analyze the methods of heat removal in advance at the stage of development of the chip design [6]. The dynamic characteristics of all prototypes in the mode of a large high-frequency signal were calculated for an unloaded transistor. Fig. 6 shows the transient characteristic of the prototype 1. For an input signal with an amplitude of 0.5 V and a frequency of 10 GHz, the time delay of switching the transistor is 2.3 ps. The delays of the other prototypes are shown in table 3. It should be noted that the weight of the device transmits the pulse sequence without distortion. The time delays of the studied prototypes differ significantly. This is due to the large difference in the capacities (cross-sectional areas) of the prototypes. In accordance with classical concepts, the lower latency is due to a smaller capacity (smaller cross-sectional area). In our case, even the large current of prototype 4 cannot compensate for the lag in delay relative to prototype 1.

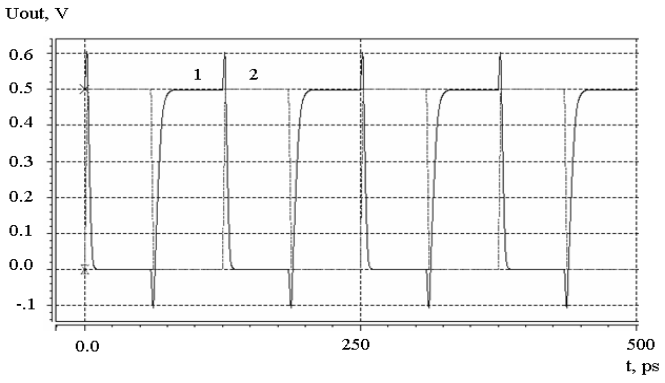

Fig. 6. Transients in JSOMOSFET number 1, where the 1 – input signal (point line), 2 - output signal (solid line).

Figure 7 shows the dependence of the time delay for each prototype on the characteristic length at a supply voltage of 0.5 V. This dependence is almost linear.

Comparing the simulation results shown in Fig. 4 and 7 and in table 3, we can say that there is a correlation between the characteristic length, currents and delays. Therefore, when scaling, it is possible to reliably predict changes in both the transistor currents and delays if the conditions b/a>0.2 for a>b are met.

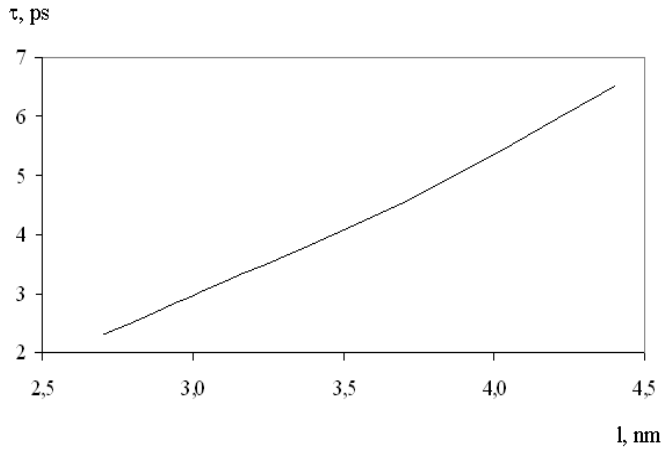

Fig. 7. Dependence τ (l) at Uds=0.5 V.

A distinctive feature of this transistor design is the ability to be placed in a vertical position, which significantly increases the degree of integration [5-6]. Summarizing the results obtained, it can be assumed that devices based on the considered transistor architecture can be used in the development of analog and digital circuits applicable for both high-frequency and low-voltage applications. The presented transistor architecture potentially allows for a wide variety of design versions: with a single gate or with several, with an unevenly doped active region, with combined gates with different output operation, and the "underlap" design [10, 11]. This variety of configurations will greatly simplify the task of designing complex-functional electronic circuits [3, 6].

IV. CONCLUSION

Developed a design of a nanoscale joint surrounding gate MOSFET with a work area of oval shape. The operated principles of a nanoscale joint surrounding gate MOSFET with an oval work area under different modes of control voltages at its contacts are analyzed. The TCAD model of this transistor was developed. With the help of computer simulation the electrophysical characteristics of several prototypes with different transverse dimensions were numerically calculated at a supply voltage of 0.5 V. From the simulation results, it follows that all prototypes are low-voltage devices that can function at voltages below 0.5 V in the gigahertz frequency range with a high gain. The proposed devices perform the function of inverting the input signal without distortion. From the comparison of modeling data, the scope scaling capabilities are determined. The obtained result create prerequisites for the development of the proposed transistor architecture, since electronic chips created on their basis will differ in low power supply voltage, high performance, and minimal occupied area, which meets modern requirements for transistors for analog and digital applications.

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