Performance Analysis of Non-Identical Master Slave Flip Flops at 65nm Node

Urvashi Chopara, Alok Kumar Mishra, D. Vaithiyanathan

Abstract: **This paper presents the performance analysis of the different master slave flip flop reported and comparison of their parameters such as power, area, delay setup time and hold time. To reduce the number of transistor count various logic structure mater slave design have been proposed that results reduction in total area of the flip flop. Advantage and disadvantage of the each flip flop has been discussed. Process corner analysis of all flip flop is also presented at supply voltage of 0.7 volts at 27°C temperature. Percentage reduction in power and speed of operation i.e. frequency are discussed**

Keywords: Transmission gate, auxiliary transistor, Flip Flop, switching activity.

I. INTRODUCTION

THE technological advancement such as Internet of Thing (IoT) devices means that processors are now going to be comprehensive [1]. IoT have application in various field that includes smart environments and transportation, healthcare, traffic etc. However, prevalent deployment of these devices demands low power/energy [2]. Based on such background several types of master slave flip flop logic structure have been reported. From the last decade main idea behind the development of the flip flops is the need of low power consumption circuit without any degradation in speed and area concern are also there behind the development in addition to single-phase clocked circuits minimization power efficiency[3][4]. A considerable reduction in power consumption can be seen using single phase clocked circuits. A flip flop should be contention free that helps in lowering power consumption concerns [5] [6].

II. REVIEW OF DIFFERENT MASTER SLAVE

In the era of VLSI circuit there is a need of a storing element that consumes less power and will not get effected by the changing input. A master slave circuit fulfils this requirement [6]-[10]. The conventional master slave i.e., SRMS Flip Flop consist of 30 transistor. In order to reduce area some other Flip Flop have been reported. One of them is Transmission gate Flip Flop (TGFF) shown in fig.1 which is the most commonly used Flip Flop now a days. It consist of 4 transmission gates, 6 inverters and 2 inverters in its clock generator circuit. There is requirement of additional circuitry for generating clock and clock bar signal in both SRFF and TGFF clock. Clock and clock bar signals makes sure that either one of master slave should work at a time. Along with the requirement of extra circuitry for clock and clock bar signal there is a problem of clock overloading in TGFF. There is a work load of 12 transistors on a clock which causes a persistent power consumption even at the condition when input vestiges static. This setback in additionally occurs in SRFF too [11]-[16].

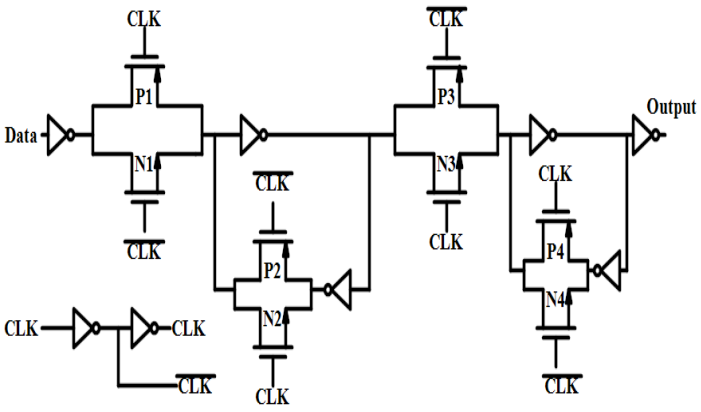

Fig. 1. CMOS circuit of TGFF

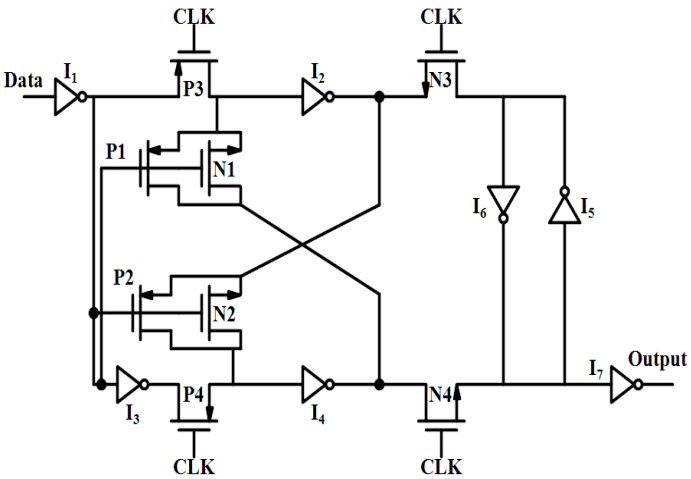

Fig. 2. CMOS circuit of ACFF

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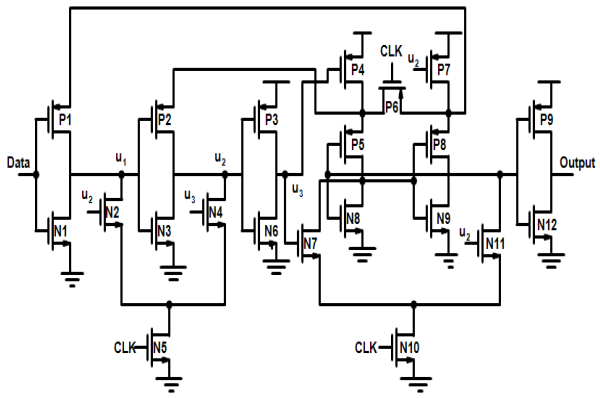

Fig. 3. TCFF CMOS circuit

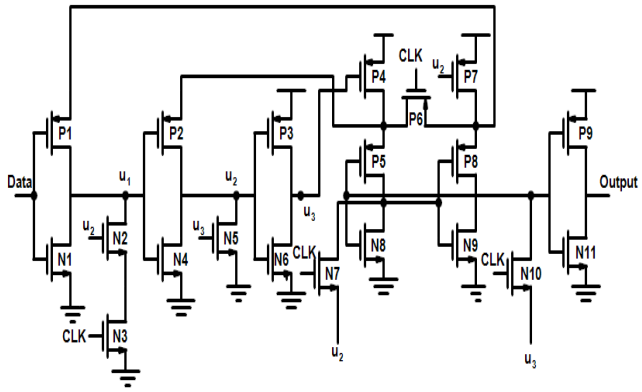

Fig. 4. CMOS circuit of LRFF

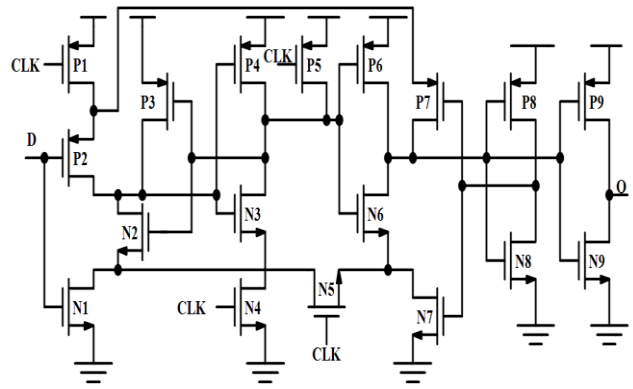

Fig. 5. CMOS circuit of 18TSPC

Therefore the aim of the circuit designer is not only reducing the transistor count but also to achieve a circuit that rescue it from clock overloading. A number of circuit have been reposed so far including these two properties. One of them is Adaptive Coupled Flip Flop (ACFF) in Fig.2 which consist of 22 transistors. It consist of 4 pass transistors that help to provide a strong 0 or strong 1 to master and slave. ACFF consist of a differential structure having a NMOS and a PMOS transistor connected parallel having same input at gate terminal. This differential structure forms a latch in master ride and it overcomes the impact of process variation on master latch. There is a considerable variation in power consumption can be seen from table. Transistor count reduction is only 2 transistor but power is considerable. This is due to no clock overloading problem in ACFF. Another circuit called topologically compressed Flip Flop based on the idea of making master circuit using multiplexer circuit. By topologically compressing the circuit of SR Flip Flop that use multiplexer as a master, TGFF [6] has achieved like ACFF [5], TCFF [3] also have no clock overloading in fig.3. Another reported Flip Flop design is Logic Structure Reduction Flip-Flop (LRFF) [2] in fig.4 that consist of 19 transistors with no work load on clock problem. It is further extension of TCFF. It consist of CPL structure (Complementary Pass Logic) that replace 2 NMOS transistor connected in such having one transistors with input clock and other with input u1, u2 to a transistor having input as clock and u1,u2 connected to source.

The recent MSFF reported is 18TSPC flip flop that have transistor count of 18 in fig.5. Main idea behind 18TSPC is the replacement of master and slave by multiplexer.

In TCFF only master is replace by a multiplexer but in 18TSPC both master and slave are replaced by multiplexer.in 18TSPC also used the topological compression technique. Transistor having clock signal are converted to a single transistor with clock signal as input. Drawback of 18TSPC is that the master is not holding the data correctly when clk=1. There is no direct Path from input to output can be seen in 18TSPC FF.

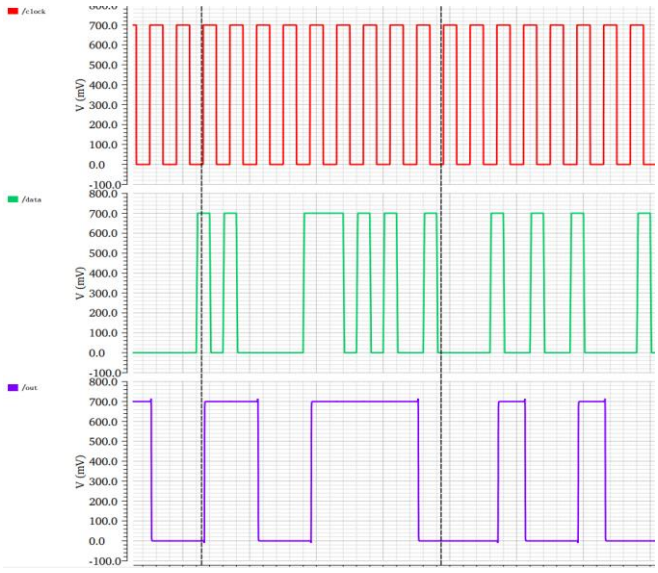

Fig. 6. Output Waveform of Master Slave Flip Flops

III. RESULT AND DISCUSSION

Tabulation comparison of flip flops is shown in Table I. It is shown that as transistor count is reducing from TGFF to 18TSPC, power consumed by the flip flop is also reducing. Clock to Output and Data to Output delay of the flip flops are in a decreasing manner because of less number of transistors in the critical path. Further comparisons of these Flip Flops are made on the basis of Layout Area, Setup time, Hold time, and PDP's.

TABLE I COMPARISON OF VARIOUS FF DESIGNS AT 500MHZ AT 0.7 V

FF Designs	TGFF	ACFF	TCFF	LRFF	18TSPC
Number of Transistors	24	22	21	19	18
Layout Area(um^2)		39.07		45.14	28.76
Clock to Q Delay(ps)	126.4	40.98	69.77	40.17	73.37
Data to Q Delay(ps)	1641	1556	1585	1555	968.4
Average power (uW)	1.099	0.594	0.760	0.561	0.285
SetupTime(ps)	208.2	239.6	239.8	209.8	283.6
Hold Time(ps)	190.6	160.3	160.2	190.2	215.2
PDP_{CQ}(aJ)	138	24.3	53.02	22.53	20.91
PDF_{DQ}(fJ)	1.803	0.924	1.204	0.872	0.276

TABLE II CQ DELAY AND POWER OF 18TSPC WITH TEMPERATURE (nW)

Temp	CQ Delay(18 TSPC)	Power(18 TSPC)
-25	73.28	0.264u
0	73.23	0.273u
25	73.35	0.284u
50	73.61	0.299u
75	74.01	0.320u
100	74.61	0.349u
125	75.37	0.387u

TABLE III POWER VS SUPPLY (uW)

Supply\ f/f	TGFF	ACFF	TCFF	LRFF	18 TSPC
0.5	0.535u	0.285u	0.393u	0.231u	0.154u
0.6	0.753u	0.408u	0.480u	0.371u	0.211u
0.7	1.099u	0.594u	0.760u	0.561u	0.285u
0.8	1.532u	0.903u	1.108u	0.866u	0.386u
0.9	2.324u	1.596u	1.692u	1.476u	0.627u
1.0	4.680u	3.278u	3.225u	3.076u	1.578u

TABLE IV SWITCHING ACTIVITY(S.A.)VS POWER (uW)

S.A.\F/F	TGFF	ACFF	TCFF	LRFF	18TSPC
100%	1.312u	1.128u	1.342u	0.925u	0.480u
50%	1.954u	1.776u	2.717u	1.690u	0.607u
25%	1.355u	0.919u	1.592u	0.851u	0.369u
12.5%	1.080u	0.497u	1.048u	0.439u	0.248u
0%	0.940u	0.216u	0.700u	0.225u	0.315u

TABLE V PROCESS CORNER POWER (uW)

Process Corners	TGFF	ACFF	TCFF	LRFF	18 TSPC
TT	1.098	0.592	0.324	0.556	0.285
SS	0.968	0.461	0.257	0.425	0.254
SF	1.122	0.640	0.352	0.602	0.301
FS	1.120	0.599	0.339	0.574	0.296
FF	1.397	1.054	0.656	1.060	0.468

Fig.6 shows the output waveform. Waveform satisfies for different combinations of clock and data. Table II shows the CQ DELAY and POWER comparison of 18TSPC circuit at a temperature range of 25 degree to 125 degree. As temperature if rising delay and power is increasing, but in a controlled fashion. Table III shows the power consumed by Flip Flops at different supply voltages. 18 TSPC FF have least power consumption value among different FF. Table IV shows power vs. switching activity variation of different flip flops. Switching activity is the fraction of occurrence of data at constant clock pulses. 18TSPC have least power consumption among 5 flip flops.

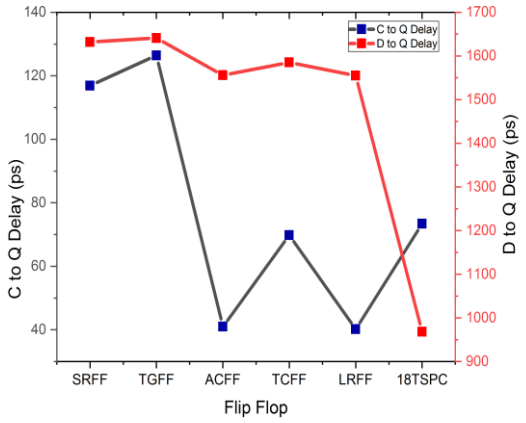

Fig. 7. Data to Q delay and Clock to Q Delay of different Flip flops

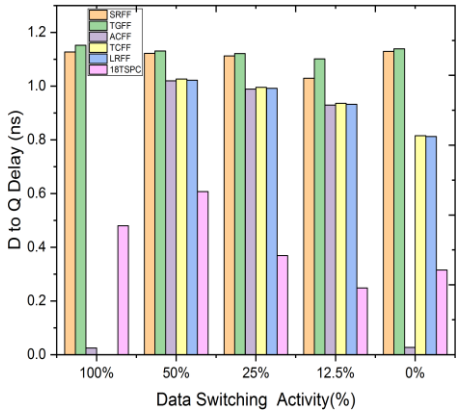

Fig. 8. Data Switching Activity vs. Data to Q Delay.

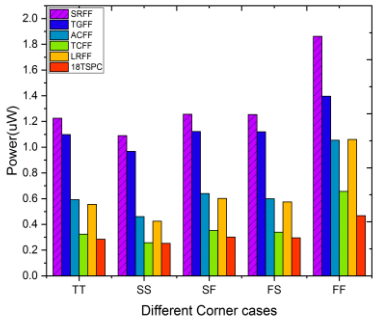

Fig. 9. Process Corner analysis of different flip flops

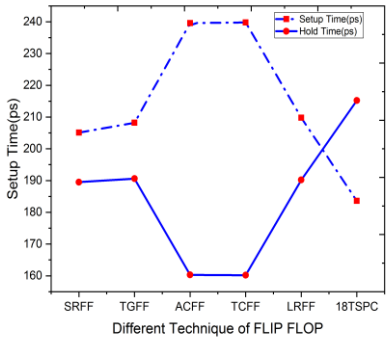

Fig. 10. Setup and Hold time of various flip flops

IV. CONCLUSION

From the results we can see that there is considerable reduction in power dissipation when clock overloading problem has been eliminated. There are two advantage in the ACFF, first is two pass transistor is used in order to pass strong zero or strong 1 from either of them second is differential structure having PMOS and NMOS in parallel that helps to pass strong logic 0 or logic 1in latch. From the ACFF we can get the idea of how transistor count can be reduce without affecting the performance. In TCFF redundant transistor are replace by 2 transistor each in Master and Slave. From the LRFF one can learn To reduces two transistor having input as clk and node voltage to only one transistor having as input and node voltage at source terminal of the transistor having clock as input.

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