# Modelling and Simulation of Tri-layered (s-Si/s-SiGe/s-Si) Channel Double Gate NanoFET

**Kuleen Kumar, Rudra Sankar Dhar**

***Abstract*: The down scaling of Meatal Oxide Semiconductor Field Effect transistor (MOSFET) devices nevertheless the most important and effective way for accomplishing high performance with low power adopted the miniaturization trend of channel length from the past, which is very aggressive. The double gate NanoFET with the incorporation of the strain Silicon technology is developed here on 45nm gate length comprises of tri-layered (s-Si/s-SiGe/s-Si) channel region with varied thicknesses. The induction of strain increases mobility of charge carriers. Two gates are deployed in bottom and up side of strained channel provides better control over the depletion region developed by applying same gate bias voltage. This newly developed double gate NanoFET on 45nm channel length provides 63% reduced subthreshold leakage current, and maximum electron drift velocity in strained channel.**

***Keywords* : *HOI MOSFET, lattice mismatch, strained Silicon, work function.***

## I. INTRODUCTION

In order to follow International Technology Roadmap for Semiconductors (ITRS) conventional MOSFET need to improve with each scaling [1, 2]. But as channel length reduces below 50nm new impacts emerge such as barrier lowering by drain voltage due to shorter gate length, leakage current flow below threshold voltage, and hot carrier effect. The controllability of gate over depletion region formed in bulk MOSFET reduces due to charge sharing between source/drain to substrate [3-5]. The Silicon on Insulator (SOI) technology is adopted to avoid charge sharing in bulk MOSFET. An oxide layer is placed between channel and substrate known buried oxide (BOX). In SOI MOSFET have much greater short channel effect suppressing capability then bulk MOSFET [5].

To enhance the mobility of charge carriers other material such as strained Silicon is also used rather than Silicon. As from literature M.J. Kumar et.al [6] developed a device with strained Silicon (s-Si) on SiGe, shows that strain is developed across channel region due to lattice mismatch between s-Si and SiGe and conduction band splitting in two fold and four fold valleys [6-8].

So the mobility of charge carrier is increased due to strain induction and drive current capability of device gets increased.

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**Kuleen Kumar,** Pursuing Ph.D., Electronics and Communication Engineering, National Institute of Technology Mizoram, Mizoram, India.

**R. S. Dhar,** Assistant Professor, Department of ECE, NIT Mizoram, India.

Furthermore to suppress the narrow channel effects in sub-nanometer scale multigate techniques also incorporated [9]. The double gate MOSFET acquired much better control over the depletion region and minimum electric field penetration.

In this work considering the concept of strain Silicon channel and two gates placed top and bottom side of channel region developed tri-layered channel (s-Si/s-SiGe/s-Si) DG NanoFET on 45nm channel length. This new developed device is analyzed for subthreshold leakage current, electron velocity and maximum electron drift velocity.

## II. DEVICE STRUCTURE AND SIMULATION

The double gate NanoFET with BOX layer inducting the concept of SOI system is designed on 45nm channel length with strained channel comprising of three layers (s-Si/s-SiGe/s-Si) having varied thickness as tabulated in Table 1 employing sentaurs TCAD Tool [10]. This tri-layers channel based structure on 45nm channel length compared with HOI MOSFET developed by Khiangte et.al. [11] on 50nm channel length. The tri-layered channel on bottom and top is developed on SOI surface as shown in Fig. 1. The buried oxide provides lower coupling capacitance between source/drain to substrate. Two depletion regions are developed due to additional gate on bottom of substrate. The cross sectional view of two depletion region formed in double gate SOI NanoFET is shown in Fig. 2

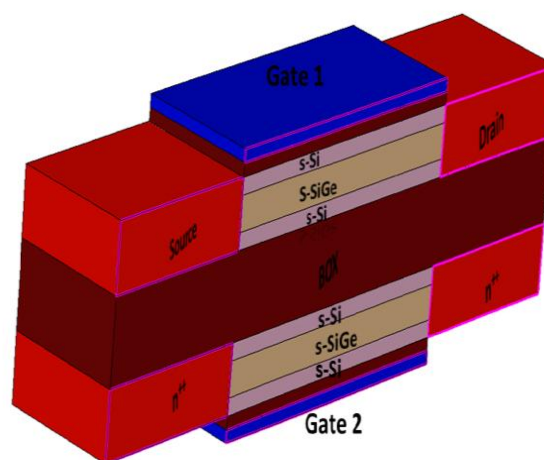


**Fig. 1 A schematic of DGSOI NanoFET with strained channel.**

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Equal potential is applied on each gate having same work function so that equal depletion region is created in the tri-layered channel resulting in lowering of the electric field penetration with minimal short channel effects [12-14]. The doping dependence model Shockley Read Hall recombination [15 -17] and strain induces based piezo-restive model [18] are incorporated in device simulation to investigate strain effect on electron velocity and drift velocity of electrons in tri-layered channel. The induction of strain further enhances the carrier mobility due to confinement in two depletion region of double gate NanoFET.

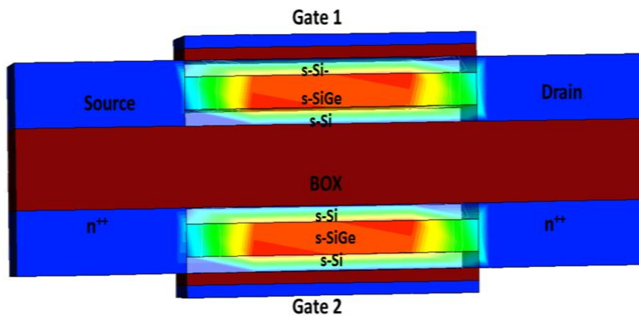


**Fig.2 A cross sectional view for formation of depletion regions in the DGSOI NanoFET.**

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**TABLE 1 Double gate SOI NanoFET with strained channel parameters**

| Parameters | Dimensions |
|---|---|
| Channel length | 45nm |
| Ge mole fraction($m_0$) | 0.2 |
| s-Si layer thickness($t_{s\text{-}Si}$) | 2nm |
| s-SiGe layer thickness($t_{s\text{-}SiGe}$) | 4nm |
| Gate Dielectric thickness($t_{ox}$) | 2nm |
| Source/Drain doping ($N_D$) | $10^{18}$ cm$^{-3}$ |
| Channel doping ($N_{A)}$ | $10^{16}$ cm$^{-3}$ |
| Drain bias | 50mv |

## III. Results and Discussion

The DG SOI based NanoFET with hetero-layered channel is developed using Sentaurus Device Simulator [19] on 45nm channel length. The double gate NanoFET is developed here and analyzed for subthreshold leakage current reduction, enrichment in electron velocity and electron drift velocity in channel region. The current voltage ($I_D$-$V_{GS}$) characteristics of double gate NanoFET is compared with HOI MOSFET on 50nm channel length applying drain bias voltage 50mV as shown in Fig. 3. The two gates are electrostatically coupled and having same work function. The additional gate provide equal potential to bottom depletion region so that more control over channel region is acquired by two gates in short channel device. The leakage current reduction up to 63% is obtained by adding supplementary gate on bottom of substrate. The drain current of double gate NanoFET is compared with HOI MOSFET on 50nm as shown in Fig 2.

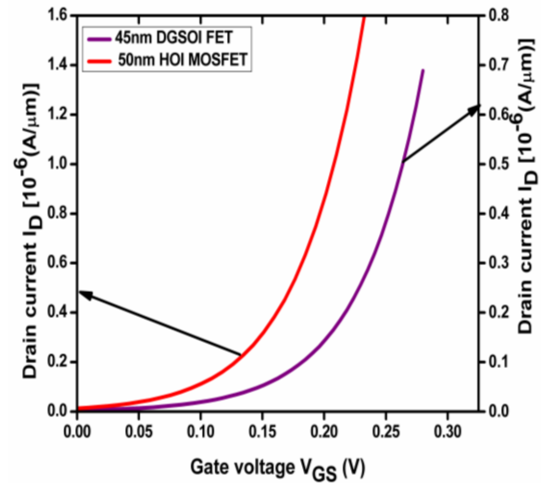


**Fig. 3. $I_D$ –$V_{GS}$ transfer characteristics comparison of double gate NanoFET with single gate HOI MOSFET.**

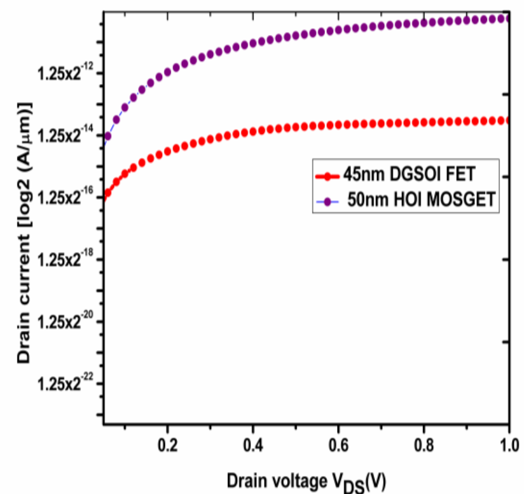


**Fig. 4. $I_D$ -$V_{DS}$ output characteristics comparison of double gate NanoFET on 45 nm with single gate HOI MOSFET.**

The tri-layered channel comprises of (s-Si/s-SiGe/s-Si) with thickness of 2nm-4nm-2nm respectively so that biaxial strain is induced between the hetero-structure. The electron velocity and electron drift velocity from source to drain is also observed in tri-layered channel and compared with HOI MOSFET on 50nm channel length. The electron velocity in double gate NanoFET is show narrow peak in channel region as depicted in Fig. 5. The carriers are confines in narrow channel and depletion region suitably controlled through potential applies on two gates. The electron drift velocity is also observed within three layers of double gate NanoFET on 45 channel length as shown in Fig. 6. The induction of biaxial strain in tri-layered channel and equal potential on two gate maximum electron drift velocity is observed in s-SiGe layer. Due to narrowing the channel thickness, lattice defect mismatch electron mobility gets affected resulting in reduction drain current but ultimately improve overall performance as reduction in subthreshold leakage current is observed on double gate NanoFET 45nm channel length.

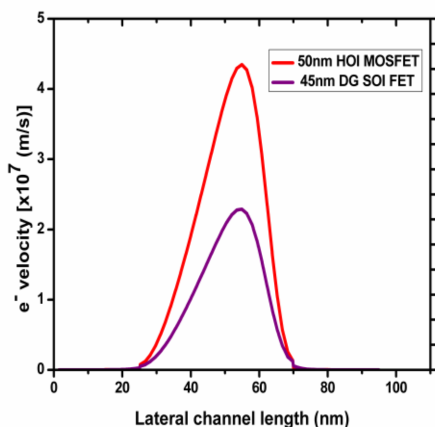


**Fig. 5 Comparison of electron velocity of double gate NanoFET with single gate HOI MOSFET.**

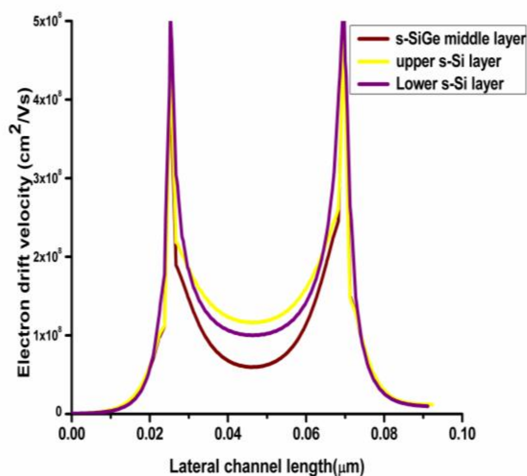


**Fig. 6. Examination of electron drift velocity in tri-layer channel of double gate NanoFET.**

## CONCLUSION

The novel double gate NanoFET with strained channel is developed here on 45nm channel length for the first time. The device characteristics are compared with single gate HOI MOSFET on 50nm channel length. The thickness of tri-layer channel reduced as that of 50nm single gate HOI MOSFET to maintain strain mechanism and threshold voltage roll-off. The maximum drift velocity is observed in s-SiGe layer providing 63% reduced subthreshold leakage current. This novel double gate NanoFET with strained channel has thereby the functionality to fulfill the need of low power and fast operating device with minimal short channel effects in exiting technological era.

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## AUTHORS PROFILE

**Kuleen Kumar** received the M.E, degree in Microelectronics and VLSI Design from Chandigarh University, Punjab India, in 2017. He is currently pursuing the Ph.D. degree in electronics and communication engineering with the National Institute of Technology Mizoram, Mizoram, India. His current interests include semiconductors device modelling on nanoscale with 2-D materials for improving their performance.

**R. S. Dhar** received his M.Phil in Microelectronics from University of Newcastle, UK in 2006 and Ph.D. in the area of Nanotechnology Engineering from University of Waterloo, Canada in 2014. From 2006 to 2010, he worked as Lecturer and then as Assistant Professor in India. He worked as a postdoctoral Fellow at University of Alberta, Canada. Since December 2015, he has been an Assistant Professor with Department of ECE, NIT Mizoram, India. He is the author of one book, and more than 50 articles in international peer-reviewed journals and conferences. His research interests include semiconductor device physics, nanomaterials technology, microelectronic devices and applications.