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Design and Development of a Very Large Scale Integrated Circuit Architecture for a Digital Image Compression and Realization on Field Programmable Gate Array

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Abstract*: *The domain of image signal processing, image compression is the significant technique, which is mainly invented to reduce the redundancy of image data in order to able to transmit the image pixels with high quality resolution. The standard image compression techniques like losseless and lossy compression technique generates high compression ratio image with efficient storage and transmission requirement respectively. There are many image compression technique are available for example JPEG, DWT and DCT based compression algorithms which provides effective results in terms of high compression ratio with clear quality image transformation. But they have more computational complexities in terms of processing, encoding, energy consumption and hardware design. Thus, bringing out these challenges, the proposed paper considers the most prominent research papers and discuses FPGA architecture design and future scope in the state of art of image compression technique. The primary aim to investigate the research challenges toward VLSI designing and image compression. The core section of the proposed study includes three folds viz standard architecture designs, related work and open research challenges in the domain of image compression.

Keywords* : *Image Compression, JPEG, Wavelet Transform, Energy Efficiency, Storage, VLSI Architecture

I. INTRODUCTION

The era of Image processing has moving into automated world and has become most indispensable technique in diversified system on chips (SoCs) for mobile and multimedia applications. The most common and effective image processing techniques are; image signal processing [1], video coding (HEVC) [2] and many more. However, an image compression (IC) is an advance technique in which a process of eliminating the redundant information from the storage system. This is the most emerging research area which is essentially utilized in the field of information accessing that will processed by IoT devices. The huge amount of data will be processed by IoT nodes including multimedia files [3], where IoT devices require more energy and computation.

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Image conversion or transmission over the IoT devices is significant in various fields, such as smart clinical systems, traffic monitoring, gate recognition and etc.

The following figure-1 pictorially describes about general image processing method over IoT environment which comprises with multiple image sensor devices integrated with embedded system and radio-frequency transceivers. Radio-Frequency transmission could be more costly, specifically in terms of energy constraint [4]. Though the 2-dimensional IC technique can help to solve the storage requirement and image transmission among the IoT devise, they are computationally intensive tasks [5]. Therefore, in the study of et.al [6] introduced a concept of IC by analog in memory computation. DWT and DCT i.e. discrete wavelet transmission and Discrete Cosine Transform are most significant image compression (IC) algorithms. The DWT provide multi-resolution representation of signal transmission in both time and frequency and, it is considered as more advantageous in orthogonal transformation [7]. Whereas DCT has more energy conservation capacity by comparing with DWT algorithm, but it has computation complexity. Hence, wavelet transform has been applied in wireless sensor networks and in energy constrained sensor devices and has shown high PSNR and effective compression compared with DCT [8]. The core objective in architecture designing is target outcomes among the communication and computation with more emphasis toward more energy consumption with high computation. The IC technique, for e.g. JPEG-2000, requires complex hardware devices which increases the computation power to the level of communication power. Therefore, multiple numbers of low complexity algorithms have been introduced with the aim to minimize the computation power and prolong the network lifetime with providing high image quality results [9].

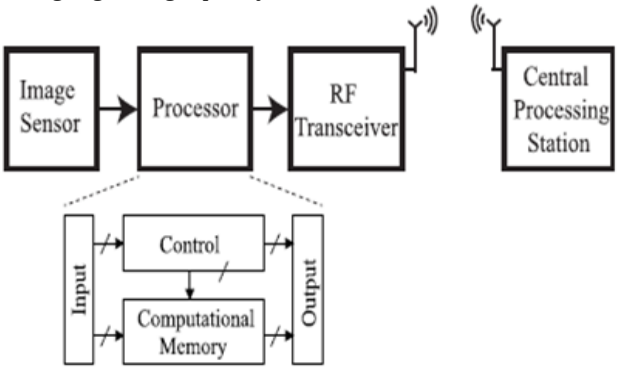

Fig.1. Typical Image processing method

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The most of the IC algorithms has been implemented on hardware/software platform. As software view-point, IC techniques totally depend upon operation which performed such as image transform phase computed by matrix multiplication and matrix transpose calculation. Such image transform operations are not applicable for real world IoT applications owing to the more computational cost and storage requirement [10]-[12]. While in hardware scenario, the complexity of the model design is mainly depends upon two major parameters including storage components and mathematical calculation. The mathematical factor consists of arithmetic operations and modules, while a storage component mainly consists of memory transposition which holds the intermediary outcomes. In contrast, lifting based hardware implementation need very less storage space with minimum computation complexity at high cost rate [13], [14]. Hence, developing the new hardware designs which can efficiently perform IC task for IoT based application and similar way lower cost resource constrained are required.

The core objective of the proposed study is to provide comprehensive report on standard FPGA architecture based image compression algorithms. Also provide comparative analysis on different IC mechanisms with one another and measured the performance parameters in terms of computational cost and energy consumption rate. The outline of the manuscript is structured as; Section-II represents the brief background of IC scheme followed by major research problems identified from the literature studies in section-III. The section-IV discusses about existing research solutions followed by different IC mechanisms with respect to hardware design in section-V. The section-VI illustrates the related work and open research challenges in IC architecture design in section-VII. The last Section-VIII provides conclusion and future directions for designing energy efficient FPGA architecture.

II. BACKGROUND

The image compression is the most evolutionary mechanism in the field for image signal processing which performs the high quality data transmission operation by eliminating the redundant information from existing data and manages the storage efficiency transmission rate. The IC is achieved by reducing the spatial or spectral redundancy among the different image files. The computation process is intensive which involves multiple matrix manipulation operations. These mathematical operations can results both lossy or lossless compression and results higher compression ratio. The typical IC process follows some significant operations; including, in the first phase image is transmitted into compact power representation, i.e. reversible process. Later, the transmitted image is considered for compression that is attained by quantization and programming operations. The threshold value gets clear with certain predefined values and stores useful information with clear image quality which is not recognized by human eyes. Then, the process followed by programming which takes benefits of initial values with high frequency zone. Entropy method is the one of the significant process for wavelet image transmission [13]. Another method of image compression is discussed in [14], [15-18].

The prior IC techniques like JPEG-200, H.264 and HEVC able to eliminate the refund data with minimum energy consumption and transmit the high quality image data. Nevertheless, an energy efficient IC technique like JPEG standard is utilized on conventional IoT based multimedia application to compress the image frame. But, existing IC standards does not fulfills the users demand by providing clear image quality owing to its static implementation methodology. To attain visual lossless 40-dB compressed image, the JPEG method needs floating point processing system which consumes more energy. Additionally, for a high-resolution image with a visually lossless image where information of minute size is important, a line error is advantageous for recovering information rather than an error of a block occurring in conventional block-based compression standard methods. Another requirement for multimedia IoT devices is that a compact compression technique with small physical size and small production cost is often more important than high compatibility, because the IoT devices are often used in dedicated applications which often require very high volume of small-size devices.

III. RESEARCH PROBLEM

The existing image compressing standards like JPEG using DCT algorithm contains more computational complexity and hardware constrained with excessive energy consumption, which is not suitable for WSNs. The JPEG-2000 mechanism was introduced for joint-photography system with the aim of replacing their actual DCT based JPEG standard with wavelet transform. Also JPEG-2000 utilized more complex entropy encoding operation to achieve higher compression ration over the JPEG. Hence, JPEG-2000 IC scheme is not reliable for hardware implementation owing to the computational complexity of wavelet-transform.

Some major research problems are listed below:

1. High performance and reliable VLSI circuit design: A high throughput for encoding the high dimensional images into HEVC format in real time, with efficient software simulation operations.
2. High prediction mode pruning: Proper selection of inter or intra prediction modes, receiving high resolution image data, and cost efficiency with flexible computation.
3. Selection of appropriate encoder: Deciding of reliable and suitable encoding scheme, using HEVC correlation among the neighbors for better coding efficiency.
4. High resolution image feed: Ultra wide-band image memory catering to large size of reference image demand from HEVC.
5. Multi-chip scalability: multi-chip circuit design and data sharing capability scalable to 8k ultra high resolution HEVC encoding.

IV. IMAGE COMPRESSION SCHEME IN HARDWARE

The three primary steps have been followed during the compressions that are a) Quantization, b) DWT and c) Entropy encoding.

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After performance of the preprocessing method, every module has been studied by proper DWT [19]. The FPGA executions might be speed-up the DWT by pipelining these processes. The DWT based-VLSI-design is executed based on real-world signal processing [20]. The Quantization, wavelet image compression as well as lossy compression method is introduced after pertaining the wavelet, where a position of costs is squeezed into a single quantum cost. In the other hand entropy coding may offer a smaller image demonstration by using short code words for probable images and higher code words for minimum probable images [21]. Several low power designs has been demonstrated in the review study for the wavelet transform which is based over allocated arithmetic, spline and lifting. The work of [23] presents the design for DWT based over B-Spline factorization. The B-Spline has been categorizes into two divisions: a) B-Spline division, b) Allocated division.

V. RELATED WORK

The original image representation carries more storage space. Therefore, it can make the more complexity in the system storage system for further operations. In this context, researchers investigated the concept of image compression, in whch efficiently eliminate the redundant information and consider only significant data. The compressed image contains limited bandwidth and takes less energy for transmission process. The transform based IC technique is very preferable mechanism which includes entropy coding and quantization methods. However, image data management in the IoT application with limited energy consumption requires less memory space and contains less complexity in compression. Thus, Lee and Kim [21] introduced a limited memory IC technique for IoT based multimedia applications. The implementation process includes multi-level dual mode DWT and adaptive line prediction. Also includes bit-rate controlling mechanism which responsible to improvise the image quality consistency in single frame. The result analysis show that, the proposed methodology gained high compression ratio compared with existing methods. A hardware based IC algorithm is introduced by Chen et.al [22] using digital and block truncation coding methods which efficiently achieved the compressing color images with low complexity and high performance. The proposed VLSI architecture contains 8.1k-gatesand 100 MHz of frequency range as well as energy consumption rate is 2.9 mega W, which is efficient to implement wireless system with fulfilling the requirement of IC in real scenario. Comparing with prior techniques like JPEG, this mechanism efficiently reduces the power consumption rate at 53%. The initial aim of IC technique is to provide optimal compression ratio with less complexity and minimum energy consumption. The study Adil and Kamil [23] discussed about the fundamental architecture of IC system which automatically set the compression ratio for specific image data and maintain the image quality at higher level. In this experiment, authors adopted Artificial Nerual Network (ANN) mechanism which efficiently compressed the image data as compared to existing methods and determines the optimal compression ratio by linear-regression method and made the analytical reports of different compression ratio. In the last, the study has been proved that, it is an efficient tool for clinical image data analysis with good compression ratio. Chen et.al [24] designed hardware based lossless color IC technique to achieve low complexity with less storage space demand. The previous study of the same authors represented a JPEG encoder model and the study [24] implemented a JPEG based lossless IC algorithm which removes the excessive storage space with small size chip area and maintain the high performance. The proposed algorithm uses the pixel restoration and Golomb-rice programming technique which efficiently reduced the gate counts upt ot 28% and improved the compression ratio at 15.1%. Miguel et.al [25] introduced a dual concept of reversible and irreversible color image transformation scheme name as “Mosaic optimization". The aim is to achieve minimum computational complexity and capable to perform continuous scanning operation. The experimental results shown that, for JPEG-2000 at similar compression-ratio, the optimized resultant transformed image are more similar to original color image as compared to other transform techniques. The both reversible and irreversible transform technique achieved the PSNR up to 0.9 dB and 1.1 dB respectively. Most of the existing studies mainly focused on designing the efficient hardware based IC architectures with the aim to reduce the memory chip siz. The significant fact of these research studies is to introduce IC technique with cost effective hardware architecture. The typical architecture design of line buffer is utilized for static length code by Wang et al. [26]. The proposed mechanism not only improves the compression ratio even also fulfills the specific demands in line-buffer hardware architecture design. Furthermore, the IC algorithm provides the efficient results and pipe-lined VLSI circuit design. The results illustrated that, proposed VLSI architecture achieves the 6.6 PSNR at 50% compression ratio. Halawani et.al [27] introduced the new mechanism of “Memristor based” IC architecture which uses the 2-D DWT method. The proposed architectural mechanism is composed into memoristor-crossbar and intermediatroy array of memory which stores the transformed co-efficient and holds the compressed image content. The performance parameters like PSNR, structural similarity index, and complex wavelets are considered to evaluate the image quality ratio and achieved the better results at quantization and CMOS implementation. In the hardware architecture design, memor size and cost is the most concerning parameters. According to the analysis of memory requirement has been increasing whereas high throughput hardware devices can effectively compress the large amount of data in real application are needed. Hence, Choi et.al [28] proposed a high throughput based hardware architecture which can efficiently perform lossless IC operations. To mitigate hardware cost complexity issues due to the high throughput, authors utilized “Huffman” matrix is implemented, additionally, variable size streaming merge is performed at minimum cost rate by reducing the hardware size by mathematical Haffman coding operation. The proposed concept achieved the high throughput at eight gigabytes per sec with 40% IC ratio and its throughput is superior to prior methods.

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The study by Hsieh et al. [29] presented a VLSI hardware based architecture design with low power, small size and high-performance algorithm design named as SPIHT. The proposed design includes very less code processing time and maintains the high quality while implementing the DWT based ECG image compression data. The simulation results of proposed SPIHT algorithm provides the high computation speed, minimum energy consumption in the VLSI design implementation and speed ups the code implementation in less time. The major advantage of proposed system is highly suitable for healthcare system in ECC image compression. The super-pixel based on chip circuit design is proposed by Kaur et al. [30]. The main objective is minimum energy consumption (at 39 uW with 1.8 voltage supply). The compression results provide PSNR improvements up to 2-3 dB. The experimental analysis was carried out in MATLAB simulator which takes 2xmagnitude less time as compared with existing methods. Also this mechanism applicable for thermal imaging technique. The several research studies faces various computation complexities including power consumption, processing time, compression/decompression challenges, etc. To overcome such major challenges, Onishi et.al [31] designed a single chip video encoder LSI architecture model including multiple features in terms of high prediction rate, high compression ratio for real time multimedia data and centralized encoding operation. Internal 210 megabit image data storage is built and linked with multi-blocks unit with 5120 bit buses with high bandwidth rate. It achieves multi-chip encoding implementation and fabricated with 28 nm CMOS technology which helps to built broadcasting system in 4k to 8k. In the image processing domain, image coding and decoding are the efficient methods which helps to eliminate the redundant information from the raw-data which is the top most priority and it is highly considered in all major applicatory area. In IC scheme, the primary goal is to perform compression without degrading the original image quality and conduct encoding operation. The transform based downward image data translation scheme is implemented [32] with the aim by discarding the high frequency elements from the transformed image. In this experimental study, authors adopted the interpolation direct filtering compression technique and quantization scheme, resulting the lower compression distortion for image pixels. Also demonstrated the coding mechanism which can achieve the high quality image pixels over the prior compression mechanisms. The paper [33], introduced a novel algorithm of sub-pixel text image for smart devices. This technique achieved high performance compared from other conventional IC standards including JPEG, JPEG-2000, H.264 and HEVC compression because the proposed approach compresses the three sub-pixels simultaneously whereas the conventional standards have main coding tools that handle the three color components independently.. However, they do not take advantage of the correlation among neighboring sub-pixels caused by sub-pixel rendering in a text image. This correlation is available only for a text image displayed on a screen which displays red, green, blue sub-pixels in sequence. The paper [34] aims to exploit the algorithm and VLSI architecture of a worst-case driven display frame compression. By using a prediction-and compression framework and a semi-fixed length coding scheme, the proposed design can achieve the much better balance between compression efficiency and throughput, and substantially reduce the bandwidth requirement and energy consumption of external memory system in the meanwhile. Extensive experiments demonstrate that the proposed display frame compression achieves 5.7 dB Peak Signal-to-Noise Ratio improvement, 3.1% compression ratio reduction, 3× throughput and 66.4% hardware cost saving, compared with the best previous work. In addition, the proposed VLSI design can support the throughput of 4K×2K@60Hz and reduce at least 17.6% energy consumption of external memory system by exploiting dynamic voltage and frequency scaling, compared with conventional display frame compression works. The work carried out by Kim et al. [35] presented a different implementation design considering improved 1D-SPIHT. The authors have modified the algorithm to obtain evaluation of the bit stream length before performing decoding. However, the study has also used optimization mechanism, to improve performance of compression efficiency. In the same way the study of Jin and Lee [36] also introduced modified version of SPIHT techniques as block-oriented pass-parallel-(BPP) approach. The main principle is that BPP-SPIHT decomposes a WT-image within 4×4 blocks and at the same time all the bits are encoded in the bit-plane of a same block size (i.e. 4×4).

Table.1. Summary of the above literatures

Authors	Problem	Methodology	Results	Limitations
Lee and Kim [21]	Energy conservation for IoT based multimedia applications	2D DWT and adaptive line prediction	Improves the compression ratio of high-frequency data, achieve a compression ratio at 4:1 with PSNR of 40-dB	Transmission error
Chen et.al [22]	Hardware based IC algorithm, Reduce the energy consumption rate during IC operation	Digital and block truncation coding methods	Reduce the power consumption rate at 53%.	Requires a one-line-buffer memory

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Adil & Kamil [23]	To design optimal IC system	ANN	efficiently compressed the image data	Only applicable for medical image data
Chiung et. al [24]	To design a hardware based lossless color IC technique	JPEG -LS	maintain the high performance	Not benchmarking
Miguel et. al [25]	To introduce a color image transform scheme	"Mosaic optimization"	achieved the PSNR upto 0.9 dB and 1.1 dB	**Nor benchmarking**
Wang et.al [26]	To design an efficient hardware based IC architectures	" Line-buffer using fixed length code "	improves the compression ratio even also fulfills the specific demands in line-buffer hardware architecture design	**Not benchmarking**
Halawani et. Al [27]	To Define area, Energy-efficient design and Speed	2D-DWT and Har wavelet	PSNR, SSIM, and CW-SSIM	Only suitable to hardware implementation
Choi et.al [28]	To design a high-throughput hardware device for IC	Haffman coding	Achieved 40% IC ratio	**Not benchmarking**
Jui et.al [29]	To introduce a VLSI hardware based architecture design	DWT algorithm	High computation speed, low power, less coding time	Only applicable for ECC compression
Kaur et.al [30]	The super-pixel based on chip circuit design	Wavelet transform and Deep convolution neural network	PSNR-30.9, SSIM-0.908, and 70% improvement in neural image compression	requires a super-pixel detection circuit
Onishi [31]	To design a single chip video encoder LSI architecture	HEVC encoding	Maintain the real visual quality	Need more improvement
Zhu et.al [32]	To design improved TDDC coding method	Compression dependent-TDDC coding method	Offers high quality reconstructed image samples	Image blocking is mandatory
Kim et.al [33]	To design an IC algorithm	Sub pixel text image compression algorithm	Achieve high compression ratio	**Not benchmarking**
Chen [34]	VLSI architecture for IC	Compression and semi-fixed length coding scheme	Balance the compression efficiency and throughput, less bandwidth and low energy consumption	**Not benchmarking**

VI. RESULT & FINDINGS ON THE BASIS OF ANALYSIS AND EVIDENCES

This section discusses about the finding of presented based on the observation analysis and Evidences.

Table 2 Observational Analysis

Design	Existing Techniques		
	[29]	[35]	[36]
Application	ID	ID	ID
Block-size	1024×1	64×1	4×4
Gate-Count (Kilo gate)	134.2[2]	68.08	14.05
Operating Frequency	434	167	110
Process (nm)	90	130	130
Normalized Operating Frequency 1(MHz)	434	241	159
Quality-Control Capability (PRD_T)	v	×	×
Power (μW)	24.4	-	-

Table 2 presents analysis considering comparative analysis of few existing techniques to show the scope of research towards image compression using hardware design. Based on the above discussions it has been analysed that SPIHT is an extensively considered compression technique for wavelet-transformed images. However it is associated with on the big disadvantages i.e. requires too much computation, thereby results in slow processing speed because of its dependency dynamic operation is on the image content. The exploration of literatures in hardware based information compression shows that there are few efforts have made using VLSI and FPGA based implementations. However, the critical findings show that the traditional approaches mostly incorporate complex design but do not emphasize much about selection of appropriate parameters and functions which can enhance the computational performance. The research work mention in table 2 has focused on similar task i.e. associated with the improvement of performance in the design of hardware based compression scheme. In this, it can be analysed that the high-speed, and low-power characteristics of existing SPIHT decoder design is compared and analysed. The design approaches presented in techniques mention table-2 can minimize size of VLSI of SPIHT decoding, thereby achieving the compact design goal of mobile devices.

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The performance improvement is due to our hardware-oriented algorithms and cost-effective VLSI architecture. However, huge research gap still exists as there are no adequate design approach, which clams better compression process with lower processing time. Therefore it is highly recommended, that there are requirements of more efforts by the researchers based on the identified gaps mentioned in the next sections.

VII. OPEN RESEARCH PROBLEMS

The proposed paper provides an overview about the existing image compression algorithms. However several compression techniques were developed over the years. In this section, open research gap based on the above-mentioned literature study will be discussed, which need to be addressed by further research.

The demand for effective image compression technology is increasing because the raw image requires a large amount of storage, which is a one of the major disadvantage in the transmission and storage process. However, many compression techniques already exist, an improved technique that is faster, cost-effective, and memory efficient, is definitely better for the user.

- For present-time application, various DWT based VLSI designs are presented with lift-based scheme which saves multipliers and adders, but it does not reduce complexity.
- It has also been observed that few image compression mechanism uses 2nd generation image coding like pyramidal coding, direction decomposition and vector quantization.
- However, such methods are associated with the entropy coding process, which is computationally not efficient and time consuming which makes computationally head to implement in a hardware-based environment.
- It has also been observed that most of the prior studies are followed repeated pattern. Therefore, there is not much discussion of the prior art in terms of parameters which is also a important concern towards implementing efficient compression technique.
- It can also be seen that most existing studies have not yet been benchmarked.

In addition, simulation and other evaluation tools are a tremendous choice. A problem occurs when attempting to measure the performance of one system with another existing system and both are implemented in different computing tools. In addition, the performance of the current approach should be evaluated on the same implementation tool.

VIII. CONCLUSION

Now days, image compression techniques like JPEG-2000, DWT and Haar wavelet transform algorithms are mainly utilizing in many applicatory area including medical, surveillance, and many research fields. The primary idea behind this process is to reduce the redundant image pixels form original image in order to transmit with high quality information. In this regards several research papers invented a solution of FPGA architectural mechanisms and provided effective solution, but they include various computation complexity issues. Therefore, this paper critically analyze the paradigms of research studies towards image compression with respect to hardware design and highlighted significant research challenges which needs to be improve or resolve for future application design.

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