Three Level Inverter Controlled UPFC for Harmonic Reduction using Space Vector Pulse Width Modulation Technique

R. Jayachandra, G. Tulasi Ram Das

Abstract: Unified Power Flow Controller (UPFC) is one of the most important device in FACTS family, this device in this work is used for power quality improvement. In this paper three level inverter is proposed for UPFC for the reduction of harmonics and for the enhancement of power transfer capability. SVPWM technique decides switching pattern of three level inverter. Therefore, in this paper this method is applied for controlling the three level inverter output. The proposed method is applied on four bus system and results are compared with UPFC without three level inverter. Results demonstrated that the proposed method effectively decreases the harmonics and increasing the power transfer capability.

I. INTRODUCTION

Now a day’s power quality is the major problem in an interconnected power system. In an interconnected power system the power transfer through transmission lines can be increased by using FACTS devices without violating the limits. UPFC is one of the versatile device in facts family. UPFC can be operated independently and simultaneously for controlling the power flow effecting parameters like impedance, voltage and phase angle. This device not only used for power transfer, it can be used for angle stability and also voltage stability. Voltage stability involves maintaining the voltage within the acceptable limits and harmonics elimination. Conventional UPFC consist of two transformers, two voltage source inverters and dc link capacitor. In conventional UPFC harmonics are more because of voltage source inverter [1-3]. On the other hand multilevel inverters are used for reducing harmonics.

Different types of multilevel inverters are Diode clamped, flying capacitor and cascaded. Because of number of advantages with Cascade Multilevel inverters over other, In most of the applications cascaded Multilevel inverters (CMLI) were used [4-7]. The performance of CMLI depends on pulse generation pattern. Different types of Pulse width modulation (PWM) techniques have been developed for reducing the total harmonic content. SVPWM technique is considered as a best method of generating pulses for Cascaded multilevel inverter because of better fundamental output voltage, reduced THD and easy to implement[8-11].

In this paper space vector pulse width modulation technique is used for generation of pulses to Unified power flow controller voltage source inverter.

II. IMPLEMENTATION OF ROPOSED METHOD

Space vector pulse width modulation technique implementation involves three stages [12-15]:

Stage 1: calculation of \( V_d \), \( V_q \) and angle \( \alpha \)

\[
V_d = \left( \frac{2}{3} \right) \begin{bmatrix}
1 & -1 & -1 \\
0 & \frac{2}{\sqrt{3}} & -\frac{2}{\sqrt{3}} \\
0 & 2 & 2
\end{bmatrix} \begin{bmatrix}
V_{an} \\
V_{bc} \\
V_{cn}
\end{bmatrix}
\]

\[
|V_{ref}| = \sqrt{V_d^2 + V_q^2}
\]

\[
\alpha = \tan^{-1}\left( \frac{V_q}{V_d} \right)
\]

Where \( V_{an} \) = phase A voltage \( V_{bn} \) = phase B voltage \( V_{cn} \) = phase C Voltage

\( V_d, V_q, V_{ref} \) and \( \alpha \) are calculated by using equations 1 to 3.

Stage 2: Time duration calculation \( (T_1, T_2, T_0) \)

\[
T_z \cdot |V_{ref}| \cdot \left[ \frac{\cos(\alpha)}{\sin(\alpha)} \right] = T_1 \cdot \frac{2}{3} V_{dc} \cdot \left[ 1 \right] + T_2 \cdot \frac{2}{3} V_{dc} \cdot \left[ \frac{\cos\left(\frac{\pi}{3}\right)}{\sin\left(\frac{\pi}{3}\right)} \right]
\]

\[
T_1 = T_Z \times a \times \frac{\sin\left(\frac{\pi}{3} - \alpha\right)}{\sin\left(\frac{\pi}{3}\right)}
\]

\[
T_2 = T_Z \times a \times \frac{\sin(\alpha)}{\sin\left(\frac{\pi}{3}\right)}
\]

\[
T_0 = T_Z - (T_1 + T_2)
\]
Where $T_z = \frac{1}{f}$

$$a = \frac{V_{\text{ref}}}{\frac{2}{3} V_{dc}}$$

For sector 1 switching time durations are calculated using the equations 4 to 6.

$$T_1 = \frac{\sqrt{3} \cdot T_z \cdot |V_{\text{ref}}|}{V_{dc}} \sin\left(\frac{n \cdot \pi}{3} \cos(\alpha) - \cos\left(\frac{n \cdot \pi}{3} \sin(\alpha)\right)\right)$$

$$T_2 = \frac{\sqrt{3} \cdot T_z \cdot |V_{\text{ref}}|}{V_{dc}} \sin\left(-\frac{n-1}{3} \cos(\alpha) + \cos\left(\frac{n-1}{3} \sin(\alpha)\right)\right)$$

$$T_0 = T_2 - (T_1 + T_2)$$

Where $\alpha = 0$ to 60 degrees.

$n$ = no of switching states (6 for three level)

For any sector switching times are calculated by using equations 7 to 9.

**Stage 3: Calculation of switching time for switches (S1 to S6)**

<table>
<thead>
<tr>
<th>Sector</th>
<th>S1, S3, S5</th>
<th>S4, S6, S2</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>$S_1 = T_1 + T_2 + \frac{T_0}{2}$</td>
<td>$S_2 = T_1 + T_2 + \frac{T_0}{2}$</td>
</tr>
<tr>
<td></td>
<td>$S_3 = T_2 + \frac{T_0}{2}$</td>
<td>$S_6 = T_1 + \frac{T_0}{2}$</td>
</tr>
<tr>
<td></td>
<td>$S_5 = \frac{T_0}{2}$</td>
<td>$S_4 = \frac{T_0}{2}$</td>
</tr>
<tr>
<td>II</td>
<td>$S_1 = T_1 + \frac{T_0}{2}$</td>
<td>$S_2 = T_1 + T_2 + \frac{T_0}{2}$</td>
</tr>
<tr>
<td></td>
<td>$S_3 = T_1 + T_2 + \frac{T_0}{2}$</td>
<td>$S_6 = \frac{T_0}{2}$</td>
</tr>
<tr>
<td></td>
<td>$S_5 = \frac{T_0}{2}$</td>
<td>$S_4 = T_2 + \frac{T_0}{2}$</td>
</tr>
<tr>
<td>III</td>
<td>$S_1 = \frac{T_0}{2}$</td>
<td>$S_2 = T_1 + \frac{T_0}{2}$</td>
</tr>
<tr>
<td></td>
<td>$S_3 = T_1 + T_2 + \frac{T_0}{2}$</td>
<td>$S_6 = \frac{T_0}{2}$</td>
</tr>
<tr>
<td></td>
<td>$S_5 = T_2 + \frac{T_0}{2}$</td>
<td>$S_4 = T_1 + T_2 + \frac{T_0}{2}$</td>
</tr>
</tbody>
</table>

**TABLE 1**

**III. TEST SYSTEM & RESULTS**

Four Bus systems shown in fig.1 is taken for testing the effectiveness of the proposed method.

**Fig.1 Test system**

**Fig.2 Simulation diagram of SVPWM three level UPFC**
Fig. 3 MLI based UPFC internal structure.

Fig. 4 SVPWM Pulse Generation Pattern.

Fig. 5 Three level inverter of UPFC.
Fig. 5 shows pulse generating pattern of SVPWM technique, these pulses are generated based on the equations 7 to 9 provided. The respective phase voltages of all phases are shown in fig.6 to fig.8. FFT analysis for line as well as phase voltages is shown in fig.9 and 10.

Fig. 6 Pulse generations for switches S1-S6 with respect to time.

Fig. 7 phase a voltage of three level inverter
Three level Inverter controlled UPFC for Harmonic Reduction using space vector pulse width modulation technique

Fig.8 phase b voltage of three level inverter

Fig.9 FFT analysis of phase voltage with three level inverter for UPFC

Fig.10 FFT analysis of Line voltage with three level inverter for UPFC

Fig.11 Real power with respect to time with three level inverter for UPFC

Fig.12 Reactive power with respect to time with three level inverter for UPFC
Fig.13 Real power in Lines with respect to time with three level inverter for UPFC

Fig.14 Reactive power in Lines with respect to time with three level inverter for UPFC

Table 2 indicates real and reactive power flow through line 1 with and without Three level inverter of UPFC.

<table>
<thead>
<tr>
<th>TABLE 2</th>
<th>REAL &amp; reactive POWER FLOW WITH AND WITHOUT MLI</th>
</tr>
</thead>
<tbody>
<tr>
<td>P(MW)</td>
<td>Q(MVAR)</td>
</tr>
<tr>
<td>UPFC Without MLI</td>
<td>970</td>
</tr>
<tr>
<td>UPFC With MLI</td>
<td>980</td>
</tr>
</tbody>
</table>

IV. CONCLUSIONS

The effectiveness of the proposed method is tested on four bus system. From figures 6 to 12 and table 2, we concluded that Three level inverter model of UPFC increases power flow and decreases total harmonic distortion in the power system. Therefore, svpwm based three level inverter of UPFC is better than without three level inverter.

REFERENCES


AUTHORS PROFILE

R. Jayachandra, has obtained his M.Tech degree from JNTU hyderabad. He has more than 10 years of teaching experience. He published 4 research papers at National & International level. He is presently a research scholar at JNTUH,Hyderabad., Telangana. He is working in the area of FACTS Controllers & Algorithms.

Prof. G. Tulasi Ram Das, has obtained his M.E from Osmania university and Ph.D from IIT Madras. He has more than 30 years of teaching experience. He has published 151 research papers at National and International level. His research area is Industrial Drives, FACTs devices.Telangana, India.