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The Design of Low-Power High-Speed Two-Level Three input XOR gate

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Abstract*: The Large Fan-In and high performance gates are essential to make portable electronic devices. In this paper an efficient realization of three input two level XOR(Exclusive-OR) is presented. The design of low power and high speed proposed XOR gate involves the combination of pass and transmission gates. The main objective to achieve this is based on the selection of input signals to propagate and maintain the good logic swing. Two methods were used to design proposed XOR, one (i.e. Pass_gate) is purely based on pass transistors with 8 MOSFET's and second method(Modified_Pass_gate) uses transmission gates with 12 transistors. The Modified_Pass_gate offers 86.14% and 6.66% of power dissipation reduction compared to static and Pass_gate XOR respectively and 77.18% and 50.94% less propagation delay compared to static and Pass_gate XOR respectively, at the supply voltage of 0.7v with input signal frequency of 3GHz. The simulation is performed based on 32nm technology node(PTM-models) using Hspice Synopsis simulation tool.

Keywords: Compound gate, Low-Power CMOS, Pass-transistors, Restoration logics, Static gate, Transmission gate.

I. INTRODUCTION

Now a day's the continuous growth of scaling of integration leads to the requirements of low power, high performance arithmetic circuits, which are predominantly used in portable devices and today's advanced VLSI chip design [1], [2], especially applications like Artificial Intelligence and Internet of Things (IoT). The performance parameters which are influencing the low power dissipation is govern by the fundamental power equation as shown in following.

$$P_{dyn} = V_{dd}^2 \cdot f_{clk} \cdot \sum_n \alpha_n \cdot c_n + V_{dd} \cdot \sum_n i_{sc_n}$$

Various parameters are influence the dynamic power which are power supply(Vdd), frequency of input signal, internode capacitances, activity of switching and Short circuit current.

Therefore, these parameters are responsible for reduced power dissipation. It is evident that primarily the low power circuit depends on how one can implement the circuit which is also called as the type of logic style. Let us see the influence of logic style on low power requirements. The downsizing of transistor reduces the internal node switching capacitance which is possible by choosing the best possible logic style. Moreover, functionality of the circuit should not be degrading because of voltage scaling. Therefore, it is noticed that the chosen logic style must be robust for downsizing of transistors and supply voltage scaling. The supply voltage and the logic style are related indirectly in terms of critical signal paths. The type of realization of a logic function influence the switching activity of the circuits. It is observed that the dynamic realization has more activity than static realizations [2], [3]. The input signal slopes and transistor sizing are strongly effects the short circuit current. The reduction in short circuit current is possible by giving steep and balanced input signal slopes. A good logic style allows decoupling of input and outputs of the logic gates, good driving capability and full signal swings so that it is easy to use and work reliably. Thereby for cell based designs functionality and synthesis of logics are mostly depending on these properties [3]- [4].

Rest of the paper is organized as follows: Session-II discuss about overview of logic styles necessary for design, the design of three input XOR is explained in Session-III and Session-IV mention the simulation setup and result discussion, finally in Session-V conclude the paper.

II. OVERVIEW OF LOGIC STYLES

A. Static CMOS

The Static CMOS logic implementation of digital integrated arithmetic circuits offers low static power and best choice for power efficiency, it also observes the high propagation delay compared it its counterparts [4]. The construction with pull-up and pull-down networks of static realization actually leads to low power constraints. The pull-up network drags the output to logic high value whereas pull-down network pulls down the output node to logic low level. The general construction of static CMOS is shown in Fig.1.1(a). In general, pMOS FETs for Pull-up network and nMOS FETs for pull-down network are used. For example, the static CMOS NAND and NOR gate are shown in Fig.1.1(b) and Fig.1.1(c) respectively. This implementation promises the very low static power since at a time only one network is active to obtain the output signal and good noise margin but requires more number of transistors if the fan in of the digital circuit increases. It is possible to reduce the number of transistors by taking two level realization of large fan in circuits. It is noticed that the input capacitance and propagation delay of the circuit will increases.

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B. Pass Transistor Logic(PTL)

Another way to realize the logic circuits by using Pass Transistor Logic(PTL) as shown in Fig.1.2. The one input is applied at 'A' and other input is at 'B', signal 'Y' is taken as output. It is more attractive to circuit realization in terms of utilization of less number transistors [7]- [10].

It is observing that inputs are not only applied at gate terminal of MOSFET but also at the source/drain terminals of transistors therefore it is also called as gate no-restored logic implementation. there is a serious problem inherent to the pass gate logic is that it suffers from threshold problem. For example, let us consider nMOS transistor and apply logic high at gate terminal as well as source/drain terminal it is observe that only (VDD-Vth) is the output signal strength after that the nMOS enter into cutoff region.

Similarly, the maximum output voltage of pMOS transistor is Vtp. Hence pMOS is good for logic high Signal passage but bad for logic low signal whereas nMOS is good for logic low and bad for logic high. Therefore, the maximum output voltage for pass gate realization suffers from signal strength. This problem is solved by different methods.

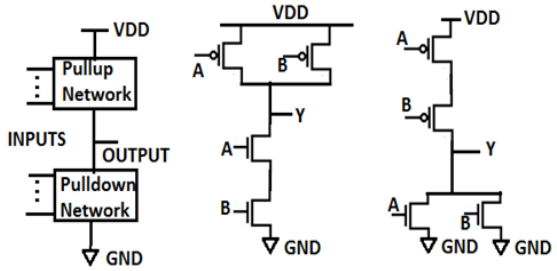

Fig.1.1 (a) Structure of a CMOS gate. (b) CMOS-NAND. (c) CMOS-NOR.

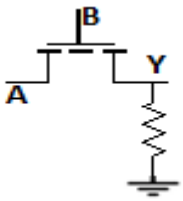

Fig.1.2 Pass Transistor

C. Transmission Gate Technology(TGL)

The threshold problem of pass gate implementation can be eliminated by the Transmission Gate Technology(TGT). The circuit diagram and circuit symbol is shown in Fig.1.3(a) &(b) respectively. It is observed that the parallel connection of nMOS and pMOS transistors gives the best possible combination to encounter the swing loss problem [10]- [11]. The electrical properties of TGT is shown in Fig.1.3(c). If the input is Logic High, then pMOS will give a chance for the input signal pass through it because it offers less resistive path for logic high whereas for the signal of logic low will choose the nMOS transistor path where it finds the low resistive path for active low signals.

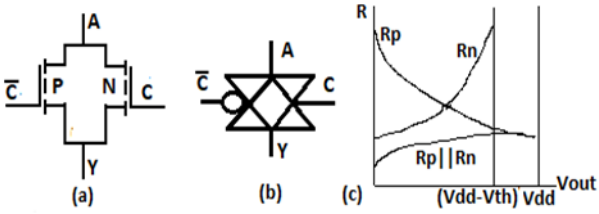

Fig.1.3 (a) TG Circuit (b) Circuit Symbol (c) Resistance characteristics of TG

Therefore, the threshold problem is easily eliminated by the TGT method. The transistors count increase but not more than that of conventional Static CMOS logic implementation.

III. DESIGN OF THREE INPUT EXCLUSIVE-OR GATE

The exclusive OR gate is a fundamental building primitive for adders which are mostly used in almost all the arithmetic circuits [5]. The efficient realization of high Fan-in XOR gate defines the performance of digital circuits like adders, magnitude comparators etc. in this section we discuss about the design of three input gate. The block diagram and functional table is shown in Fig.2.1(a), (b). The conventional approach to implement three input static XNOR gate is by using 2 two input XNOR gates, that means it uses two level circuit as shown in the Fig.2.2(a). the realization of the two input XNOR gate is shown in Fig.2.2(b). It observes from the Figure that the propagation delay of the three input XOR gate using two level method will increase as well as this implementation prone to glitch problem. Therefore, with the help of Pass gate and Transmission gate methodology it is possible construct three input XOR effectively by avoiding the completed input to propagate through pass transistors and attain the good logic swing (i.e. reduce the threshold loss problem).

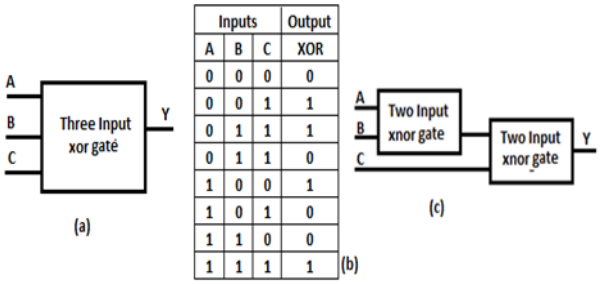

Fig.2.2 (a) Block diagram (b) Functional Table (c) Two level Three input XOR gate

The design of XOR gate is based on XNOR theory because it produces the strong output like static gate**.**

The logical expression that governs the functional table is as shown follows

$$Y(A,B,C) = \sum m(1,2,4,7) \quad \text{---(2)}$$

Where m=minterms, these are observed for the input combinations 1, 2, 4 and 7.

Equation (2) can be written as based on the two input XNOR gates as follows

$$Y(A,B,C) = (A \odot B) \odot C \quad \text{---(3)}$$

$$Y(A,B,C) = (AB + A'B') \odot C \quad \text{----(4)}$$

$$Y(A,B,C) = (AB + A'B')\,C + (A'B + AB')C' \text{----(5)}$$
$$Y(A,B,C) = (ABC + A'B'C) + (A'BC' + AB'C') \text{---(6)}$$
$$Y(A,B,C) = A'B'C + A'BC' + AB'C' + ABC \text{---(7)}$$

The best way to choose the input signal as a propagate and control signal is shown in Table-1

Table-I: Choosing control signals

Functions	Control signal
X'Y	X should be
X'+Y	X should be
XY	X or Y
X+Y	X or Y
X'Y'	X or Y
X'+Y'	X or Y

For example, From the table if any function having the possibility shown. we choose complemented signal as control signal whereas Un-complemented signal as propagate signal.

A two input XNOR is implemented by using 12 transistors in static CMOS approach whereas only 4 transistors in method-1 and 10 transistors in method-2. The transistor circuit realization of 2-input XNORS are shown in Fig.2.3(a) & (b).

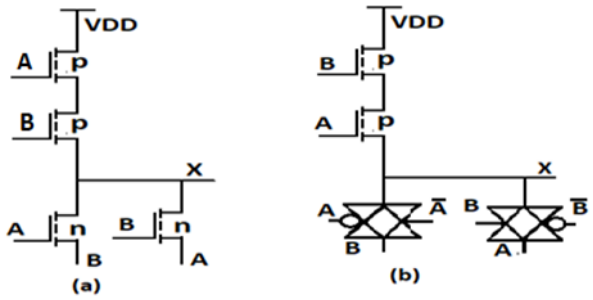

Fig.2.3 2-input XNOR (a) Method-1 (b) Method-2

In method-1 the functionality is as shown in the Table-II From the table it is noticed that all input combinations except '11' the gate produces good logic levels but last input combination gives the bad logic High value thereby this leads to glitch power in gate. The problem of bad signal strength is encountered by method-2 where we used the transmission gate at the associated palaces as shown in the Fig.2.3 (b). The complemented inputs are applied at gate terminal of pass gates so that the propagate signal could be the un-complemented signal.

Table-II functionality of 2-input XNOR

Inputs		Output	comment
A	B	YXNOR	
0	0	1/Vdd	Strong Logic High
0	1	0/A	Good Logic Low
1	0	0/B	Good Logic Low
1	1	1/A or B	Bad Logic High

Therefore, the switching power will be reduced drastically. But more number of transistors are requires compared to method-1. The three input XNOR gate is shown in Fig.2.4(a) &(b).

The input signal "**C**" considered to be propagate signal since this input signal transitions are more compared to other input signals (**B**, **C**). Therefore, we will measure the accurate results related to critical path delay and power dissipation.

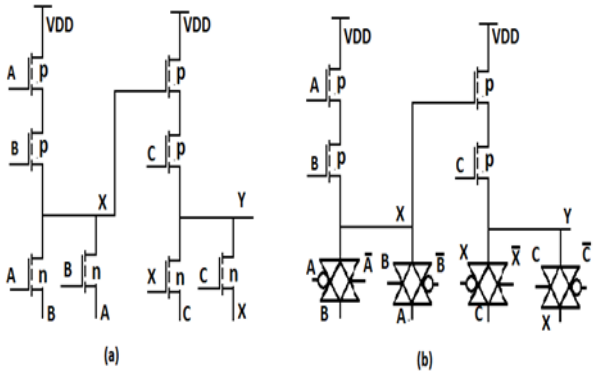

Fig.2.4 Three input XNOR (a) Method-1 (b) Modthod-2

IV. SIMULATION RESULTS AND DISCUSSION

H-spice is used to simulate the design at various supply voltages like 0.7v, 0.8v, 0.9v, 1.0v and 1.1v. The PTM model parameters are taken in to considerations under 32nm technology [12]. The measured date of power dissipation and delay are taken from H-Spice tool. The Power Delay Product (PDP) is calculated the based on arithmetic multiplication. All circuits are simulated with varying frequency of 0.5GHz, 1GHz, 2GHz, and 3GHz at a temperature of 25° C and the average power/delay is calculated and presented in each case. The Ln=Lp=32n, and Wn=48n and Wp=64n for fare estimation of proposed gate sizing. The two level design of static gate prone to glitch problem so to avoid this we used hazard filtering technique where without effect the critical path signal delays, output size logics are modified at their aspect rations. The W/L rations of static gate at the output size is increased by 2 times than that of proposed gate. Therefore, the buffer gates are having Wnp (width of proposed nMOS) =32n and Wpp (width of proposed pMOS) = 64n, similarly Wn= 128n Wp=128n for static gates.

A. Simulation Wave form

The simulation wave form is shown in Fig.3.1 for all possible input combinations.

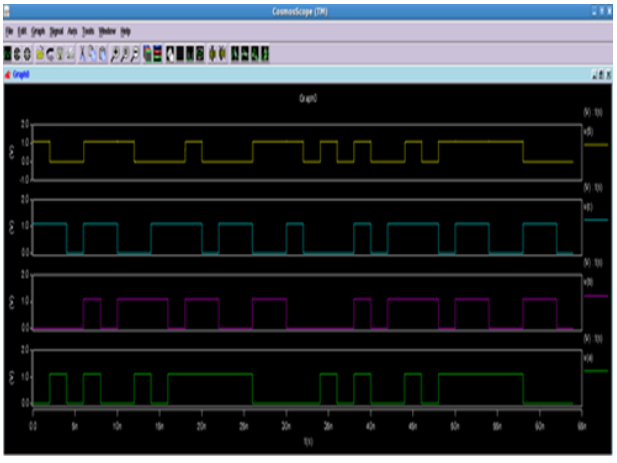

Fig.3.1 Simulation wave form

B. Results discussion

The pass gate based power dissipation is compared to static XOR gate and found the following. The average percentage reduction of power dissipation for the input frequency variation of 0.5G to 3GHz at supply voltages of 1.1v, 1.0v, 0.9v, 0.8v and 0.7v as 42.84%, 52.78%, 63.18, 72.92% and 80.48% compared to static gate respectively. Especially it is observing that the input frequency variation of 3GHz and at 0.7 supply voltage, pass gate offers very low power dissipation of 85.15% compared to static XOR gate. Similarly, the transmission gate based XOR gate offers the low power dissipation compared to Static gate as follows. The average percentage reduction of power dissipation for the input frequency variation of 0.5G to 3GHz at supply voltages of 1.1v, 1.0v, 0.9v, 0.8v and 0.7v as 79.86%, 82.39%, 84.02%, 84.98% and 85.52% compared to static gate respectively. Moreover, at the supply voltage of 0.7v and frequency of 3GHz gives us the best reduction in power dissipation. It also observes that comparison is done between pass gate and transmission gate based XORs.

The average percentage reduction of power dissipation for the input frequency variation of 0.5G to 3GHz at supply voltages of 1.1v, 1.0v, 0.9v, 0.8v and 0.7v as 62.28%, 59.86%, 53.36%, 41.12% and 22.96% compared to pass gate XOR respectively. The transmission gate based XOR offers the low power consumption compared to pass gate XOR exclusively at 0.7v and at 3GHzinput signal frequency as 6.66%.

The propagation delay of static, pass gate based and Transmission gate based XOR is shown in Table-III, Table-IV and Table-V respectively. At the supply voltages of 1.1v, 1.0v, 0.9v, 0.8v and 0.7v, for the frequency of input signal 0.5G to 3G, average percentage of propagation delay reduction 82.56%, 82.80%, 53.36%, 70.79% and 56.05% respectively. Similarly, at the power supply of 1.1v, 1.0v, 0.9v,0.8v and 0.7v, for the frequency of input signal from 0.5G to 3G, the average delay reduction is about 76.78%, 77.26%, 77.07%, 76.715 and 77.06%. If propagation delay is compared between pass gate and transmission gate, it observes that at supply voltages of 1.1v, 1.0v and 0.9v delay is increased on an average by 33.16%, 32.21% and 10.24% respectively for all frequencies. Whereas at the supply voltage of 0.8v and 0.7v the transmission gate produces best average percentage propagation delay reduction by 20.12% and 47.67% compared to pass gate XOR. Especially the percentage power dissipation at 0.7v with .3GHz input signal produces 6.66% reduction but the percentage of propagation delay is decreased remarkably by 50.94%.

Finally, the product of power and delay is called PDP which defines the quality of gate. Therefore, at all supply voltages and at all frequencies the product is calculated. The percentage improvements are as shown follows. At the supply voltages of 1.1v, 1.0v, 0.9v, 0.8v and 0.7v, for the frequency of input signal 0.5G to 3G, average percentage of PDP reduction is 90.04%, 91.87%, 92.42%, 92.18% and 91.51% respectively. Similarly, at the power supply of 1.1v, 1.0v, 0.9v, 0.8v and 0.7v, for the frequency of input signal from 0.5G to 3G, the average PDP reduction is about 95.32%, 95.99%, 96.33%, 96.50% and 96.68%. The PDP's are compared between pass gate and transmission gate XORs, at the power supplies of 1.1v, 1.0v, 0.9v, 0.8v and 0.7v, for the frequency of input signal from 0.5G to 3G, the average PDP reduction is about 49.80%, 46.92%, 48.96%, 53.41% and 60.05% than pass gate XOR.

Therefore, it is evident that the PDP value of this transmission gate XOR is better compared to static gate and pass gate based XOR. Even though the delay of the transmission gate more compared to pass gate XOR, the PDP value is remarkable at the frequencies. For low power and high speed designs pass gates and transmission gate are best compared to static XOR gate. Moreover, the transmission gate has produced the good performance at the 0.8v and 0.7v supply voltages with all frequencies. Hence the proposed XOR works better in terms of power dissipation and reasonable operating speed.

C. Graphical Representation of comparisons

The graphical representation of comparisons is shown in the Fig.3.2 to Fig. 3.4

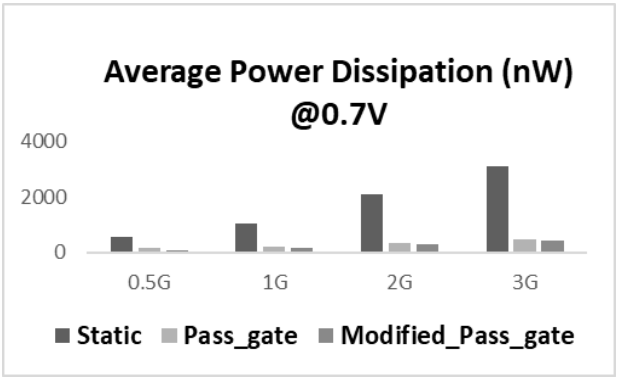

Fig. 3.2 Comparison of Average Power Dissipations at supply voltage of 0.7v

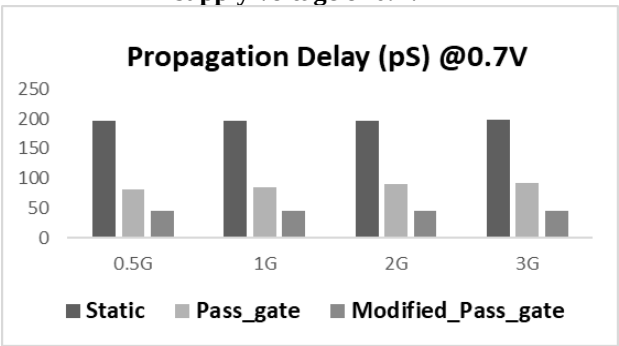

Fig. 3.3 Comparison of Propagation Delay at supply voltage of 0.7v

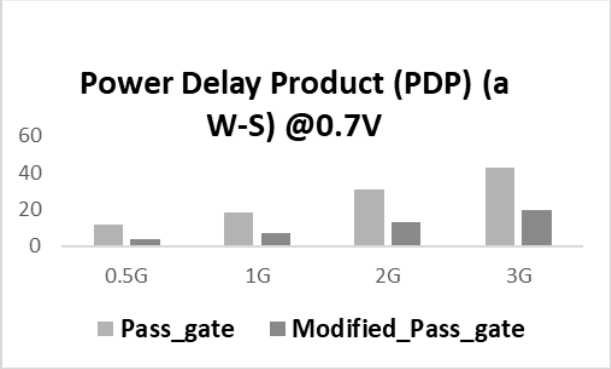

Fig. 3.4 Comparison of PDP's at supply voltage of 0.7v

Table-III: Simulation results of Average Power Dissipation and propagation delay of Static gate

Static XOR gate	Average Power dissipation(nW)					Propagation Delay(pS)				
	1.1V	1.0V	0.9V	0.8V	0.7V	1.1V	1.0V	0.9V	0.8V	0.7V
0.5G	1977.4	1399.4	1018.9	753.7	545.8	69.14	82.18	100.9	131.3	197.2
1G	3362.5	2511.6	1909.8	1433	1057.4	69.13	82.18	99.72	130.9	197.2
2G	6133.6	4750.7	3679.2	2807.9	2079.7	69.09	82.17	99.62	130.7	197.2
3G	8978.9	7042.7	5490.1	4201	3124.5	69.03	82.16	99.53	131.1	198.7

Table-IV: Simulation results of Average Power Dissipation and propagation delay of Pass gate

Pass XOR gate	Power dissipation(nW)					Propagation Delay(pS)				
	1.1V	1.0V	0.9V	0.8V	0.7V	1.1V	1.0V	0.9V	0.8V	0.7V
0.5G	1729.8	1005.6	558.2	291	142.8	12.03	14.13	19.89	35.93	80.38
1G	2113.1	1291.7	758.1	415.9	216.1	12.03	14.13	20.51	37.56	84.96
2G	2668	1713	1059	612.9	345.6	12.03	14.12	21.1	39.24	89.63
3G	3123.2	2080.9	1317.6	791.7	463.9	12.09	14.13	21.7	40.32	92.39

Table-V: Simulation results of Average Power Dissipation and propagation delay of transmission gate

Transmission XOR gate	Power dissipation(nW)					Propagation Delay(pS)				
	1.1V	1.0V	0.9V	0.8V	0.7V	1.1V	1.0V	0.9V	0.8V	0.7V
0.5G	499.4	295.9	186.9	124.1	84.2	16.07	18.66	22.92	30.5	45.33
1G	698.6	451	307.1	216.4	154	16.03	18.66	22.92	30.5	45.26
2G	1089.4	762.8	549.4	400.7	292.3	16.07	18.76	22.92	30.5	45.33
3G	1502.3	1075	799.3	597.2	433	16.01	18.66	22.89	30.5	45.32

Table-VI Power Delay Product Static gate

Static XOR gate	Power Delay Product(PDP)				
	1.1V	1.0V	0.9V	0.8V	0.7V
0.5G	136.73	115.01	102.81	98.947	107.65
1G	232.46	206.42	190.46	187.59	208.54
2G	423.78	390.41	366.56	367.07	410.21
3G	619.84	578.68	546.47	550.87	620.8

Table-VII Power Delay Product Pass gate

Pass XOR gate	Power Delay Product(PDP)				
	1.1V	1.0V	0.9V	0.8V	0.7V
0.5G	20.812	14.213	11.104	10.456	11.479
1G	25.424	18.257	15.551	15.621	18.362
2G	32.101	24.193	22.353	24.053	30.977
3G	37.779	29.415	28.597	31.923	42.86

Table-VIII Power Delay Product Transmission gate

Transmission XOR gate	Power Delay Product(PDP)				
	1.1V	1.0V	0.9V	0.8V	0.7V
0.5G	8.02	5.52	4.28	3.7855	3.81
1G	11.19	8.41	7.03	6.601	6.97
2G	17.50	14.31	12.59	12.223	13.2
3G	24.04	20.06	18.29	18.216	19.6

V. CONCLUSION

This paper has introduced an efficient implementation of three input XOR gate using pass transistors and transmission gates. The Modified_Pass_gate had an advantage of less number of transistors compared to static XOR and improved logic swings compared to Pass_gate. The glitch problem was eliminated by choosing appropriate signal to propagate, especially seen in two level circuit designs. Moreover, input capacitance is reduced for high Fan-in. A variety of comparative spice simulations were performed at 32 nm, verifying, in all possible input combinations at various frequencies and at different power supply values. From the simulation, it is evident that a definite advantage in favor of the proposed XOR gate designs. Especially, for the combination, at 0.7v and at 3GHz, the average power dissipation of Pass_gate and Modified_Pass_gate XORs were 85.15% and 86.14% less compared to static gate and 6.66% less power dissipation of Modified_Pass_gate compared to Pass_gate. But the Propagation delay of transmission gate based XOR (i.e. Modified_Pass_gate) is 50.94%lesscompared to Pass_gate at 0.7v supply voltage with 3GHz input frequency. Therefore, the proposed three input combinational gate is used in high performance arithmetic circuits and ASIC design.

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