International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-9 Issue-7, May 2020

Mathametical Modelling of Full Adder using Carbon Nanorods

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Abstract:Nanomechanical computational systems proposed by K.Drexler is one of the approaches to molecular scale electronic circuits for memory and logic applications. The nanomechanical rod logic proposed is distinguished by its small size and very low energy dissipation, compared to transistors. it has been found from the sources available to us, that presently the idea was highly unexplored and still remains in its nascent stages This paper presents the use of nanorods as variant to the existing silicon technology for the design of a full adder circuit along with the speed, power and energy dissipation characteristics. The full adder circuit is then extended to an n-bit adder (which forms the basis of an ALU circuit). The paper also addresses the use of parallel architectures to overcome the limitations of switching speeds.

Keywords: nanomechanical logic rods, full adder circuit, energy dissipation .

I. INTRODUCTION

Today the driving force for microelectronics is information technology. With the exponential growth of data and knowledge, the future will demand sophisticated microelectronics, probably nanoelectronics[8]. Evolutionary changes in CMOS have inspired research on several important topics including wire dominated designs, power dissipation and fault tolerance. A revolutionary technology change such as replacing a CMOS device, is a potentially disruptive event in the design of computing systems. Emerging technologies for further miniaturization have capabilities and limitations that can significantly influence computer architecture and require rebuilding abstractions originally tailored for CMOS. Even though such alternative technologies to silicon based technologies do not show any economic or computational importance as of now, they are still interesting research areas[8]. The paper discusses one such specific nanotechnology of "Nanomechanical computational systems"

Digital systems in nanomechanical computers are represented by displacements of solid rods and logic gates in combinational circuits can be built by using interlocks in nanomechanical systems. These interlocks can resemble CMOS transistors, in that interlocks can make the mobility of the rod dependent on the displacement applied to gate knob, either permitting motion when the gate knob is at a large displacement and blocking it at low displacements, or vice versa [1,2,3,4].

In this paper we build upon the logic suggested by K.Drexler and propose an approach for realizing a classical full adder circuit and its implementation using logic rods. In section 2 we present the architecture of an classical full adder circuit and then its extension to n-bit adders (multi-bit adder). This is followed by speed, packaging density and energy dissipation considerations based upon bounded continuum models, in section 3. Some of the problems arising from the use of these methods are also briefed. The concluding remarks are provided in section 4.

II. ADDER ARCHITECTURE

One of the challenges for nanoelectronics is the development of integrated circuits on the basis of emerging alternative technologies. For this purpose, we propose a full adder implementation using nanomechanical rods. There are several different ways to implement a such a circuit. In this section we consider the design of a basic full adder circuit using the equations (1) and (2) given in the references [9,10].The equation for the Sum S of traditional 1-bit full adder is:

$$S = A\overline{B}\overline{C_i} + \overline{A}B\overline{C_i} + \overline{A}\overline{B}C_i + ABC_i \qquad (1)$$

Where A and B are the inputs and C_i is the carry input.

The equation for output carry is:

$$C_O = A\,B + B\,C_i + A\,C_i \qquad (2)$$

Revised Manuscript Received on May 30, 2020.
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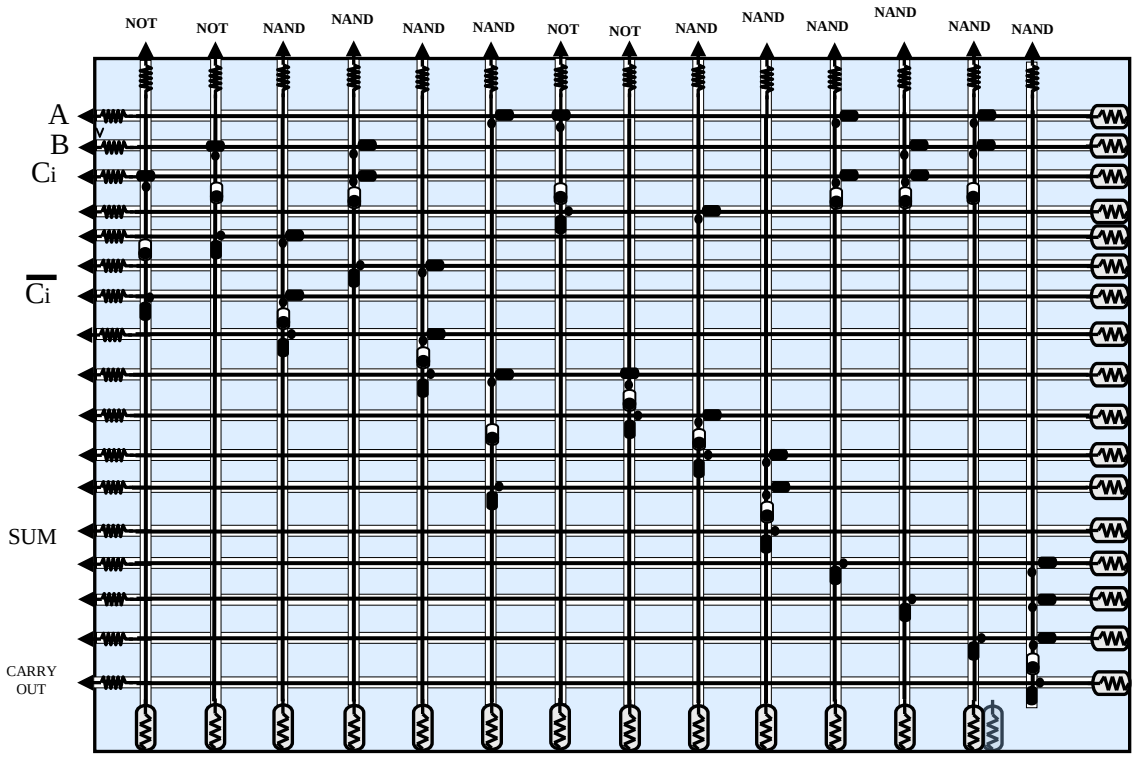

Fig. 1: Design of basic Full Adder using Nanomechanical Rods

The implementation of Eq.(1) and Eq.(2) using nanomechanical rod logic is presented in the fig1.

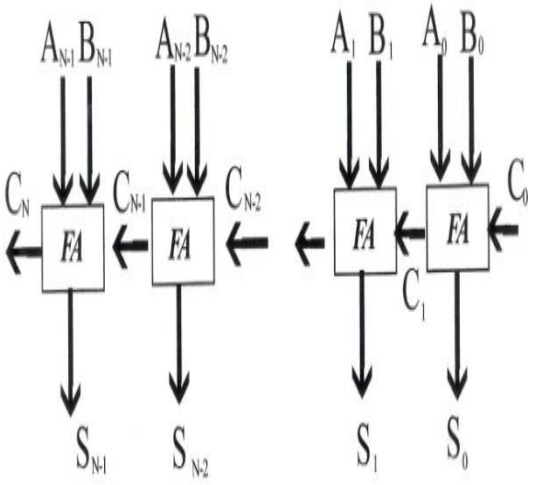

Fig. 2: N-bit Ripple Carry Adder

The proposed circuit is non optimized logic implementation of a full adder using logic rods. The circuit uses 14 vertical rods and 17 horizontal rods with each rod forming interlocks. The implementation forms a total of 39 interlocks for obtaining the sum and carry. The circuit in fig 1can be extended to form a n-bit ripple carry adder circuit as shown in the fig. 2

A second approach for realizing full adders is shown in the fig.4. The truth table of the adder can be analyzed by the following equations Eq.(3) and Eq.(4) given in the references[9]:

$$\text{if A=B then } S = C_i \text{ else } S = \overline{C_i} \qquad (3)$$

$$\text{if A=B then } C_O = \text{A else } C_O = C_i \qquad (4)$$

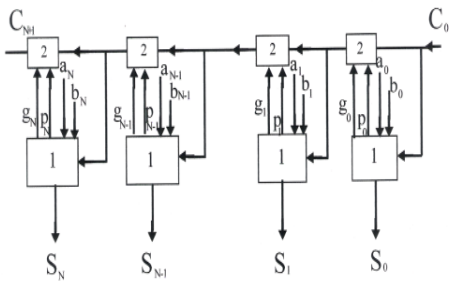

Fig. 3: Manchester Carry Adder

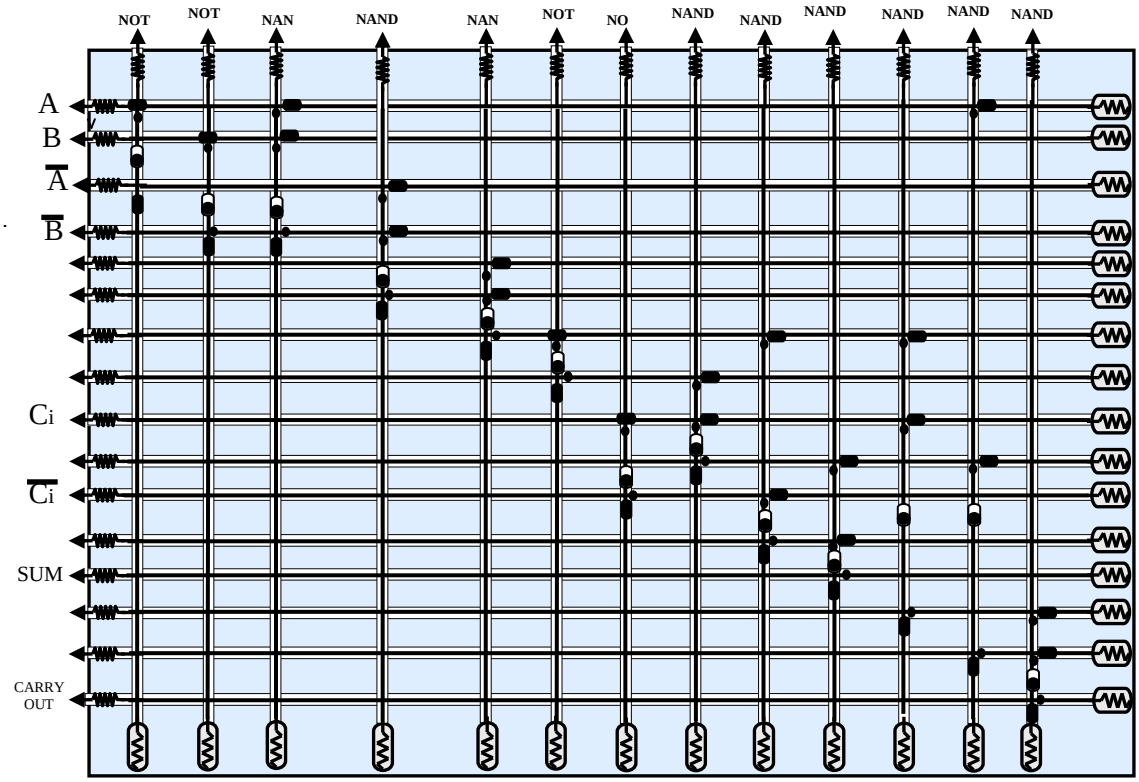

Fig.4 Design of a Manchester Carry Adder using Nanomechanical Rods

The logic implementation of the Eq.(3) and Eq.(4) involves the use of 13 vertical rods, 16 horizontal rods and 35 interlocks. The implementation of the above equations using pass logic is being studied. The above circuit can also be extended to form an n-bit adder circuit.

III. ADDER CHARACTERISTICS

To investigate the various performance parameters such as gate density, device size, speed and energy dissipation the following geometries are chosen for exemplar calculations[1] .These are given by the Eq.(5) :

$$l_{knob} = w_{knob} = w_{rod} = d_{knob} / 2 = 1nm$$
$$h_{knob} = h_{rod} = 0.5nm \qquad (5)$$

Using the geometric considerations defined in Eq.(5) the total volume of the adder including the housing structure was found to be 3588nm^3. The volume of individual interlock was found to be 16 nm^3. Hence the total volume of the interlocks present in the adder circuits approximately 640 nm^3. For assembling of these systems self replicating or self assembling architectures can be used [7].

The energy dissipation of the adder was thoroughly investigated. The energy dissipation in an adder (logic) circuit can mainly be attributed to: energy loss in interlocks, Vibrational energy loss, and energy loss due to sliding interface drag in the cam surfaces of the driver mechanism and thermo elastic losses. The overall energy dissipation as a cumulative effect of all these losses amounts to 71.062 x 10-21 J (or) 71.062 maJ.

A detailed account of individual energy losses is provided:

Energy loss per interlock:

Total energy loss per interlock per switching cycle= 0.013 maJ.

Total energy loss due to all the interlocks present in the adder circuit=0.52 maJ.

Vibrational energy loss:

Energy loss due to vibration in one rod = 0.56 maJ.

Total energy due to vibrations of rods in the adder circuit= 17.36 maJ.

Energy dissipation due to sliding interface drag in cam surface:

Energy dissipation per rod per 0.1ns = 0.012 maJ

Total energy dissipation in adder circuit = 0.372 maJ

Thermo elastic losses:

The thermoelastic losses for a probe segment are expected to be <0.41 maJ. Calculating the thermoelastic losses for the full adder circuit is expected to be around 15.17 maJ.

The delay of transmission of a signal in a rod of length 100nm was found to be 60ps and the switching time for an interlock was found to be 100 ps. Using the above exemplary calculations the time delay for an adder circuit was found to be approximately 0.66 ns.

The simulation results above are obtained at helium temperatures (0-4K). The results obtained in this section are an extension of the calculations and results obtained by Drexler [1] for a single gate. With regard to integration nanomechanical CPU scale systems containing 106 transistors like interlocks can fit within 400 nm3. In nanomechanical systems of sufficiently large sale, the ~1012W/m3 power dissipation density of ~1GHz nanomechanical logic systems exceeds any possible means of cooling [1,2].

To overcome the above limitations and speed constraints due to mechanical design, parallel architectures are one possible solution [9].

Reversible computer logic also present an appropriate solution to the above problem of energy dissipation and thermal noise [5,6]. The consideration of reversible rod logic is also one of our future research objectives.

IV. RESULTS

This paper investigated the performance of full adder structure using carbon nanorods, on various parameters like speed , power or energy dissipation and size. these results are summarized below in tabular format.

Table-I: Adder volume

Volume of individual interlock	$16nm^3$
Total volume of interlocks	$640nm^3$ (Approx)
Total volume of adder including housing structure	$3588nm^3$

Table-II: Energy Dissipation

Energy loss in interlocks	0.52maJ
Vibrational Energy Loss	17.36maJ
Energy Loss due to Sliding Interface	0.372maJ
Thermo Elastic Losses	15.17maJ

Table-III-Overall Results of Adder structure using Carbon Nanorods

Gate Density	$640nm^3$
Delay	0.66ns
Total Energy Dissipation	71.062maJ

V. CONCLUSIONS AND FUTURE RESEARCH

A Classical Full adder circuit was designed using nanomechanical logic rods and this circuitry was used to extend its operation to n-bit adder. Then the adder characteristics like packing density, energy dissipation and speed characteristics were presented. Another adder circuit design was also presented which makes use of pass-logic. The circuit delay is high when compared to CMOS as expected for nanomechanical rods. To overcome the fundamental limitations of speed, error tolerant architectures and energy dissipation considerations parallel architectures can be used for implementation. Such implementation would be one of our future research objectives. Our future research objectives would also include the detailed calculation of probabilistic error rates and optimization implementation design for effective implementation.

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