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# Analog based Neuromorphic Systems on Low Power Current Mode Circuits

**M. Parthasarathy, R. Sakthivel**

***Abstract:*** ***Neuromorphic computing is the process used to appliance the neural system models. Formerly, it is referred to as the biological process and later it turned out to be the computing algorithms. Many neuromorphic algorithms represented as the neural figures such as neural spikes, fluctuated graphs, and synapses. The biological nervous system for instance consists of huge number of neurons and they collectively work to encode the stimulus of various senses. In case of neuromorphic computing, automated brain brings in the concept of efficient work carried out through artificial means. The neuromorphic computing thus evolves as a major technological advancement and the need of such technique is the need of the hour in various scientific as well as field applications. In existing techniques, the scaling, power and area are not efficient. This study attempts to address the major issues such as scaling and power. This paper explains the design on a non-spiking network which is used for population coding architecture. The model which is discussed in this paper is based on the analog domain and the current mode circuits are also involved. The input neuron model consists of current direction selector block, current scale block and minimum current block which all comprise to form the neuron model. This paper also brings out the possible outcome of low power constraints. This paper involves 180nm technology with which the power is measured. This paper brings out the simulations of both 180 and 90nm technologies. Apart from current scale block, minimum current block and current direction selector block, there are other blocks such as current splitter block and current mode low pass filter block, where all the circuits work under the sub-threshold condition. The power consumption obtained in the 180 nm technology is 58.838 μW and its energy equivalent is 1.765pJ. Neuromorphic computing is used as an application where the machines are being automated and such machines come with self-thinking capability. Neuromorphic computing design which is evolved from this paper is found to be more power ad energy efficient. The tool used is Cadence Virtuoso.***

**Keywords:** ***Artificial Neural Network, Echo State Network, Spiking Neural Network, Trainable Analog Block.***

## I. INTRODUCTION

Before we get into the detailed discussion of deep learning, let us look into the short note on the artificial intelligence and machine learning. Artificial intelligence is the capability of a machine to replicate intelligent human being.

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Example for the artificial intelligence is self-driving cars and more. Artificial intelligence is accomplished by studying how human brain thinks and works, learn and make decisions while solving a problem [1]. The outcome rather is an intelligent software and systems. Machine learning is the process that provides the computer with the ability to learn without being overtly programmed. Machine learning is the subset of artificial intelligence. Some of the applications of artificial intelligence are speech recognition, understanding natural language and recognition of image. While deep learning is a part of machine learning. Deep learning uses neural networks to make decisions similar to the decisions made by the human brain. Machine learning is the learning process from the dataset that is training the data and testing the data. Some of the limitations of Machine learning are not useful with high dimensional data (large number of input and output), cannot solve Natural language processing (NLP), image processing, big challenge is feature extraction, such as object recognition or handwriting recognition. Deep learning models are able to focus on the right features by themselves, without the need of the human being. The idea behind deep learning is to prepare algorithms that mimic exactly as brain. Deep learning is implemented through neural networks (biological neurons). The neuron diagram is shown in Fig.1.

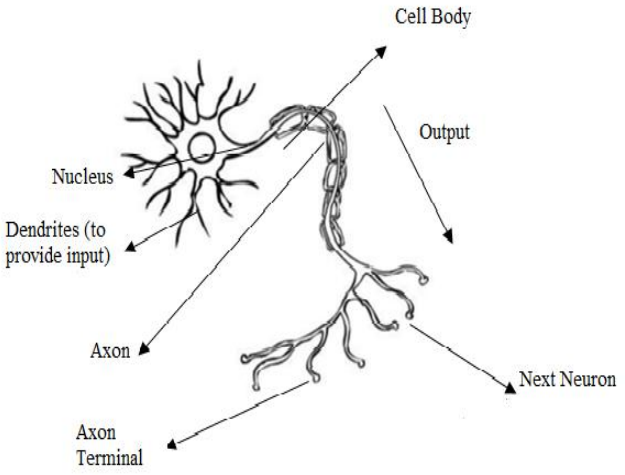


**Fig.1 Schematic of biological neuron [18]**

Two neuron never connect to each other, this gap of connection is called synapse. The transfer of current pulses between the neurons is discussed in this paper, how the current is transferred from the input to the output.

## II. OBJECTIVES

- This neuromorphic analog based system is carried out in sub-threshold condition.
- The low power consumption is made as an main objective to the circuit.
- The energy consumption is also an objective in this paper.
- The model here mentioned is of analog domain and current mode circuits.

## III. ARTIFICIAL NEURON

The artificial neuron is shown in Fig.2. The process is repeated as to get desired output. The process of updating weight is back propagation method. The applications of deep learning is self-driving cars and voice controlled assistance.

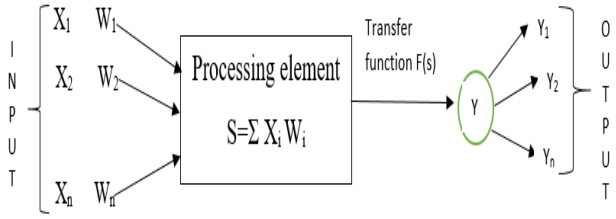


**Fig.2 Steps of Artificial neuron**

Training is initially done to the machine. There is this algorithm called perceptron learning algorithm which explains about the artificial neuron process. The steps involved in the perceptron learning algorithm is shown in Fig.3. In the output of the above algorithm, if the value is above threshold value it will give the output, else no output. The other name for the artificial neuron is perceptron.

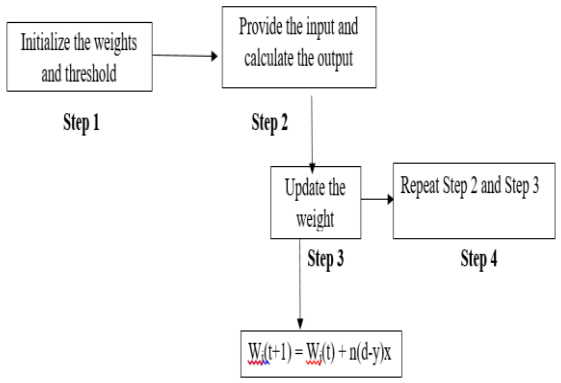


**Fig.3 Steps of Perceptron Learning Algorithm**

Machine learning is the subset of artificial intelligence. Some of the applications of artificial intelligence are speech recognition, understanding natural language and image recognition. While deep learning is a subset of machine learning. Deep learning uses neural networks to simulate human like decision making capabilities. Machine learning is the learning process from the dataset that is training the data and testing the data. As machine learning, deep learning and artificial intelligence sowed the seeds for the neuromorphic computing, predecessors of the latter are as follows. Machine learning is a subset of artificial intelligence as it focuses on designing the systems by allowing them to learn and make predictions based on the experience. Machine learning provides computers with the ability to learn without being explicitly programmed.

The prerequisites for the neuromorphic computing are machine learning, artificial intelligence and deep learning. Artificial Intelligence is the capability of a machine to imitate intelligent human behavior. Some of the examples of artificial intelligence are self-driving cars, humanoid and the more. Artificial intelligence is accomplished by studying how human brain thinks and how it works, learn and decide while trying to solve a problem. The outcome rather is an intelligent software and systems. Machine learning is the process that provides the computer with the ability to learn without being overtly programmed. Machine learning is the subset of artificial intelligence. Some of the applications of artificial intelligence are speech recognition, understanding natural language and image recognition.

Deep learning models are capable to focus on the right features by themselves, requiring little guidance from the programmer. The idea behind deep learning is to prepare algorithms that mimic exactly as brain [2]. Neuromorphic technology is generally the hardware that look like the architectures of neuron present in the human brain. This idea was applied to the computer systems using deep learning algorithm. The basic neuromorphic model is Mc-Culloch Pitts models. Inputs such as I1, I2…Im are given as the set of inputs to the neuron and the output y is obtained [3].

$$Sum = \sum_{i=1}^{m} Ii * Wi \qquad (1)$$

$$y = f(Sum) \qquad (2)$$

Trainable analog block is designed from the ideologies of the population coding present in the nervous system, which is tolerable to incompatibility of devices. The advantages of trainable analog block is analog to digital converter and digital to analog converter. The technology used in such trainable analog block is of TSMC 65nm and the supply voltage given is 1.2V. The total power obtained in the trainable analog architecture is 16.56µW [4]. A spiking neural network is a mixture of analog and digital multiprocessor. The system recognized an interface unit that relays information between analog and digital units of the system. The spiking neural systems can be applied to the neuronal sensors. The communication is developed from the input to output with the help of transceivers and the frequency of maximum value is calculated [5]. The complementary metal oxide semiconductor with set of biased currents is consecutively divided using current splitter circuits to obtain the exact results of current at the output end. The technology carried out in the master bias current circuits is of 0.5µm. At each branch of the circuit, the currents are carried onto the input end to the output end. The current mirror is the circuit which helps in the repetition of current [6]. The learning algorithms are to be efficient in terms of energy and the power also plays in the major part of the device architecture.

The cognitive tasks are such tasks which is being in field of science for machine learning resolutions. The power consumption of the brain comes around 10-20W and to perform the cognitive tasks the computers might need large amount of power to perform the better process and to obtain the desired result. The energy efficient devices can be built with the help of silicon chips that resembles the addition of various neurons and cognitive computing technologies.

There are many experiments regarding the neuromorphic computing, where the computation, power, energy, speed and cognitive thinking capability are to be ensured [7]. Deep learning is implemented through neural networks i.e., biological neurons. While deep learning is a subset of machine learning. Deep learning uses neural networks to simulate human like decision making abilities [8]. The learning through artificial means is of a tougher task, such learning algorithms must be well enriched with performance and cost efficient. The Sign based Online Learning Algorithm (SOUL) is a learning algorithm where the neuromorphic architectures comes into role. The Extreme Learning machine (ELM) comes in with the implementation of the sign based learning algorithm which consists of feed forward neurons. There are various other algorithms such as Online Pseudo Inverse Update Method (OPIUM) for better performance based learning algorithms. The SOUL algorithm is a simple learning algorithm, and such algorithm also brings in out the association between the errors occurred the number of nods hidden in the circuit. As the hidden nodes are necessary in terms of machine learning for the device to get learned according to the objects [9]. The trainable analog block uses multiple input single output (MISO) to improve the performance of the neuron design. The output voltage which is derived from TAB framework of MISO system using the input voltage V1 and V2 and their respective trans-conductance gm1 and gm2 is given in the equation.

$$Vout = \frac{gm1 * V1 + gm2 * V2}{gm1 + gm2} \quad (3)$$

The inputs are randomly obtained from the input to the non-linear hidden layers [10]. The memory and sensory locations in the neuromorphic computing are very much essential in the learning process. As memory plays a rapid role in the neuromorphic architectures, power consumption in such memory operations becomes huge. The technology used in such memory of the neuromorphic architectures is of 28nm technology [11]. Analog multiplier circuit is the major block in most of the signal processing applications. A CMOS current mode multiplier without any error is designed by squaring the analog mode circuits. The technology used to build the analog current mode circuits is TSMC 0.18µW. Current mode circuits are such circuits which define the current passing through the entire circuit. The bias current is of 60µA where the input currents are swept from -20 to 20 µA [12]. The main process of the mentioned neuron model is to pass on the current from one neuron to another neuron where the impulses takes place accordingly. The neuronal activities are based on the hidden neuron network [13]. Neuromorphic system encrypts the input stimulus using large number of neurons and decrypts the expected function by combining the activities of the neurons. It is an alternative to the traditional technology and have great future in artificial signal processing. TAB framework is designed using various principles of neuromorphic computing based on computation of various stochastic algorithms. Such TAB frameworks has low power consumption and easily adaptable to changes to learn [14]. The photonic activity of the neuro-transistors will be an advantage in the power consumption. In order to produce photonic neuromorphic chips to perform the neuromorphic computing tasks, the device must be integrated with optical input sources and wave guides to prevent the noise factor [15]. The piecewise linear model is much appropriate for analog current mode devices. The half-center oscillator in neuromorphic computing is implemented to measure the neuronal activities of the brain and the animal activities too. The non-linearity of such piecewise oscillation is of dependent on the equation.

$$f(x) = \max(0, x) \quad (4)$$

The neuromorphic oscillator is to work in order to obtain the controllability of the amplitude and the frequency of the device [16]. The low power consumption and the feedback methods are the features which are necessary in such neuromorphic designs. The current mode circuits which are operational in subthreshold regions implement the log-domain filters. The differential pair integrator is similar to the log domain filters as in such with an advantage of tunable gain, good matching and low power consumption. The technology carried in differential pair integrator circuit is of 0.35 µm. The supply voltages given in such circuits is of 3.3V and 1.2V. The area occupied by the differential pair integrator circuit is of 464.750µm$^2$ [17]. The neuromorphic computing is done with silicon chips as in to have minimum power consumption and better efficiency of the circuit [18].

The basic block diagram for the entire neuromorphic computing algorithm which is discussed in the paper is as follows in Fig.4.

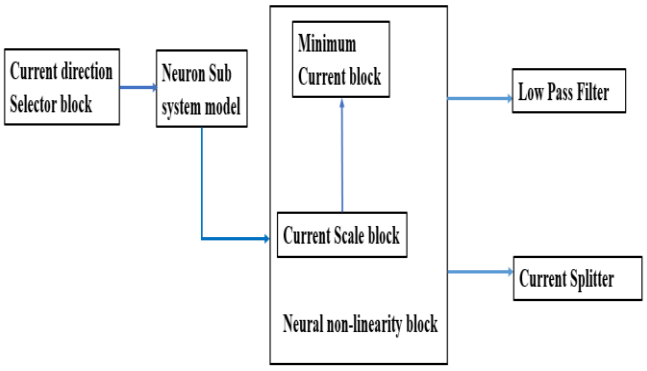


**Fig.4 Flow chart of Neuromorphic Process**

The above block diagram of the neuromorphic architecture consists of different blocks such as current direction selector block, neuron sub system model, minimum current block and current scale block which both comprise of the neuron non-linearity block. These blocks are again connected with the eight weight block current splitter circuit which acts as a building block in the power consumption bound in the circuit.

## IV. WEIGHTED INPUT BLOCK

The primary block is of current direction selector block where every input has one input current and one input voltage which represents the sign and magnitude of the input parameter. In this block, the input current is set in the direction either to source or sink based on the input sign voltage. The mismatches in the device cause the difference in the magnitudes of the input current and output current which might be used in the population coding and ESN as they need random and fixed scaling of inputs.

The schematic of the current direction selector is shown Fig. 5. The current direction selector is a significant block where the input current from one end of the neuron is forwarded to the output neuron structure. The simulation output of the current direction selector is provided in the following Fig.6. From the simulation result, it is evident that there is a transient relationship of the output with respect to the inputs given. The two such inputs given in the current direction selector block are I bias and V-bias sign. The resultant output is shown in the graph.

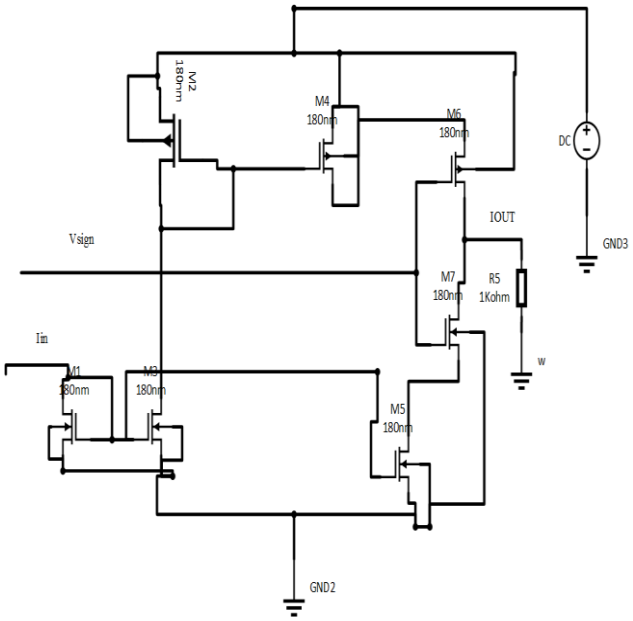


**Fig.5 Schematic of Current Direction Selector**

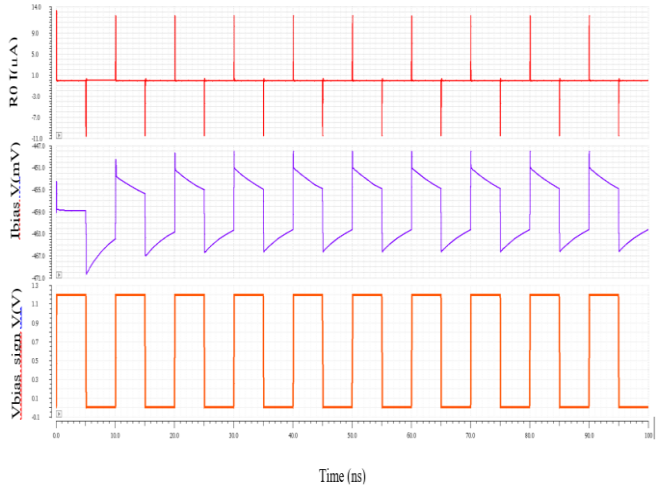


**Fig.6 Simulation of the Current Direction Selector Block**

## V. NEURON NON-LINEARITY BLOCK

### *A. Current Scale Block*

Current scale block is the secondary block which comes after weighted input block in the neuron non-linearity block. The transistors M5 and M6 are used to repeat the input current from the summation block. The two voltages which are present in the current scale block act as the differential voltages. These two voltages are the controlling scaling factor of this block, in which the Vscale1 is a variable voltage for different neuron systems whereas Vscale2 is a fixed voltage value. The schematic of the current scale block is shown in Fig.7. The simulation output of the current scale block is provided in the following Fig.8. The simulation result explains in about the output versus input dc relationship. There is a steep straight line where the voltages are adjusted accordingly and the output is obtained.

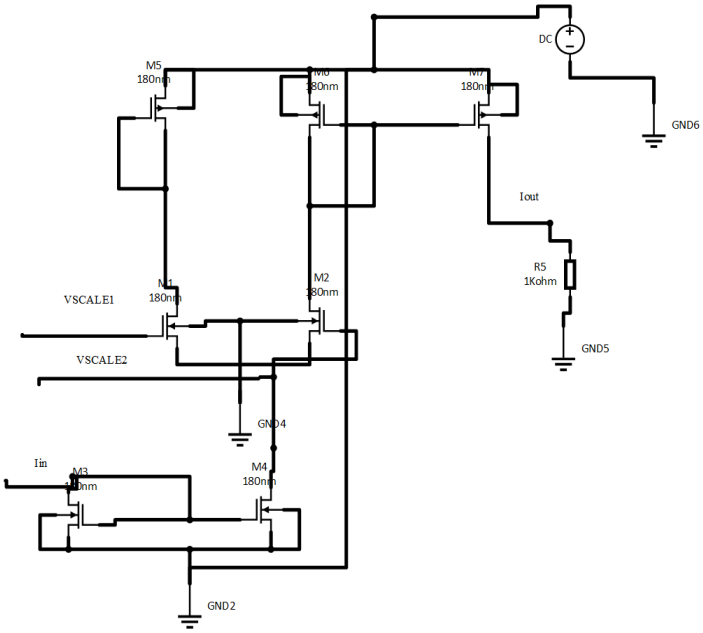


**Fig. 7. Schematic of Current Scale Block**

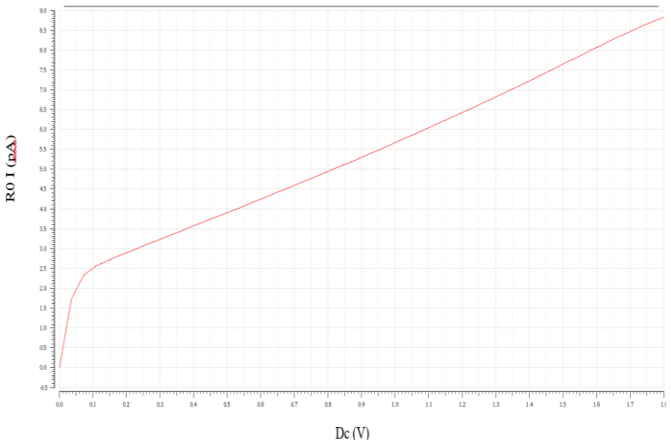


**Fig. 8. Simulation Result of Current Scale Block**

### *B. Minimum Current Block*

Minimum Current block is another block of neuron non-linearity block where the output of the current scale block is connected to the minimum current block produces the output current.

The current obtained in the output of the current scale block is directly proportional to the input current and it varies according to the scale voltage Vscale1. If the current at the input exceeds the threshold current, then the current at the output gets fixed to the threshold current itself. The output current obtained at the minimum current block is resulted as neuron output magnitude. The schematic of the minimum current block is shown in the following Fig.9. The simulation output of the minimum current block is show in the following Fig.10.

The interpretation of the simulation is that there is a transient relationship between the input currents and the obtained output.

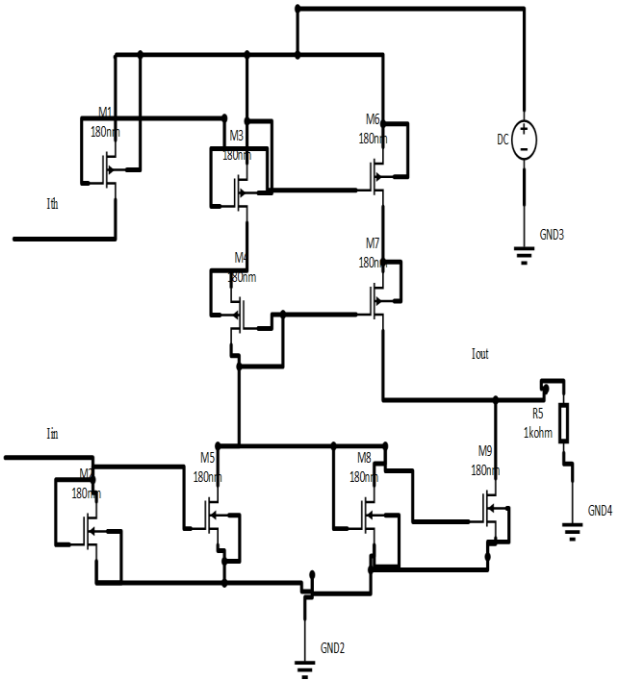


**Fig. 9 Schematic of Minimum Current Block**

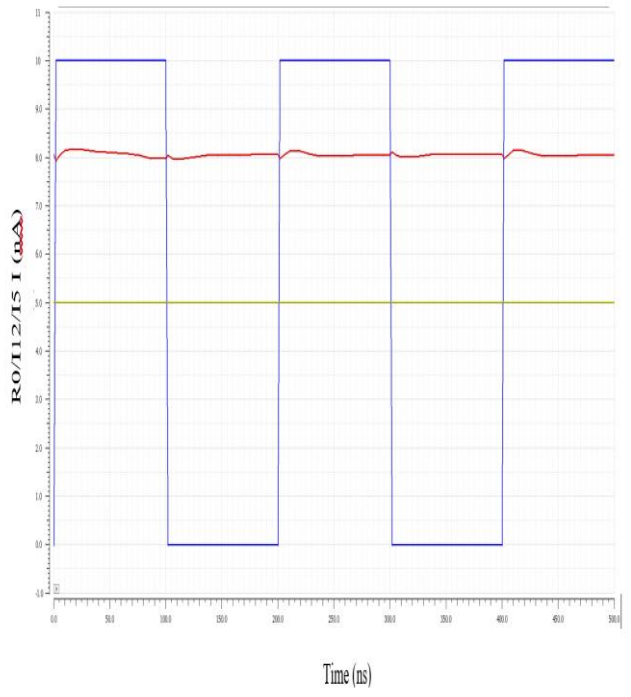


**Fig. 10. Simulation result of Minimum Current Block**

## VI. NEURON BLOCK

The main process of the mentioned neuron model is to pass on the current from one neuron to another neuron where the impulses takes place accordingly. The synapses between the various neurons act based on the passage of currents. The complete circuit along with the current splitter circuit which reduces in the power consumption accordingly so as the energy. Current splitter is made as an eight weight blocks as an experiment to attain the output current with minimum power consumption. The current splitter plays a major role in the neuron system which determines the weight of the device. The final or the complete circuit of the neuron model with weighted input block, neuron non linearity block and the current splitter block is shown in Fig.13.

The simulation results of the neuron block is, where one input current is given as 0A and the other input current is varied from -80nA to 80nA. The table mentioned also indicates the region of operation and the power which is obtained as an end result. The simulation results of the neuron block are shown in Figure 4.4, where one input current is given as 0A and the other input current is varied from -80nA to 80nA. The simulation result interprets that the two input currents are given and the output current is obtained at one end as 340.0 pA i.e., positive current end and at the other end as 2 pA i.e., negative end. At one end of the output current, the yield is 2.125mA due to the absolute difference between the input currents of -80nA and 80nA. At the other end of the output current, the yield is 12.5mA due to the absolute difference between the input currents of -80nA and 80nA. Thus the output current ranges from 2.125mA to 12.5mA due to the input current range of -80nA to 80nA.

$$\frac{Output}{Input}\text{(Ratio)} = \frac{Output\ Current}{Range\ of\ Input\ Current} \quad (5)$$

$$\frac{Output}{Input} = \frac{340pA}{16000} = 2.125\text{mA} \quad (6)$$

$$\frac{Output}{Input}\text{(Ratio)} = \frac{Other\ Output\ Current}{Range\ of\ Input\ Current} \quad (7)$$

$$\frac{Output}{Input}\text{(Ratio)} = \frac{2pA}{160} = 12.5\text{mA} \quad (8)$$

The schematic of the neuron figure is divided in terms of three parts as in to explain it in very precise form. The schematic of the first half of the entire neuron circuit consists of current direction selector block which is shown in Fig.11. The second half of the circuit shows in the combination of current direction selector block and the neuron non-linearity block which is also shown in Fig. 12.

The entire neuron circuit with low pass filter is shown in Fig.13. The simulation of the entire neuron design is shown in Fig.14 and the input versus output current ratio simulation is shown in Fig.15.

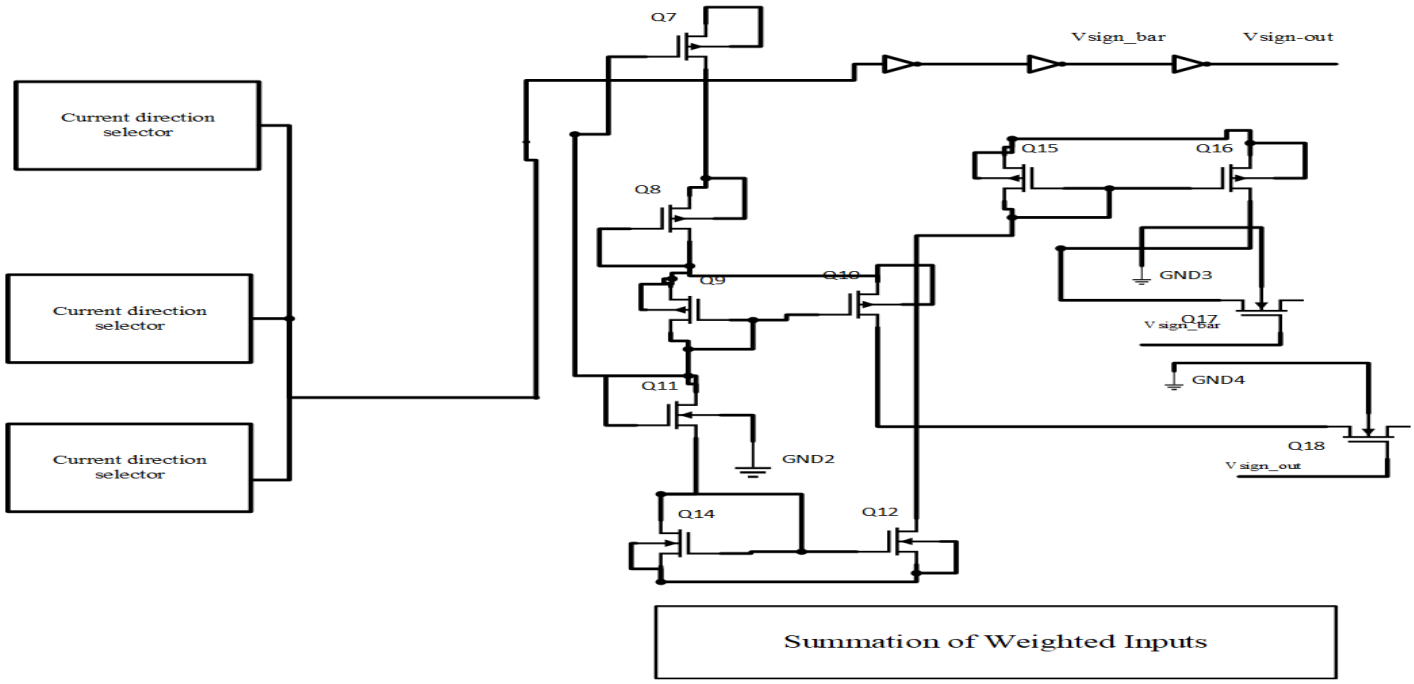


**Fig.11 Schematic of the initial part of the neuron design**

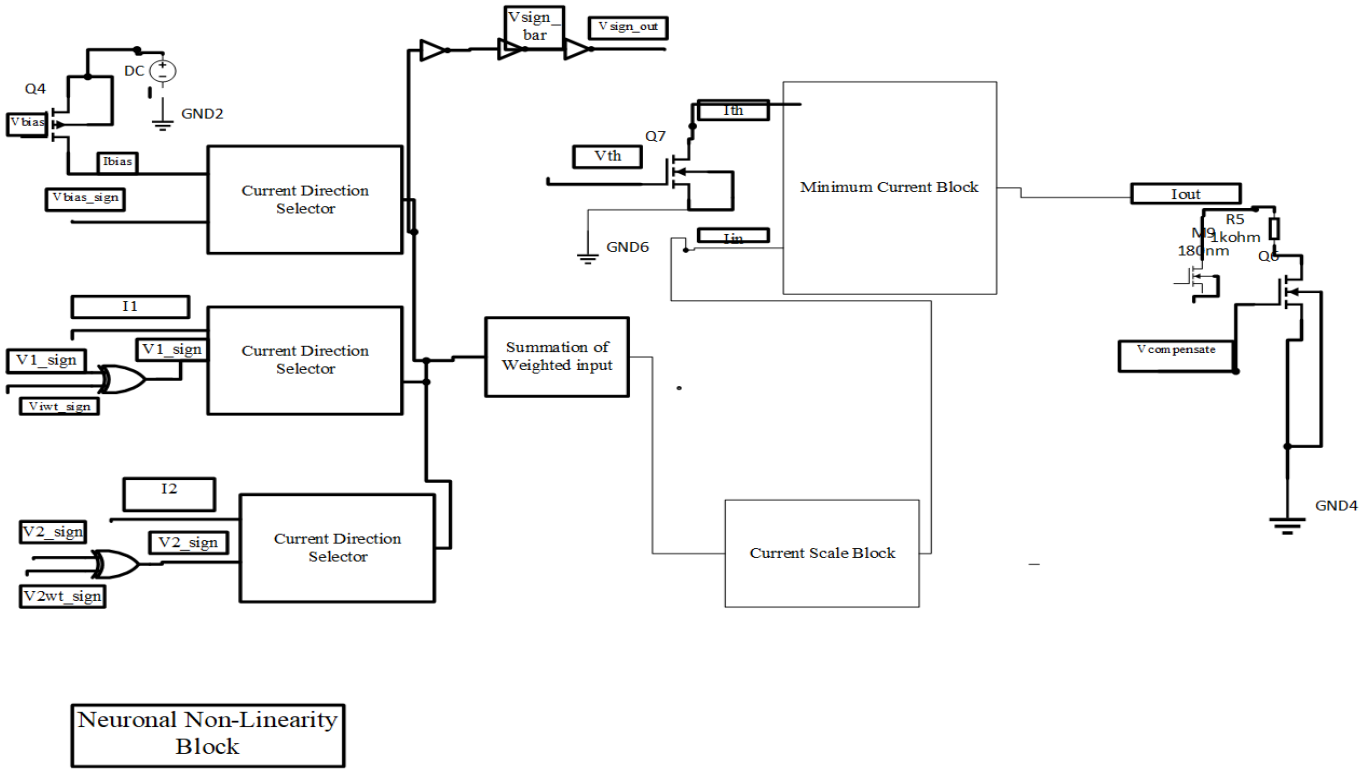


**Fig.12 Schematic of the later part of the**

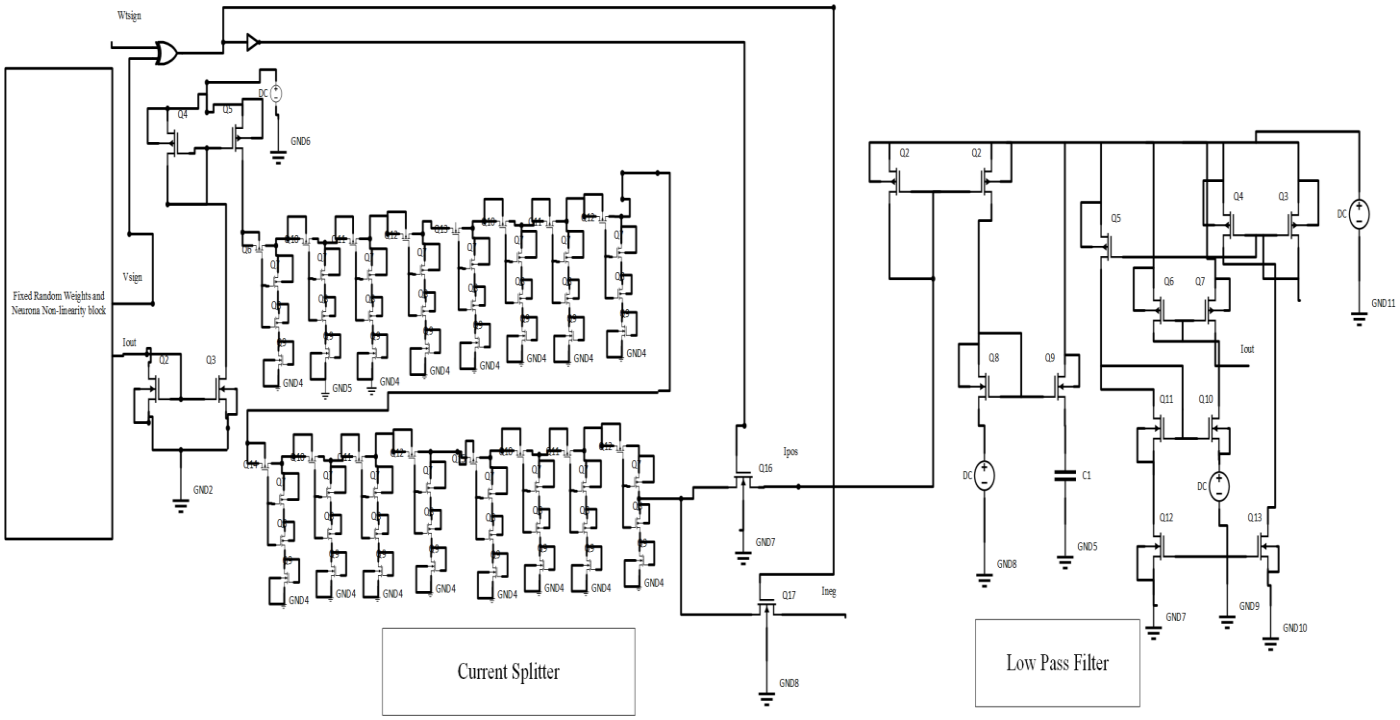


**Fig. 13 Neuron Design**

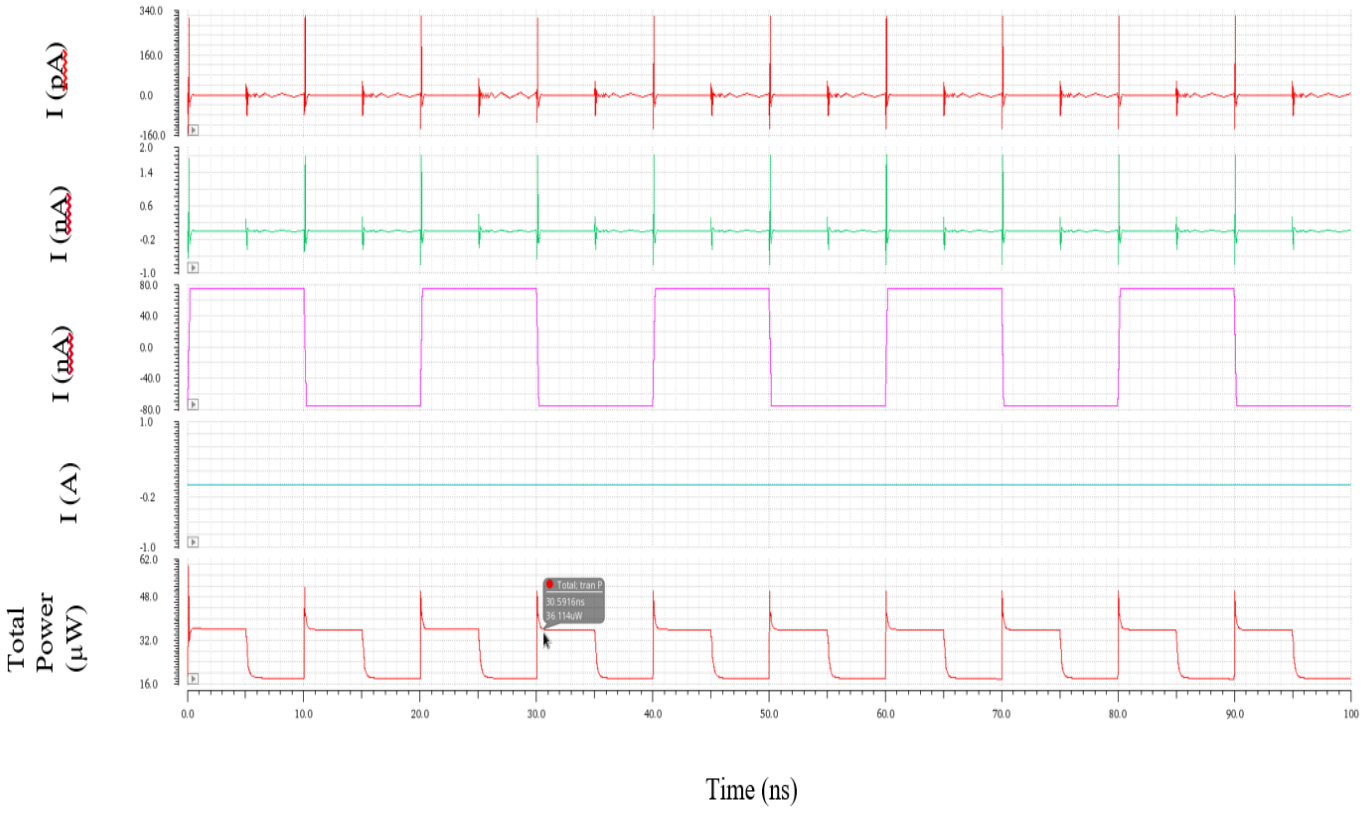


**Fig. 14 Simulation result of Neuron**

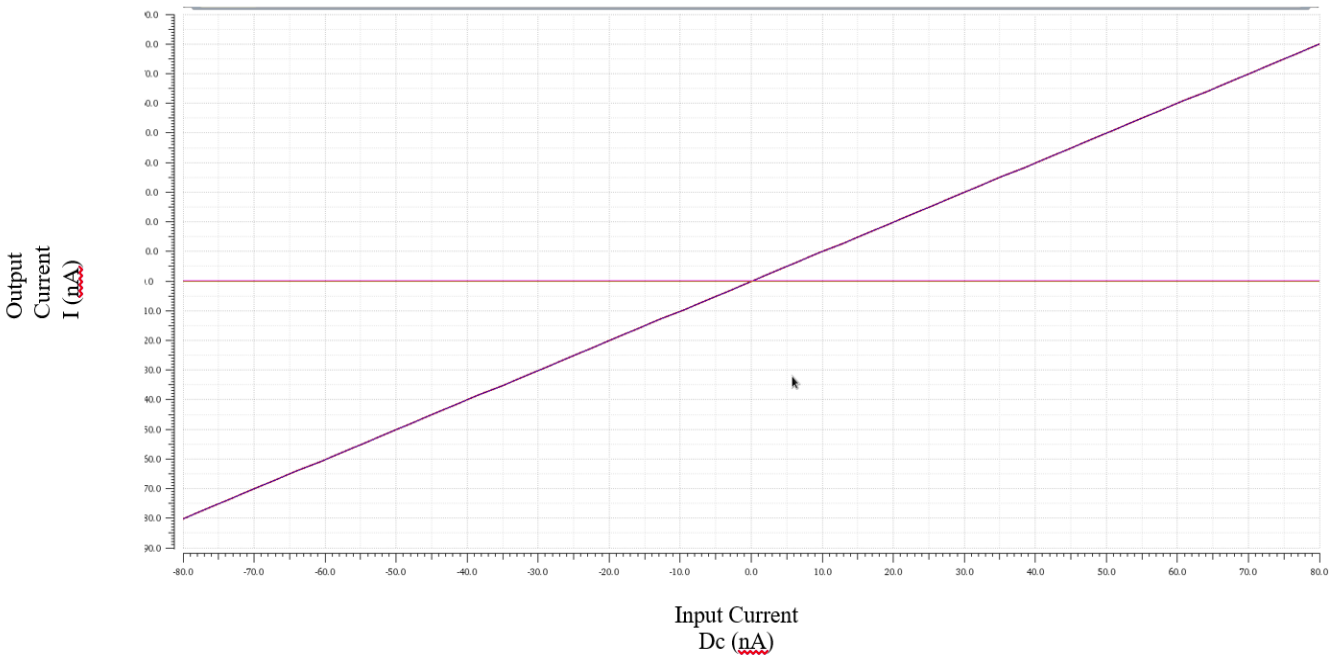


**Fig. 15 Input current vs Output current**

**TABLE I COMPARISONS OF THE PARAMETERS**

| Parameters | Current Paper | Additional contribution | Low Power Neuromorphic Analog System based on Sub-Threshold Current Mode Circuits [13] | Neuromorphic silicon neuron circuits [18] | An Analogue Neuromorphic Co-Processor That Utilizes Device Mismatch for Learning Applications [10] | A Low Power Trainable Neuromorphic Integrated Circuit That Is Tolerant to Device Mismatch [4] | A subthreshold CMOS circuit for a piecewise linear neuromorphic oscillator with current-mode low-pass filters [16] |
|---|---|---|---|---|---|---|---|
| **Technology** | UMC 180nm | GPDK 90nm | 180nm | - | 130nm | TSMC 65nm | 4.5um |
| **Region** | Subthreshold | Subthreshold | Subthreshold | Subthreshold | Weak inversion | - | Subthreshold |
| **Power** | 58.838µW | Average Power=5.4nW | Very low power | 50-1000nW | Very low power in µW | 16.56µW | Very low power in the range of µW |
| **Vth** | 0.5V | 0.5V | - | - | - | 1.2V | - |
| **Vds<=4KT** | -13.96mV<=4KT | -142.5mV<=4KT | - | - | - | - | - |

Table I represents the comparison of the parameters with the current paper of 180nm technology and the additional contribution of 90nm technology and other reference papers accordingly. The papers which is been referred are done with respect to their technological standards and the results obtained also in accordance with the technology.
Table II represents the parameters which are involved in the neuron design. The Table II represents the parameters of the neuron design in terms of the technology and the region of working. The technology used in circuit schematics and simulation are of 180nm. The region used in the circuits are subthreshold region, which is in MOSFET is where the transistor works a bit below threshold voltages The power obtained in the 180nm technology is of 58.838µW. It also gives in the values supporting the subthreshold condition of the neuron circuits.

**TABLE. II PARAMETERS IN THIS NEURON DESIGN**

| Parameters | Readings |
|---|---|
| Technology | UMC180nm |
| Region | Subthreshold |
| Power | 58.838uW |
| PMOS: Vth | -515.5mV |
| Vgs | -13.96mV |
| Vds | -13.96mV |
| Vds<=4kT | -13.96m<=0.104 |
| NMOS: Vth | 439.4mV |
| Vgs | -462.mV |
| Vds | 1.186m |
| Vds>=4kT | 1.186>=0.104 |
| Energy | 1.726pJ |

The energy which is obtained from the power output is as follows.

$$\text{Energy} = \text{Power} * \text{Time} \quad (9)$$

$$\text{Energy} = 58.838\mu W * 30.0ns = 1.76pJ \quad (10)$$

The neuron figure represents the 90nm technology which is been additionally added with the low pass filter as in to reduce the power consumption. The average power in 90nm technology is of 5.41nW, whereas the power in 180nm technology it is of 58.838µW. The simulation output of the entire neuron design with the power output is shown in Fig.14.

The simulation which is shown in Fig.15 is that of input current versus output current. The neuron circuit is maintained in subthreshold region which is where the transistor works a bit below the threshold voltage [19]. The main advantage of working at this region is that the output current is associated exponentially with the input voltage rather than quadratic relationship to the input voltage in saturation region. It rises the trans-conductance of the MOSFET and so getting higher gain.

$$Vgs \leq Vth \quad (11)$$

The above equation represents the subthreshold region which is maintained in the circuit. The main benefits of the working at this region is that the output current is related exponentially with the input voltage rather than quadratic relationship to the input voltage in saturation region [20]. It increases the trans-conductance of the MOSFET and so getting higher gain.

## VII. RESULTS

The proposed techniques have very high power consumption or the area of the design. The techniques which are used have different technologies. The result obtained in this paper is of with respect to 180nm technology i.e., power is of 58.838µW and the corresponding energy is of 1.762pJ. The output current ratio which is obtained as an end result is of 2.125mA to 12.5mA. The average power which is obtained in 90nm technology is of 5.4nW. The circuits in the neuron design are maintained in the subthreshold region. The neuron circuit which is designed in this paper consists of 10 hidden neurons. The designs are maintained as analog circuits and such circuits are of current mode circuits. The current splitter circuit which is used is of 8-input circuit.

## VIII. FUTURE WORK

The same design is carried in various other lower technology so as that the output which has been obtained in relation with power consumption will be reduced further and can be improved. Additional circuits can be for the feasible of the current from the input end to the output end.

## IX. CONCLUSION

Neuromorphic architecture is that the current impulses is passed onto to the neurons in different neuron systems. The power is stated can be improved if the low power filter technique is used in the later improvements. The area can also be reduced if the number of transistors are minimized in the later improvements. Neuromorphic design is mentioned in this paper is in accordance with the analog domain and the circuits are operated in current mode. The circuit is maintained in subthreshold condition. The prime objective is to lower the power consumption. The circuit is designed in both 180nm technology and 90nm technology as a comparison to ensure better output and low power output. Current splitter circuit is used as an eight weight blocks to minimize the total energy. The neuron model is strong in nature in both the cases of population coding architecture and echo state networks.

VLSI industry concerns with the better power consumption chips as well as more efficient circuits. The drawbacks such as lots of power consumption, huge area and improper scaling effects bring in the inefficiency of the devices. To avoid such inefficiency, scaling and better circuits are to be constructed. Neuromorphic computing is an area where the machines are to be more precise and more accurate, for accurate results better circuits are to be chipped in and the power consumption should be considerable. This paper speaks about the low power consumption and energy efficient neuron design. The neuromorphic design is such that the parameters shall adhere to their design specifications and methods.

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