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Design and Implementation of VGA, Mixer and Phase Locked Loop

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Abstract*: In this paper we discussed about different types of techniques used to design mixer, VGA and PLL circuits for Software Defined Radio (SDR). Software Defined Radio is a type of radio wherein some of the conventional hardware component is replace by a software component making it more versatile. Here we are concentrating on the hardware component of SDR. Various techniques in CMOS technology is reviewed here for example two stage amplifier, cascading of VGA blocks, PLL as a clock generator and conventional fine loop are discussed. By using CMOS technology, the IC chips can be developed within a small area and also power optimization can also be done.

***Keywords : VGA, Mixer, Phase Locked Loop*.**

I. INTRODUCTION

a) **Mixer:** Mixer is an electronic device that is used to convert from higher frequency signal to lower frequency signal. Mixer can be designed in both active as well as passive device. It has mainly consisted of three ports, were two are input ports and one is output port. The inputs are from one is Radio Frequency (RF) signal and other is Local Oscillator (LO) signal. The output is known as Intermediate Frequency (IF) which is of lower frequency signal. Fig.1. shows that schematic of Mixer.

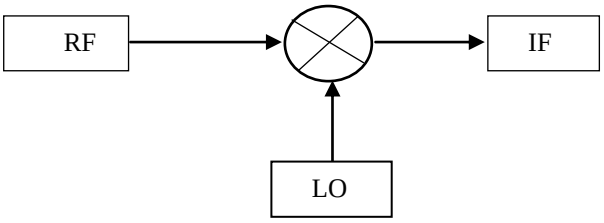

Fig. 1.Schematic of Mixer.

b) **Phase locked loop (PLL):** PLL is one of the feedback circuit which mainly consists of Phase Detector, Low Pass Filter (LPF) and Voltage Controlled Oscillator (VCO) this arrangement shows in Fig.2.

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c) The PLL mainly helps in maintaining constant phase difference at the output by continuously comparing with the reference signal. The PLL can be used in several forms but in this work, we use PLL as a clock generator.

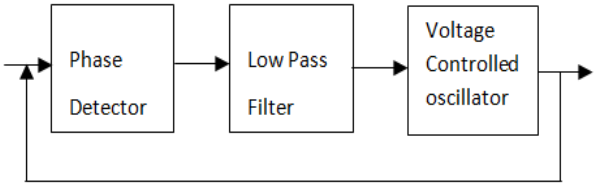

Fig. 2.Block Diagram of PLL.

d) **Variable Gain Amplifier (VGA):** The VGA is used to provide stable gain at the output signal for different input signal. VGA can be analyzed by using various parameter like bandwidth, noise, linearity and power consumption. VGA can be of two types one is Analog VGA and other is Digital VGA. Here we mainly concentrate on Analog VGA. VGA can be implemented using CMOS technology for which reduces the integration cost. Fig.3 shows that block diagram of VGA.

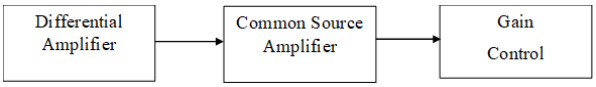

Fig. 3.Block Diagram of VGA.

II. LITERATURE SURVEY

The proposed paper [1] mainly consists of design of two stage as well as three stage amplifiers along with the small gain stages. Here designed amplifier has been compared with all the designed amplifiers along with their gain stages using their performance parameter. The amplifiers have been designed using standard 130nm CMOS technology where the DC voltage is about 0.7V and its current usage is about 20uA and its slew rate is about 0.367V/us. From this paper we have taken the circuit diagram of two stage amplifier since the amplifier used in SDR application is similar to the designed amplifier.This paper [2] mainly deals with the design of VGA for SDR using 130nm CMOS technology. VGA is used in order to provide constant gain at the output. In this CMOS process the input DC supply voltage used is +1.2V with the maximum gain of 38dB. The designing of VGA mainly depends on two factors that is linear variation with control voltage and the gain must be constant over entire frequency range. We have read this paper in order to compare the existing technology with our work.
This paper [3] deals with design of VGA for wireless communication technology. The VGA is used to increase the signal strength to provide the constant gain at the receiver.

The CMOS technology used to design VGA is 130nm.
This paper gives information about cascading of VGA block to minimize the gain error and to optimize the linear gain range. The cascading circuit requires few milli-amperes of current and voltage supply is about 1.2V.
The paper [4] gives information about comparison between phase variation and gain control range in VGA. This technology uses 28nm CMOS technology. Here, multiple input multiple output (MIMO) system is employed in order to provide large coverage range along with the high reliability. One of the disadvantages of this work is, it consumes large current of 4.2mA and voltage is about 1.8V.
The proposed paper [5] choose either Analog or Digital for design of PLL in CMOS technology and both designs are used in communication purpose and some case used to control the Servo Motor. In this paper studied the all common techniques to build a PLL for advanced communication by using CMOS technology and to achieve high accuracy and reliability at the output of PLL. Every block of PLL should be maintain linearity for achieving response of the system.
The paper [6] is used to know the design of PLL as a Clock Generator. The technology used here is 350nm using CMOS process. Since it is designed using 350nm we can optimize our work in area specification. This paper mainly concentrates on reducing and lower the jitter at the output of PLL. Phase and Frequency detection technique is also used for the technique in order to synchronize the time. The supply of voltage is about 1.3V to 3.3V. Hence, we refer this paper to known the design of PLL as Clock Generator.
The main objective of this paper [7] is to design of PLL which is used to reduce the power and glitches at the output node. This design use charge pump circuit to reduce the current glitches at the output of PLL and use the method of voltage doubler circuit to increase the voltage range and all these concepts are increase the voltage range. These new approaches of PLL design overcome the problem of glitches and achieve low power, reduce noise and increase the synthesizer bit rate using CMOS 0.12um technology.
This paper [8] mainly deals with design of novel PLL. The design of PLL involves two topologies, one among them is conventional fine loop and the other is new coarse loop. The conventional fine loop involves phase frequency detector and feedback circuit of PLL. The feedback loop circuit mainly used here is Differential Voltage Controlled Oscillator. The new coarse loop is very much faster. The entire technique used in this work ensures higher stability, lower jitter and it also ensures power stability. This paper [9] mainly concentrates on wideband mixer and VGA. For our use, mixer part is taken into consideration. This paper deals with the design of wideband mixer. Mixer is a circuit that converts RF signal into an IF signal. Here active mixer topology is chosen for long distance communication. Gilbert cell mixer is the mixer topology used in this paper. Advantage of using this topology is high conversion gain, high even order linearity and port to port isolation. There are disadvantages of using this topology as well some of these disadvantages are difficulty in optimizing conversion gain linearity and noise. But the paper provides the solution to the above disadvantages. The issues can be overcome by increasing DC current of the RF input stage. The paper [10] deals with design of N-phase passive mixer. The passive mixer performs the same basic frequency translation function as an active mixer. There are additional features such as bidirectional impedance transparency i.e. simultaneously up converts the signal on its base band port and down convert those on the RF port. Advantage of using passive mixer is bidirectional signal translation. There are some disadvantages as well such as a resistive behavior, lack of power gain, attention of signal there translate, degrade the noise and gain of the system.
The paper [2] presents a low voltage, low power, high linearity quadrature mixer for SDR application in a 90nm CMOS technology. The mixer consumes a DC power of only3.8mW under 1V supply. For energy-efficiency software radio the most practical solution is reconfigurable RF front-ends can be widely programmed to operate with all present & future standards. The proposed mixer has excellent performance in comparison with other CMOS mixers.
In the paper [11] a low power, high linearity wideband passive mixer for SDR is presented. It employs the improved current reuse Gm stage, combines source degeneration with MGTR to extend the linearity region while enhancing the power performance. Measured results show that power is improved about 5dBm, this passive mixer achieves 13.7dB NF under 13dB conversion gain at 900MHz.

III. DISCUSSION

From all the above papers, CMOS technology plays a very important role for designing of VGA, Mixer and PLL. The VGA can be designed using two stage and three stage amplifiers along with gain stages [1]. The PLL can be designed with the help of two topologies, conventional fine loop and new course loop [8]. The design of N passive mixer is discussed under the paper [10]. The paper [2] deals with design of both mixer as well as variable gain amplifier.

Advantages:

1. Area optimization
2. Power optimization
3. Reduced fabrication cost

IV. DRAWBACKS OF PREVIOUS METHODOLOGY

Use of LC tanks in the design of VCO (Voltage Controlled Oscillator) acquires large chip area and has low Q factor. Oscillators based on LC tanks have low frequency tuning range and the required frequency of operation is may not reside the limited tuning range as the temperature varies. Therefore, inductor less oscillators are under tremendous research. One of major difficulties associated with PLL based technique is that a PLL with wide frequency range cannot be achieved easily. Also, fast switching is difficult to achieve.

V. PURPOSED METHOLOGY

The proposed methodology for designing of PLL, Amplifier and Mixer uses 45nm technology. The device tool used to design these analog circuits is Cadence Virtuoso. To optimize the power and area we use Gilbert and Current Starved circuits.

An RF mixer is an active or passive device that converts a signal from one frequency to another. It has three ports RF input, local oscillator input, and the intermediate output.
A Phase Locked Loop (PLL) is a system that locks the phase or frequency to an input reference signal. PLLs are widely used in computer, radio, and telecommunications systems where it is necessary to stabilize a generated signal or to detect signals. PLL is closed loop frequency system that can be used as a frequency synthesizer and for synchronizing purpose. When it used as a frequency synthesizer then one more block is required which is called divider circuit (Fig. 4). PLL based frequency synthesizer has five main building blocks:

1. Phase Frequency Detector (PFD)

2. Charge Pump (CP)

3. Loop Filter (LPF)

4. Voltage Controlled Oscillator (VCO)

5. Divider

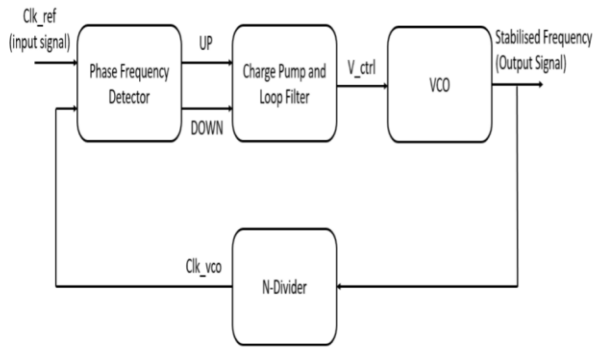

Fig. 4. Basic block daigram of PLL

VI. RESULT

A. Phase Frequency Detector:

The voltage-based phase frequency detector is a combination of two D latch with the combination of an AND gate in a way that the output of the two latch are connected to the input of the AND gate and the two data input are connected to the supply voltage or biasing voltage of the circuit.

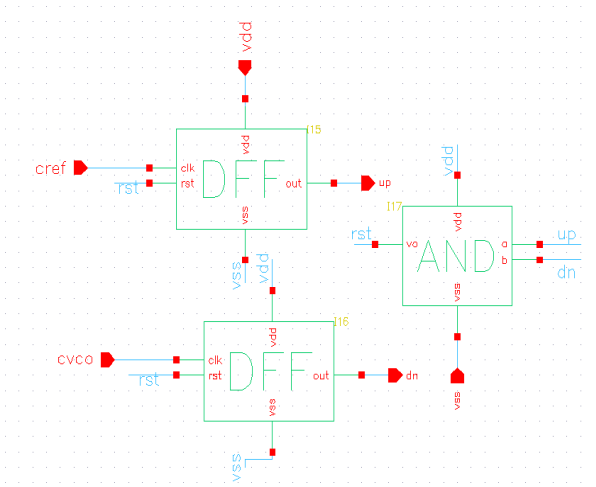

Fig. 5.Schematic of Phase Frequency Detector

1) D flip-flop:

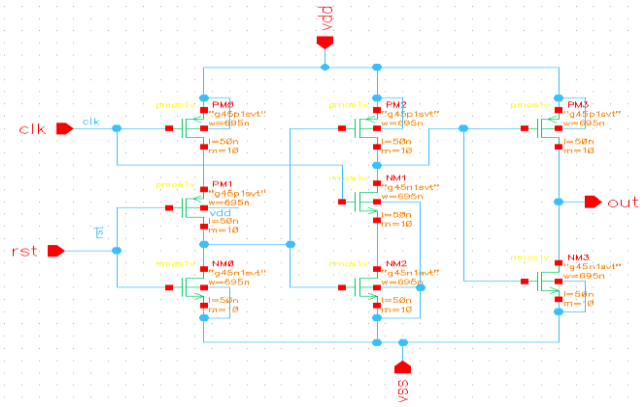

Fig. 6.D flip-flop

The flip flop is a basic building block of sequential logic circuits. It is a circuit that has two stable states and can store one bit of state information. The output changes state by signals applied to one or more control inputs.
The basic D Flip Flop has a D (data) input and a clock input and outputs Q and Q (the inverse of Q).

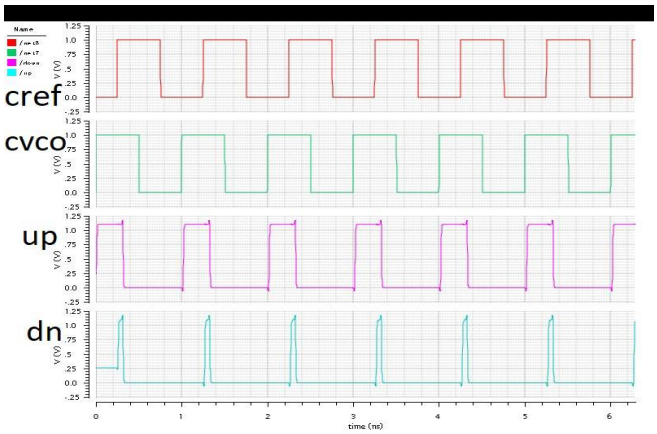

Fig. 7. Simulated output of Phase Frequency Detector when cvco>cref

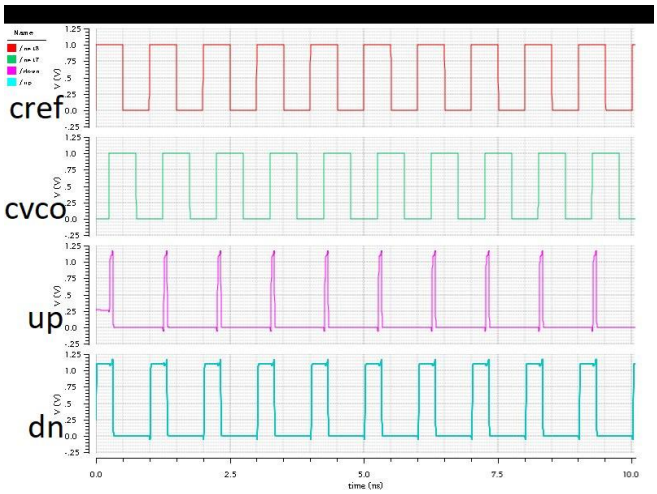

Fig. 8. Simulated output of Phase Frequency Detector when cvco<cref

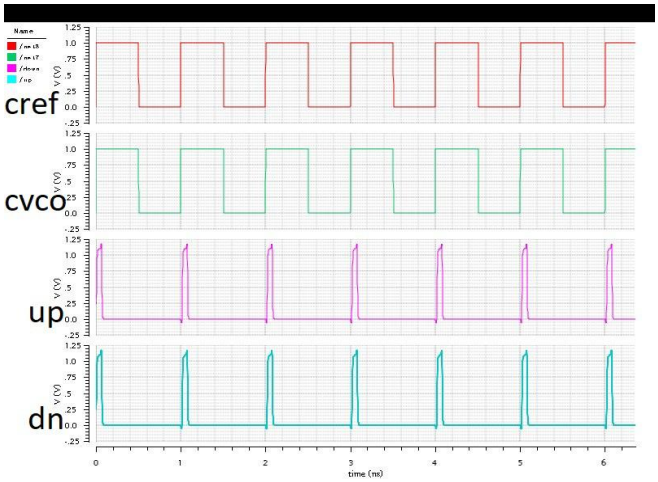

Fig. 9. Simulated output of Phase Frequency Detector when cvco==cref

B. Charge Pump and Loop Filter

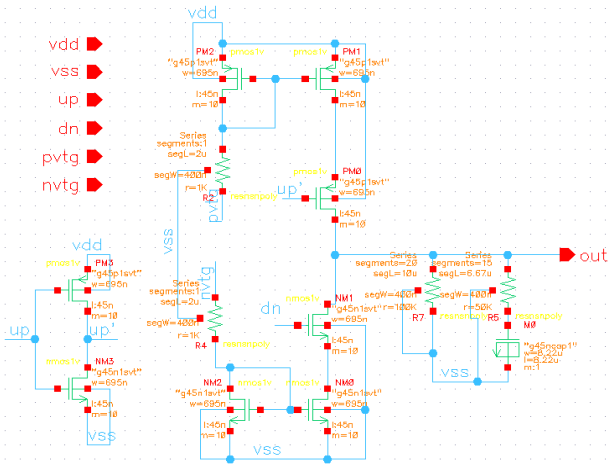

Fig. 10. Schematic of Charge Pump and Loop Filter

The function of a charge pump and loop filter is to take the digital UP and DOWN pulses from the PFD and convert them into an analog control voltage, V_{cntrl}. The design of the PLL, loop filter is crucial to the operation of the whole phase locked loop.

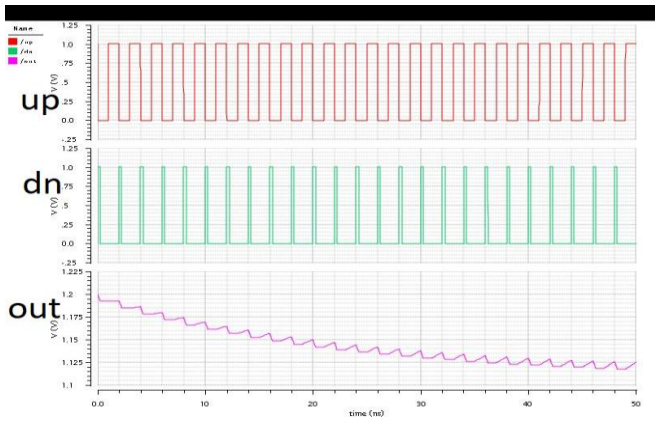

Fig. 11. Simulated output of Charge Pump and Loop Filter

C. Voltage Controlled Oscillator

A voltage-controlled oscillator (VCO) is an electronic oscillator whose oscillation frequency is controlled by a voltage input. The applied input voltage determines the instantaneous oscillation frequency.

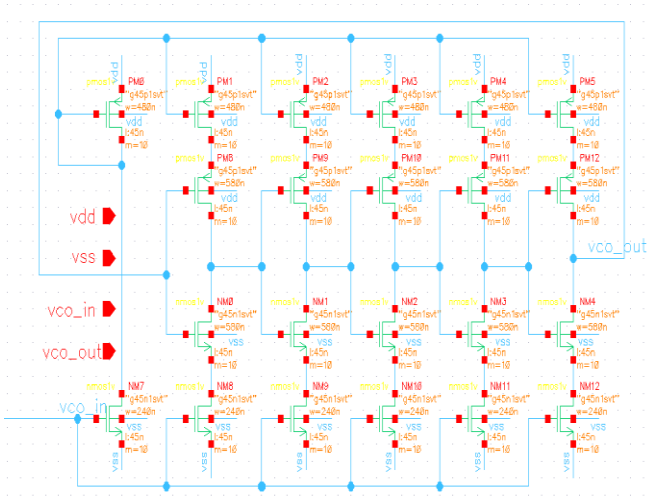

Fig. 12. Schematic of Voltage Controlled Oscillator

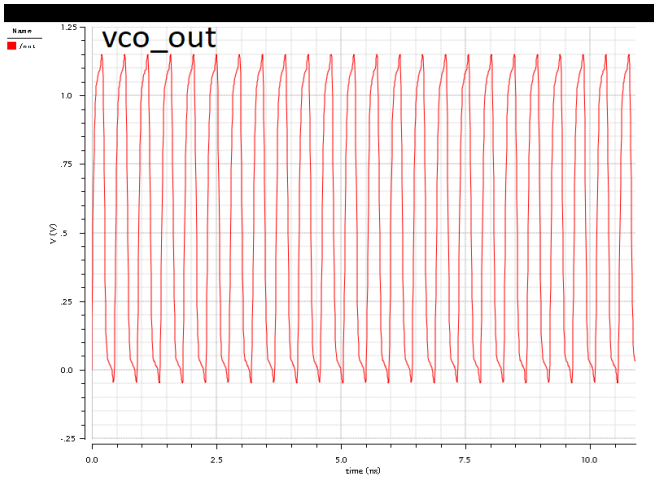

Fig. 13. Simulated output of Voltage Controlled Oscillator

VII. CONCLUSION

From all the above papers surveyed we can conclude that VGA, Mixer and PLL circuits can be developed by using various technologies. The technology or method which is discussed above has both advantages and disadvantages. Here, the main objective is to know the method and CMOS technology used. The existing CMOS technology is 100nm technology. In future scenario the 45nm can also be included for future enhancement of this field.

1. The given frequency synthesizer is giving a lock in time is 3.2ns at 2.3GHz which is a good performance
2. The power consumption of the frequency synthesizer is 1.7609 m watt at 1.1 V power supply voltage.
3. The CSVCO frequency depends upon the current through the inverter and it is finally depending upon the size of transistor so proper value of transistor size will control the center frequency of CSVCO.
4. The loop filter is very important for dynamic behavior of the frequency synthesizer therefore the selection of proper value of resistor and capacitor will decide the speed and behavior of the frequency synthesizer circuit.

5. The phase frequency detector will decide the linearity and the pull-in range of the frequency synthesizer therefore the selection of PFD is very important in the design.

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