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A Novel Three phase Three Wire UPQC (Unified Power Quality Conditioner) Configuration using Ten Switch Topology for linear RL loads

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Abstract*: *This paper presents a novel configuration scheme for UPQC using ten switch topology. Generally, two six-switch inverters connected back to back will form the basic power structure of three wire three phase UPQC. But there are some switches which are less utilized all the time. In order to improve the efficiency of the system, or to improve the effective utilization of the IGBTs there is a need to reduce the switch count in the system. The proposed topology uses only ten switches and gives all the results pertaining to twelve switch toplogy. The Simulation results of proposed UPQC Topology are validated through MATLAB/Simulink environment.

Keywords: Power Quality, UPQC, Inverters, Ten Switch Converter Topology.

I. INTRODUCTION

In Modern Power Electronics Technology, the extensive use of Semiconductors in applications of domestic side and commercial side is increasing the harmonics in current waveform in the transmission as well as distribution sector.[1],[2],[5] Further, it will cause the over-heating of the motor loads, transmission cables which results in poor power quality. To reduce these type of heating losses and to improve the quality of the power flow through distribution lines a unique power device is needed. This can be achieved by a device such as UPQC(Unified Power Quality Conditioner). [4],[8] It is a flexible device which uses modern power electronic semiconductor technology and gives very attractive solution for power quality problems. Any converter/inverter is not connected to the power grid directly instead there is a separate mechanism called Point of Coupling (PCC)[7]. A UPQC is basically a series and shunt combination of two VSI (Voltage Source) inverters connected to grid to improve the quality of the power. The series connected VSI protects the grid from voltage sag/swell and shunt connected VSI compensates harmonic distortion. [10]

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When this type of configuration is used as a twelve switch topology, the switches in series connected VSI operate with less M_a (Modulation Index). This effect of less utilizing the switched is termed as under-utilization which results in huge computational problems.[11][12] This paper presents an entirely new ten switch topology where the main objective is to reduce the switch count. Simulation results are described and explained clearly. The circuit diagram of twelve switch topology is shown in fig.1. The switches in series connected VSI are very less utilized as per the circuit operation.

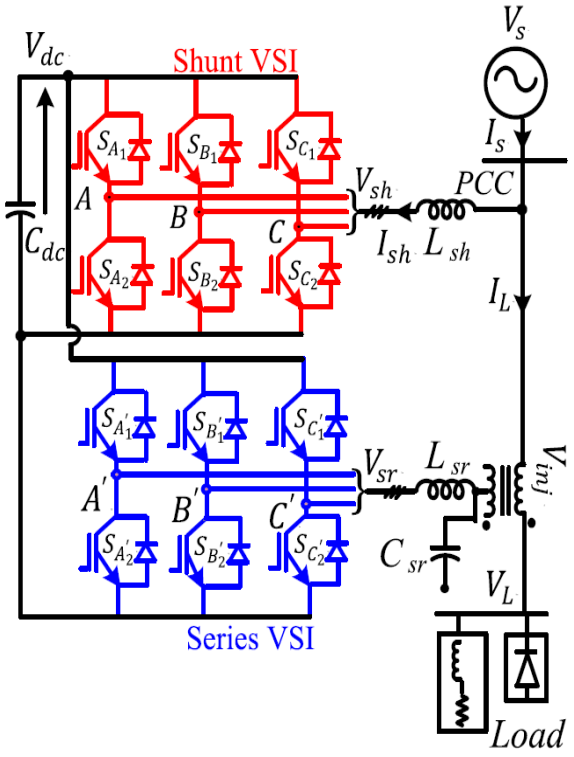

Fig1. Twelve Switch Topology

The shunt connected VSI has the switches namely S_{A1}, S_{A2}, S_{B1}, S_{B2}, S_{C1}, S_{C2} and series connected VSI has switches namely S_{A1}^1, S_{A2}^1, S_{B1}^1, S_{B2}^1, S_{C1}^1, S_{C2}^1 out of which, the switches S_{A1}^1, S_{A2}^1, S_{B1}^1, S_{B2}^1, S_{C1}^1, S_{C2}^1 are very less utilized.[9] The output current of the series connected VSI is through L_{sr} and introduced directly into the grid through a transformer which will reduce the effects of voltage sag/swell. The output current of the shunt connected VSI is through L_{sh} and introduced to the grid in parallel manner which reduces the effects of harmonic currents. [3],[6]

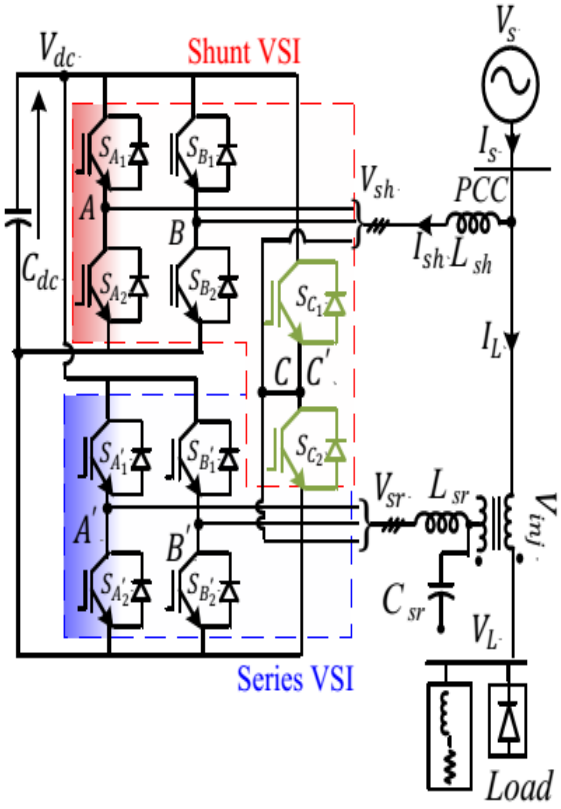

Fig.2 Proposed Ten switch topology

Circuit Description:

The novel ten switch proposed topology is shown in Fig.2 which consists of four switches for shunt connected VSI and four switches for series connected VSI. The two four switch inverters are connected between point of common coupling (PCC) and load.

The general switching configuration for phase C as represented in circuit diagram is given in table 1.

Table: 1 Switching configuration

Voltage	Switching configuration	
	S_{C1}	SC_2
$V_{sh} = V_{sr} = V_{dc}$	ON	OFF
$V_{sh} = V_{sr} = 0$	OFF	ON
$V_{sh} = V_{dc}$, $V_{sr} = 0$	Cannot Realize	
$V_{sr} = V_{dc}$, $V_{sh} = 0$	Cannot Realize	

The switches S_{C1} and S_{C2} are called as shared set of switches which are replaced by combination of S_{C1}, S_{C2} , $S_{C1}{}^{1}$ and $S_{C2}{}^{1}$.

II. CONTROL SCHEME

The control scheme used for this operation is presented in fig.3 To design a ten switch modulator, the voltage signals from the series connected VSI and shunt connected VSI are taken and compared with the carrier signals. The designed ten switch modulator is used in the control scheme for providing the gating signals for all the ten switches.

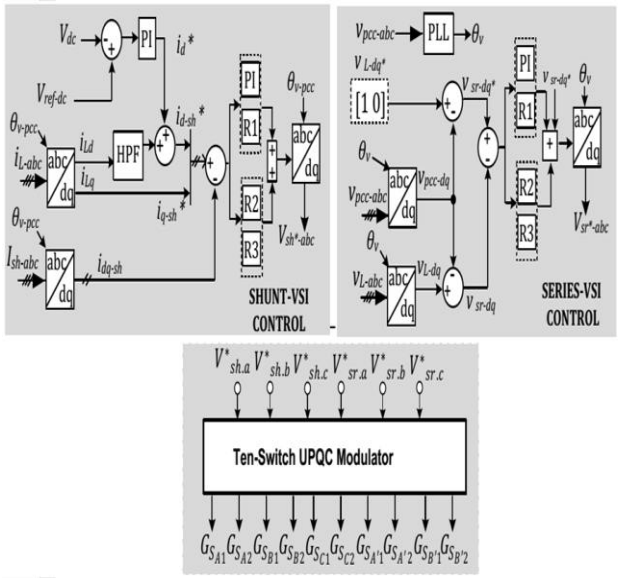

Fig.3 Control Scheme used to produce gating signals

III. SIMULATION RESULTS

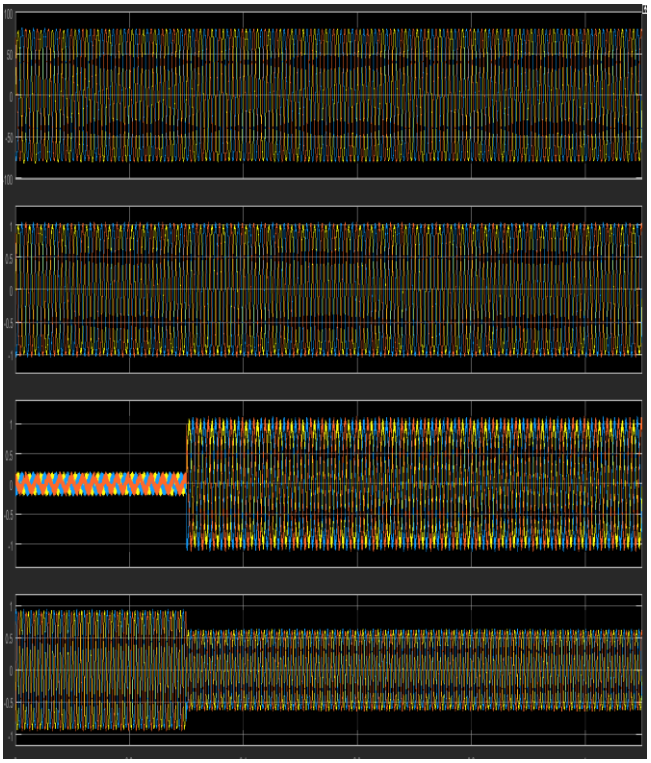

Fig.4 Power factor Correction during steady state condition. (a) Grid Voltage (b) Load Current (c) Current through shunt VSI (d) Current through grid

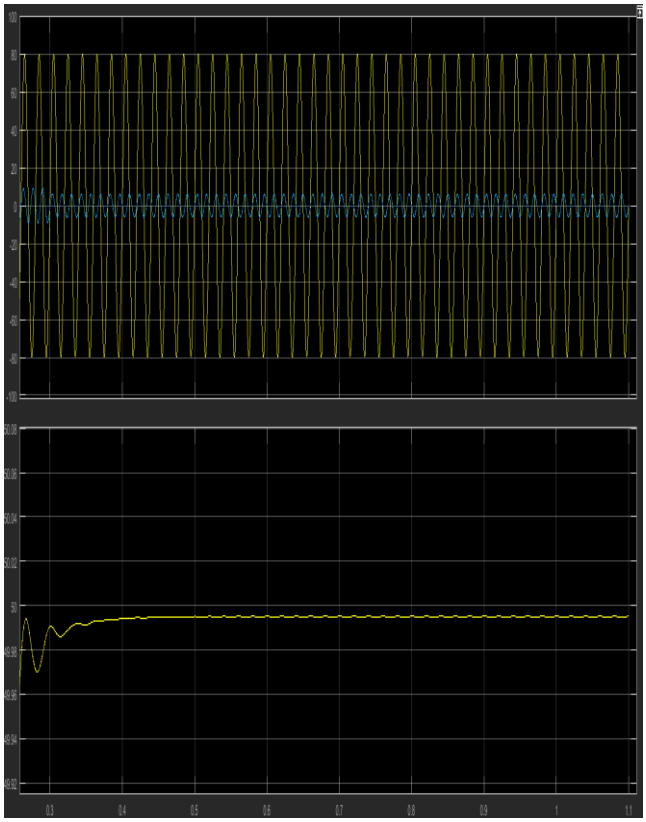

Fig.5 Power factor Correction during steady state condition. (a) V_{grid}, I_{grid} (b) Frequency

The Voltage, current & frequency variations are shown in fig.4 and fig.5

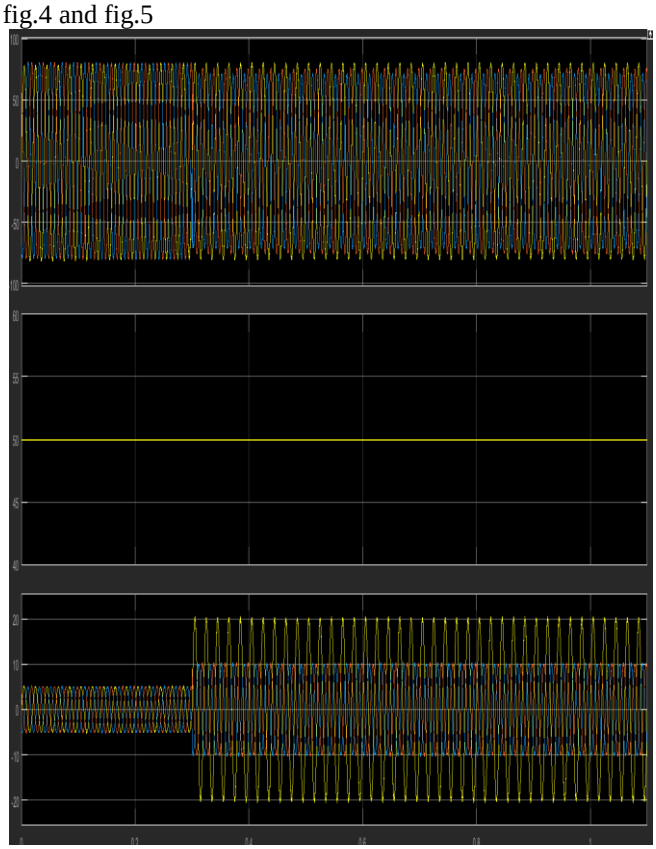

Fig.6 Change from steady state to unbalanced voltage condition (voltage sag) for linear RL load.(a) V_{grid} (b) V_{dc} (c) V_{load}

Table II: Simulation Parameters

S.No	Parameter	Value
1	Supply Voltage	175 V(L-L)
2	R_g	0.047 ohms
3	L_g	160 micro henry
4	C_{dc}	110 micro farads
5	L_{sr}= 2.5Mh C_{sr} = 15 micro farads L_{sh} = 5Mh, R=27 ohms L= 50 H	

IV. CONCLUSION

The proposed ten switch UPQC topology overcomes the disadvantage of under utilization of switches in twelve switch topology which causes huge computational problems. The power factor correction and voltage sag elimination using ten switch UPQC topology is presented in this paper with MATLAB simulation results.

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