Design a Low Power and High Speed Parity Checker using Exclusive–or Gates

Brahmaiah Battula, Valeti SaiLakshmi, S. Durga Sri Sravya, Putta Vijaya Lakshmi, Sunanda Karpurapu, S. Lakshmi Navya Sri

Abstract: In the presented paper we designed the parity checker by using EX-OR modules. The two EX-OR modules are presented to design the parity checker and correlated their outcomes based on the constraints like power, area, delay and power delay product (PDP). The previous design is with eight transistors EX-OR, but in the present six transistors EX-OR is used to design the parity checker. While correlating the parity checker design with 8T EX-OR and 6T EX-OR, the 6T EX-OR parity checker design gives optimized power, delay, area and PDP over the 8T EX-OR parity checker design. Simulations are done by using the 130nm mentor graphics tool. Finally the constraints like power, area, delay and PDP gets optimized successfully with the presented technology. Also, alternatively we can replace EX-OR modules with NAND modules to design parity checker.

Key terms: Power Delay Product (PDP), Parity Checker, EX-OR modules, Mentor Graphics tool.

I. INTRODUCTION

In this the parity codes are explained with different A parity-bit-signature especially apt for exhaustive methods are proposed and results shown that it is agreeable to valuable error coverage computations. And A PC relations based on consolidated generators has been studied and also gave easy formulas for cryptography, finally resulted with successful outcomes. Also A comparison among the parity-relations and its parameters are exhibited and found that they can be used to find the degree-of-freedom to analyze parity generators, to observe the durability. A technology to build codes using certain rate for the given number is presented, represented as repetition and single PC (RSPC) code and found that it works well for various ranges of code-rates. To raise the basic cone and to calculate the pseudo-code-words of PC code is studied and found few technologies, also gives some tools to examine the irreducible pseudo-code words. And A theoretical study on matrix transformations is done using Fourier-transforms and permutations. Also, their capacity on white-Gaussian-noise is showed. Also A parity-generator based on uni-resonant-tunneling-bipolar-transistor (RTBT) is described and found that it yields important advantages as compared to previous ones. A virtual memory using hit RAM, which gains fastness and capacity, is proposed which results in less energy usage and delay.

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The code suited to solve burst faults is demonstrated, since the used components is less than their code lengths it is shown as LDPC codes concept and concluded that it is efficient in correcting the faults. Various errors finding PC is described which can totally detect faults with the help of test-patterns that are created from identity and binary matrix which in turn supposed to find various errors which raises wired-OR networks shows the parity checker codes [1]-[9].An altered A* algorithm has been invented to fasten the tree search and concluded that it decreased the tree count as correlated with other A* algorithms. And A part of error-blocks with one-second assemble figure of bit-interleaved parity (BIP) disruption is proposed and evaluated using Poisson-error and error-burst distribution. Also A generator matrix (GM)-depending technique is used and resulted that it needs low calculation time as compared with previous ones. A number of bit-parity depend, error finding technique for parallel CRC calculations is presented, by using some soft ware and ASIC development it is known that it is capable of finding errors that comprises low area and time. Parity vector which build minimized residual-generators is derived and concluded that the error finding probability is upgraded as compared to old techniques. An efficient method of parity-space dependent fault-detection and isolation (FDI) technology straight from input to through put is studied and found to be fruitful at every point. A stationary-wavelet-transform (SWT) is used in the residual wave along with that a novel residual generator, minimization technique is described and correlated with other techniques which found to be successful shows the issues of several techniques [10]-[16]. In the parity checker we use some recordings like A normal and efficient method to merge constrained-codes with parity-check (PC) codes for optical-recording is presented and found that it can rate 2/3-code with no parity at normal as well as high density. Cross-parity-check (CPC) codes to secure the information present in magnetic-tape is proposed and checked, found that it is used to divide the pc matrix by some number and to gain the remainder [17]-[19]. Likewise there are several techniques to detect the errors in the transmission and reception of bits as A new technology of low-density PC (LDPC) producer in china-digital-radio (CDR) is described and enforced on Xilinx FPGA which resulted 400 Mbps output and also reached the error essentials of CDR. Low-density based PC (LDPC) code is designed and studied in three parts with various technologies and found that it is having good performance. An LDPC code using finite-affine-planes is shown and found that it is having high fault detection capability with high rate. A low-density based generator matrix is changed as low-density PC code and concluded that it reduced the encoding difficulty and enhanced the decoder circuit resilience [20] [23].

And the calculations are optimized by following the techniques as A quantum-stabilizer-code is built which is depending on syndrome-assignment through classic PC matrix and studied; finally found that they provide quality through put. An 11-bit pc was described using vertically-integrated-diode (VID) and concluded that it restored huge amount of EX-OR gates in standard PC. With the use of PC encoder an effective design was made which reduced the flip-flop count completely. Here self-testing-embedded (STE) PC was used with EX-OR gate as fundamental block which provided easy and accurate results. A new architecture of systematic-circulant (SC) generator-matrix depending on matrix transforms is demonstrated and concluded that the density reduces automatically with normal mathematical difficulty. The effective encoding of quasi-cyclic (QC) LDPC codes is studied and resulted that the difficulty of the code depends on the number of bits and length of code for serial and parallel encoding respectively [24]-[29].

II. IMPLEMENTED DESIGN:

In this parity checker is structured through the Ex-or gates in transistor level.

A. Existed 8 Transistor Ex-or Design:

In this we implemented the two input Ex-or gate by using the eight transistors. This eight transistors Ex-or design uses the pass transistor logic. This existed 8T Ex-or design shows the highest power utilized, more delay and such that more PDP. To reduce these constraints like power, delay, transistor count, size and PDP.
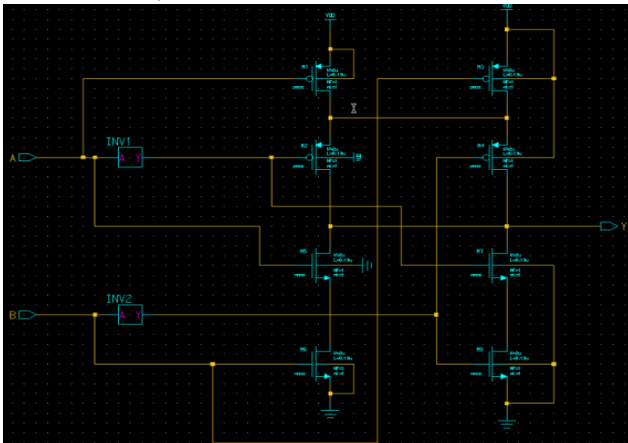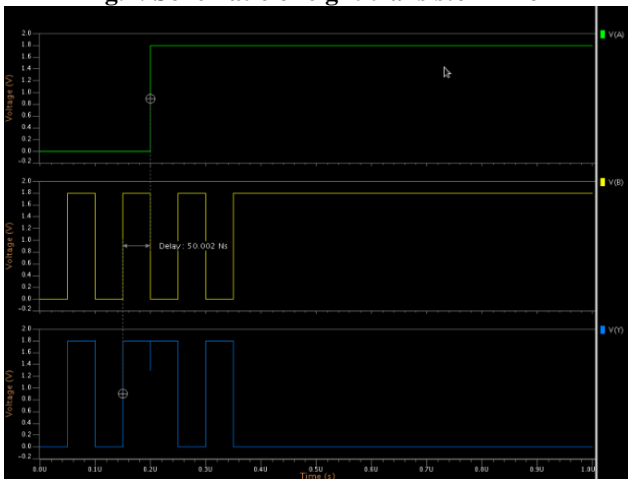

Fig.1: Schematic of eight transistor Ex-or

Fig.2: simulated outcomes of eight transistor Ex-or

B. Implemented 6 Transistor Ex-or Design:

We implemented the two input Ex-or design with six transistors by using the Pass transistor logic (PTL) style. So that the optimized six transistor Ex-or gives low power, less delay, less size, optimized transistor count and reduced PDP.
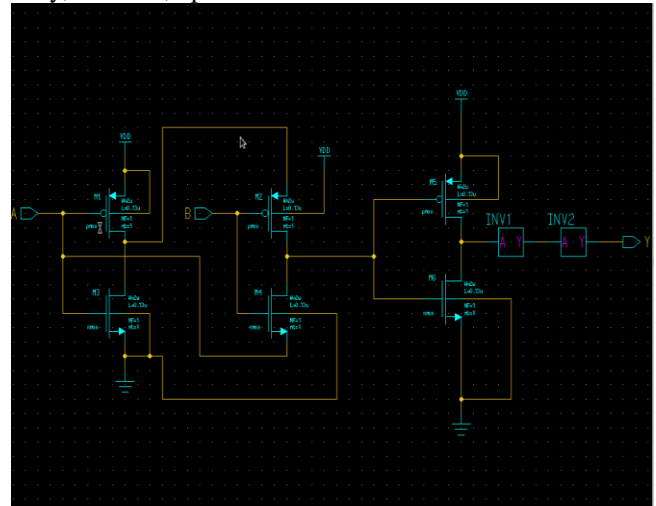

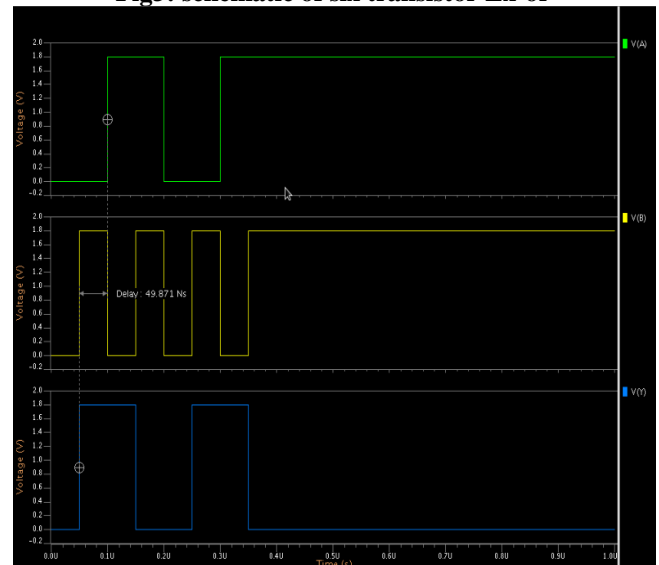**Fig3: schematic of six transistor Ex-or**

Fig4: Simulated outcomes of six transistor Ex-or

The simulated outcomes of 6T Ex-or visualizes in the clear manner without any overshoot and undershoot when compared over the 8T Ex-or design. The constraints of power, delay and PDP are tabulated in the table1.

Table1: comparison between 6T and 8T Ex-or design

S. No	Gate Designed	No.of Transistors used	Power dissipation(nanowatts)	Delay (nanoSeconds)	PDP (attojoules)
1	EX-OR	8	6.4727	50.002	323.6479
2	EX-OR	6	5.6580	50.034	283.0923

:The logic involved to design Ex-or gate is if inputs are two different logic then output is '1'. Otherwise if those two inputs are similar then output is '0'. So by using the both eight transistor Ex-or and six transistor we implemented the parity checker design.

C. Design of Parity Checker:

Parity checker employs a key role in the digital communication for finding out the error bits. The procedure involved in this is if we sends the data from one stage to another stage in the middle there is chance of adding the noise that is the additional data gets added and then it reaches at the receiver. Because of this there is a possibility of modification in the transmitted data that is either from '0' to '1' or '1' to '0'.So to identify that error bit we used the parity bit at the edge of the message signal.
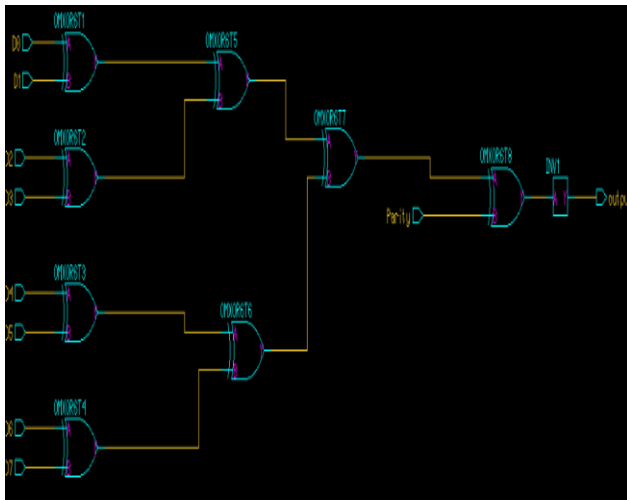

Fig.5: Schematic of Parity checker

Table2: truth Table of Parity Checker

S. No	Input Data	Parity Given	Output
1	Even number of ones	0	1
2	Even number of ones	1	0
3	Odd number of ones	0	0
4	Odd number of ones	1	1

According to the table2 if there are even numbers of ones and if the given input parity bit is zero then the output values that is check shows '1'. In the same for even number of ones if the given parity bit is one then check shows the output as '1'. The parity checker for odd number of ones if the given parity bit is zero then check shows the output value as '1'. The parity checker for odd number of ones if the given parity bit is one then check shows the output value as '0'. So according to the truth table the schematic of parity checker works. The operation involved in parity checker is to identify the errors while sending the data. So the parity checker design first verifies the total number of logical ones is even or odd while transmitting the data. At the receiver it verifies the number of ones that the sent data and received data are same or not. The number of ones at the transmitted data is correlated with the parity bit, which was occurred due to parity producer and specifies the number of bits in advance of sending the data. If number of bits is equated, no errors are shown otherwise if the number of bits at the transmitter and receiver are not equal then there is an error in the data. The schematic is designed to result a '1' if the parity is equal, and a '0' if not.
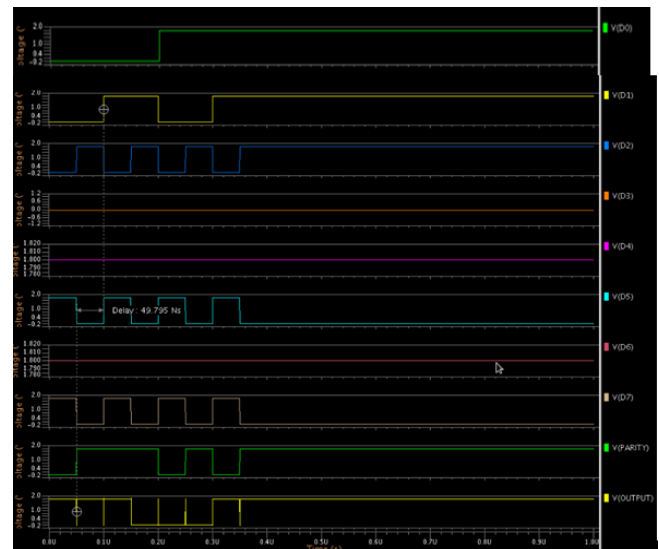
III. SIMULATION RESULTS:

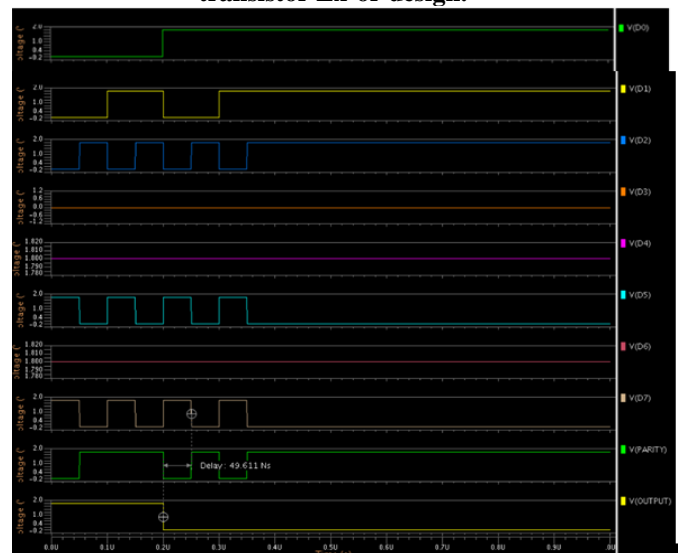**Fig.6: Simulated outcomes og Parity checker with eight transistor Ex-or design.**

Fig. 7: Simulated outcomes of parity checker six transistor Ex-or design.

Table 3: Comparison table of Parity checker eight transistor Ex-or and Parity checker Six transistor Ex-or

S. No	Ex-or used to design parity checker	Power dissipation (nano watts)	Delay (nano Seconds)	PDP (atto joules)
1	EX-OR 8T	47.1539	49.795	2348.0284
2	EX-OR 6T	28.3703	49.611	1407.4789

In this the circuit is simulated by giving all the information bits to modify and to feed in all the probable amalgamations. In this we can check out all the 256 probable bit amalgamations at once, with odd and even parity bit. In this the outcomes are mainly focused to check the parity checker functionality. The focus is mainly verified only when the feed in parity bit is zero that is for the even parity check.

And it shows that the schematic of parity checker is giving correct and proper functionality. But in this the result shows there is an observed delay. This occurred due to the philosophy schematic and the CMOS inverter utilized in the parity checker schematic. This is calculated by observing the time from edge to edge when the result gets modified. The power dissipation for the eight transistor Ex-or parity checker is 47.1539 nano watts and the delay is 49.795 nano seconds and PDP is 2348.0284 atto joules. And the implemented design six transistor Ex-or parity checker Power dissipation is 28.3703 nano watts and delay is 49.611 nano seconds and PDP is 1407.4789 atto joules. This design is implemented at the 1.8V Power supply.

IV. CONCLUSION:

From the literature, it shows that the implemented design is more and well effective in terms of area, power, delay and PDP in correlation with the existed structure. So that the use of this implemented structure is taken into analysis because of the size, and the power delay product for this is very effective. The reduction in the schematic has minimized the constraints like power, delay and PDP among the previous structure. The necessity of the implemented design is more preferable while drawing the minimum outcomes than the previous structure. It clears that 59.57 % of power is reduced when compared to previous structure, likewise 0.0009% of delay is minimized when compared to previous structure, more over the 62.60% of total power delay product is reduced in comparison to the previous structure.

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