

# Design of a 4 bit Arithmetic and Logical unit with Low Power and High Speed



C.Arunabala, Ch. Jyothirmayi, D N S V Sreeja.T, Suma Burra, Hrithika Reddy Udumula, I.R.Anusha Devi

**Abstract:** In this presented work we designed the 4-bit Arithmetic & Logical Unit (ALU) by using the different modules. The Various modules are AND gate & OR gate designed with six transistors, While the XOR modules is designed with both eight transistors & six transistors. The six transistor XOR module gives optimized results. Another one is the four by one multiplexer designed with eight transistors implemented using Pass transistor logic (PTL) style. The full adder module is designed by using 18 transistors implemented through PTL style. Here because of PTL style the number of transistor count optimized such that the constraints get optimized results. By using the AND, OR, XOR, 4X1 MUX and full adder modules with reduced transistor count we designed the one bit ALU. With one bit ALU we designed 4 bit ALU and compared the outcomes with conventional 4 bit ALU design so that the proposed 4 bit ALU design has optimized transistor count, area, power, delay and power delay product (PDP). Simulations are verified through 130nm mentor graphics tool.

**Key terms:** Pass Transistor Logic (PTL) style, power delay product (PDP), Arithmetic and logic unit (ALU), mentor graphics tool.

## I. INTRODUCTION

The ALU is designed with techniques as A quantum-dot-cellular-Automata (QCA) is used to design ALU and the executed output proved that this design is efficient in terms of cell count, place and energy utilization. And A new structure of magnetic ALU depending on the combination of Spin-transfer-torque-magnetic-tunnel-junction/CMOS devices is proposed and concluded that they can provide low energy consumption with less transistors. The layout and utilization of ALU based on logarithmic structure is proposed and analyzed on various arithmetic functions. Finally, concluded that the designed one is providing fast output.

Also The modeling and analysis of 8-bit-asynchronous signal-pipelined –sparse tree Rapid-single-flux-quantum(RSFQ) ALU is done & Correlated with earlier ones, found that it has decreased the design complexity and can perform 8 mathematical and 12-logical functions. An ALU based on RSFQ is developed and constructed using HYPRES' technique which provided the output with less delay. K-bit-binary-integers depending on discrete-logarithm-number-system (DLS) which offers integer-multiply to decrease to addition as well as integer-exponency to decrease to multiply. Results concluded that it is effective & can be extended to 16-bit also. A technology to improve all optical ALU for performing various binary & arithmetic functions can be done by exactly opting the frequencies and encoding them and found that effectiveness and switching-speed is high. So that An asynchronous-logic quasi-delay-insensitive (QDI) acknowledgment access for less energy sub-limit activity is proposed and resulted that it optimized the gain rate for stable yield states and provided low energy with rapid output. Such that A new automated debugging technique for arithmetic design is used and found that it is powerful in all required calculations at high speed, can find and replace the error automatically Here different techniques are used to design ALU A less – energy 1- GHz four-bit time based arithmetic-logic-unit (ALU) addressing hard-ware conventional accelerator is Proposed and found that it can provide fastness with low power utility. Also With the utilization of Threshold logic gates (TLG's), a 4-bit ALU is demonstrated and concluded that it showed comparative outcomes from the ALU's executed in the FPGA assessment unit. And To design 32/64 bit RSFQ micro-Processor, a 16-bit based bit-slice-ALU is proposed and came to know that it is capable of executing every type of sixteen n-bit functioning. Such that A new technique based on system-on-chip to construct data-flow graphs is designed and concluded that it decreased 46 percent of the critical path along with cell region. In this the ALU is designed to minimize the Power, To find faults in various computational functions using pipelined structures, mostly systolic ones is demonstrated and found that they have high capacity in detecting errors as compared to earlier methods. And High Velocity, high return ALU's worked at scaled stockpile voltage with versatile clock extending is demonstrated and found that Hybrid units come about measure of quick math into the more slow ones & it show 18 percent half enhancements & 2 to 8 percent expansion in die-region at Iso-yield.

Manuscript received on March 12, 2021.

Revised Manuscript received on March 19, 2021.

Manuscript published on March 30, 2021.

\* Correspondence Author

**Dr.C.Arunabala\***, E.C.E, JNTUK, Guntur, India. Email: [arunabala4700@gmail.com](mailto:arunabala4700@gmail.com)

**Ch.Jyothirmayi**, E.C.E, JNTUK, Guntur, India. Email: [jyothirmayi.93@gmail.com](mailto:jyothirmayi.93@gmail.com)

**D N S V Sreeja.T**, .C.E, JNTUK, Guntur, India. Email: [sreejatanuguntla@gmail.com](mailto:sreejatanuguntla@gmail.com)

**Suma Burra, Hrithika** .C.E, JNTUK, Guntur, India. Email: [suma.b413@gmail.com](mailto:suma.b413@gmail.com)

**Reddy Udumula**, .C.E, JNTUK, Guntur, India. Email: [reddyhrithika939@gmail.com](mailto:reddyhrithika939@gmail.com)

**I.R.AnushaDevi**, E.C.E, JNTUK, Guntur, India. Email: [illaanusha431@gmail.com](mailto:illaanusha431@gmail.com)

© The Authors. Published by Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP). This is an [open access](https://creativecommons.org/licenses/by-nc-nd/4.0/) article under the CC BY-NC-ND license (<http://creativecommons.org/licenses/by-nc-nd/4.0/>)

Such that An ALU 4-bit, bit-slice for 32-cycle fast single-flux-quantum performs bit-sliced processing i.e., 32-bit information that are Partitioned into 8 four-bit slices is described and concluded that it works on the structure of the circuit & decreases the equipment cost with better output. And An equal 8-bit ERSFQ number- crunching rationale unit (ALU) is described and found that at low recurrence, clock and all rules proliferation through ALU were seen with predisposition edges of +/- 11, +/- 9 percent individually and at low speed it showed all calibrations perfectly.

In this DNA- based reversible ALU capable of 4 logical & 3 arithmetic functions is described and resulted that it is quicker, needs less area and power as compared to the other techniques. To support the reduction of functioning fault an Array-based- approximate-arithmetic computing (AAAC) is described along with error-compensation-unit (ECU) and concluded that it reduced area, power utilization and delay in a better way. Stateful rationale task based on Complementary resistive switching (CRS) utilize material ramifications with memristors is proposed and achieved best results using cadence tool. And With single-spin rationale an ALU is proposed by setting the quantum dots in explicit mathematical examples to understand the ideal links among the info & yield turn states. So that Test-pattern-generators (TPG's) in math activities are getting practical implicit-individuals test solutions for circuits with inserted processors is studied and found that it limits the test time by 43.47 percent as compared with previous ones. Such that Reconstructable bend based crypto processor that quickens scalar augmentation of elliptic curve cryptography (ECC) & hyper elliptic curve cryptography (HECC) is designed and resulted with fast and accurate outcomes.

And to minimize the Calculations A math unit for finite-field-  $GF(2^m)$  plays out all fundamental arithmetic tasks, where  $m$  is an absolute whole number is proposed and observed that it is programmable & has low circuit intricacy. So, any mistake – revising decoder is easily actualized. So that Zero anticipation with error correction is the strategy used to actualize the rapid drifting point units and eliminated the blunder amendments with less size and error-rate. Such that A new method for demonstrating the accuracy of math circuit plans portrayed at the register transfer level (RTL) is done and found that this is utilized to discover the confirmation of various multipliers that is hard to streamline with the current devices & methods.

## II. PROPOSED DESIGN

### A. Behavior of CMOS Circuits in Terms of Power Dissipation:

The constraint power can be defined in three terms there are short circuit, static and dynamic Power. The constraint static is the multiplication of VDD and direct current. This occurs due to unwanted elements in the design. And its equation is

$$P_s = \sum_n I_i V_{dd} \quad (1)$$

Where  $m$  is number of circuits used dynamic can be defined as power consume by the circuits in the design. This moulds on switching. Here it is depends on  $V_{dd}^2$  and written as

$$P_d = \sum_n C_l V_{dd}^2 f_c \quad (2)$$

$C_l$  is the load capacitance,  $V_{dd}$  is the supply given to circuit and  $f_c$  is the switching frequency. So the composited power can be defined as summation of static and dynamic power.  $P_{total} = P_s + P_d$  in this for the optimization of total power we concentrate on  $C_l$ ,  $V_{dd}$  these can be optimized by minimizing the number of transistors.

### B. Circuits Involved Designing Four Bit ALU:

In this first we will design the one bit ALU and then the circuits required to design the one bit ALU are AND, OR, EX\_OR, four by one multiplexer and Full Adder. So procedure involved in this is first we design the AND gate and OR gate with six transistor and EX-OR with Eight transistors and six transistors with pass transistor Logic (PTL) style. So for power minimization we used the six transistor EX-OR. While going to 4x1 mux we designed it with 8T in PTL style. So one by one design is explained below.

And gate:

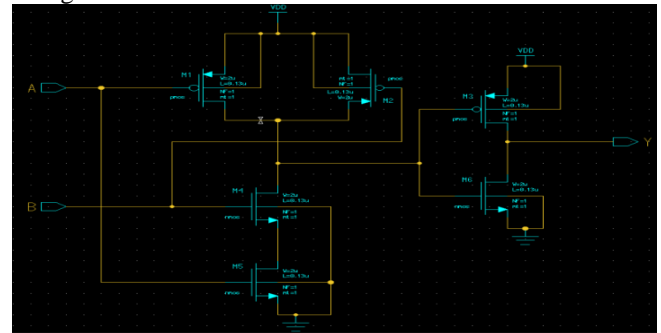


Figure (1): Schematic of AND gate in transistor level

AND gate consists of 6T in this the logic involved is to if the two inputs are logic high then only the output is logic high. In other cases, output is logic '0'. This supports multiplication and does the logical operation.

OR gate:

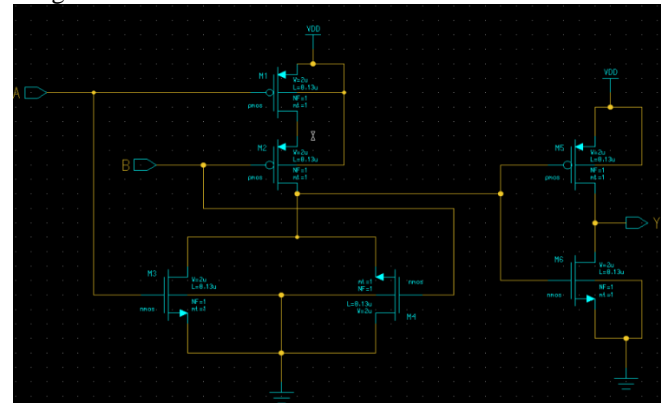


Figure (2): Schematic of OR gate in transistor level

OR gate consists of 6 transistors in this the logic involved is if any of the input is logic high then the output is logic high. In other cases the output is Logic '0'. This supports addition and does the logical operation.

EX-OR gate:

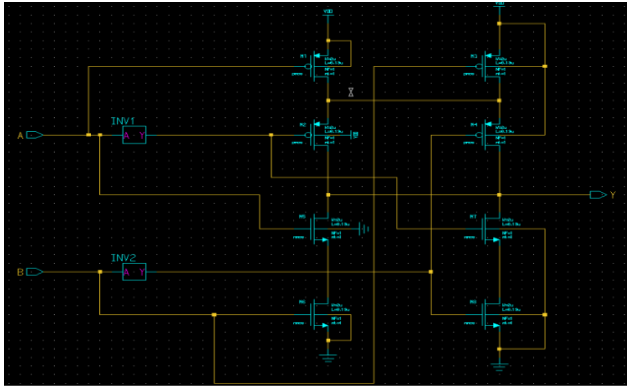


Figure (3a): Schematic of EX-OR gate in transistor level with eight transistors

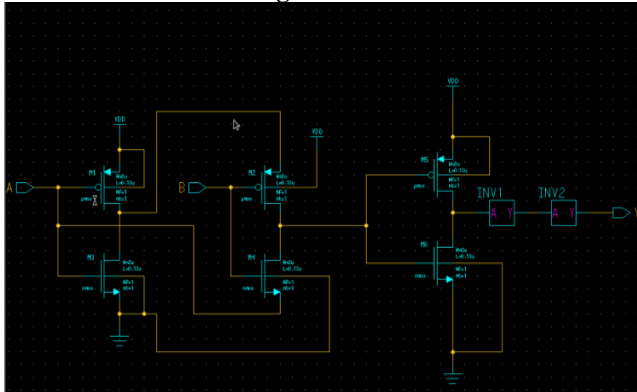


Figure (3b): Schematic of EX-OR gate in transistor level with six transistors

In this EX-OR gate is designed in Pass transistor logic style with two models. Those are one with 8T and second one is the optimized design of 6T in terms of Power, Delay and Power Delay Product (PDP). In this an extra tailing inverter is added to maximize the less quality of the signal with high quality. And the Comparison between EX-OR 8T and 6T in terms of Power, Delay and PDP are shown in table given below.

Table(1): Comparison table of EX-OR with Eight and six transistor

S.No	Logic used	Design	Power (nano watts)	Delay (nano Seconds)	PDP (atto joules)
1	PTL	XOR 8T	6.4727	50.002	323.6479
2	PTL	XOR6T	5.6580	50.034	283.0923

Four by one multiplexer:

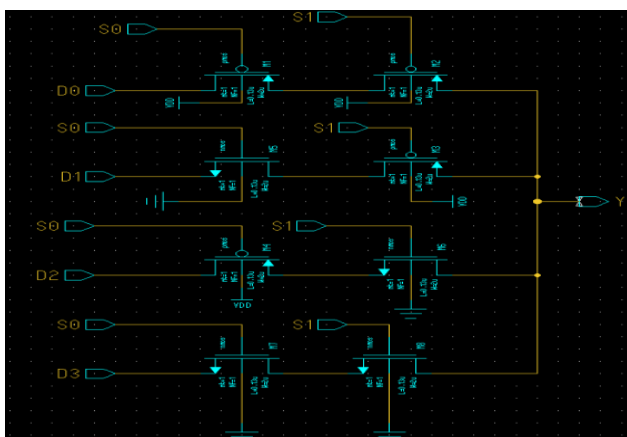


Figure (4): Schematic of four by one multiplexer in transistor level with eight transistors

The 4x1 mux design is having four inputs and one output. In this the design consists of 8T which follows PTL style. Such that the power, delay and PDP get optimized. The 4x1 mux PTL and CMOS styles comparison is shown in Table(3).

Table(3): Comparison table of four by one multiplexer with CMOS and PTL logics.

S. No	Logic used	Design	Power (nano watts)	Delay (nano Seconds)	PDP (atto joules)
1	CMOS	Existed Multiplexer	16.477	0.0201	0.346
2	PTL	Multiplexer with 8T	0.0252	0.0039	0.0001

Full Adder:

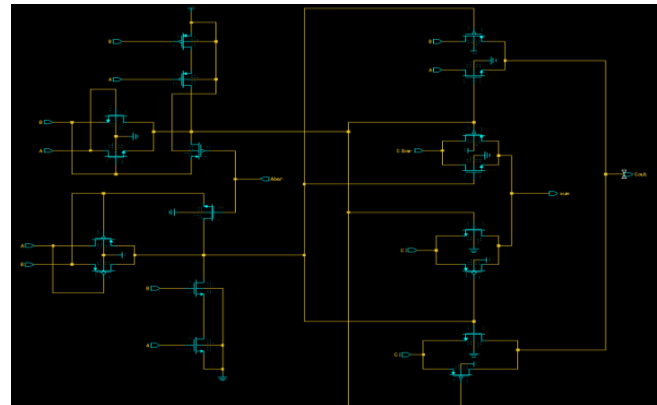


Figure (5): Schematic of Full Adder in transistor level with twenty two transistors

In this the full adder design consists of 22T with optimized Power, Delay and PDP. And this has followed PTL style. And the comparison table (2) of CMOS and PTL styles is shown below. And the logical expressions are given below  
 $SUM = A \oplus B \oplus C_{in}$   
 $CARRY = AB + BC_{in} + C_{in}A$

Table (2) Comparison table of Full Adder with CMOS and PTL logics

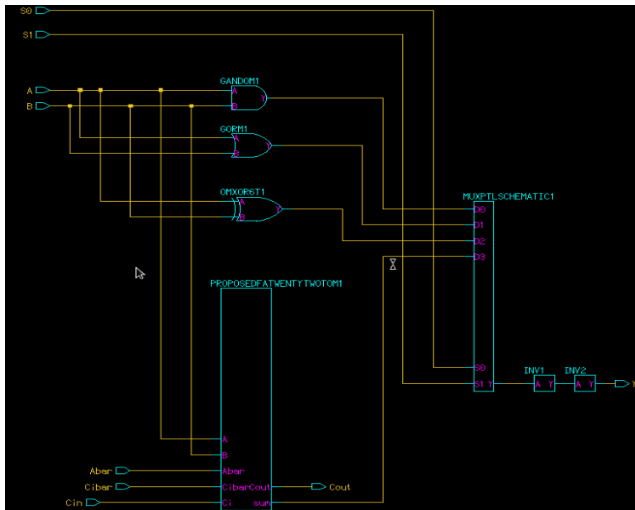
S.N o	Logic used	Design	Power (nano watts)	Delay (nano Seconds)	PDP (atto joules)
1	CMOS	Existed FULL ADDER	27.6902	49.894	1381.574
2	PTL	FullAdder with 22T	8.9266	0.0160	0.1436

One bit ALU:

By utilizing the above all designs we proposed the one bit Arithmetic and Logical unit which performs Arithmetic operations through full adder and logical operations through AND, OR, EX-OR and these four are given as input to the 4x1 mux. And that 4x1 mux performs the arithmetic and logical operations and gives the output based on the figure (7) below.

# Design of a 4 bit Arithmetic and Logical unit with Low Power and High Speed

And the truth table is shown in table(4)



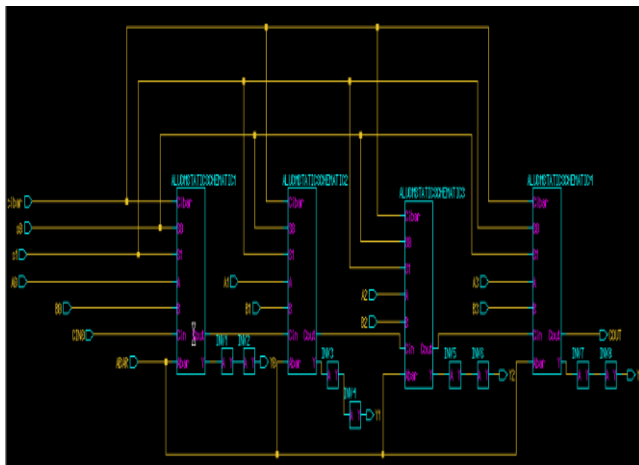
**Figure (7): Schematic of one bit ALU Design**

**Table (4): Truth Table of one bit ALU**

S.No	S1 (MSB)	S0 (LSB)	Operation
1	0	0	AND
2	0	1	OR
3	1	0	XOR
4	1	1	Full Adder

Here s1 is the MSB and s0 is the LSB.

Four bit ALU Proposed DESIGN:



**Figure (8): Schematic of Four bit ALU Design**

Figure (8) shows the schematic diagram of four bit ALU which gives one arithmetic and three logical functionalities. The three logical functionalities are AND operation, OR operation and EX-OR operation. The one arithmetic functionalities are addition. We composited four one bit ALU to get Four bit ALU Design. Each stage of ALU consists of AND, OR, EX-OR, Full Adder and 4x1 multiplexer. The 4x1 mux is at the output side designed with PTL style to optimize Power, Delay and PDP. The multiplexers are required to fed the correct feed in to the full adder design based on the functionality done at the feed in side. And the output of Full Adder is given to the ALU. Figure (5) shows the schematic of full adder and figure (6) shows the schematic of 4x1 multiplexer. Here the full adder gives Sum and Cout as outputs. Where Cout is given to Succeeded ALU Cin and then Soon. And SUM as y0, y1, y2 and y3. Here the logical functionalities are done

through the basic logic gates, such that the delay for every logical functionality will be the delay over the gate. In this the arithmetic operations will make use of adder design. When compared to arithmetic and logical operations the time requirement is more for arithmetic because it involves addition or summation operations and it is very difficult. The logical functionalities delay depends on gates used to design the full adder circuit to give the Sum and CARRY operations and also on the feed in given to the circuit and the critical path followed by that. Reducing the full adder reduces the functionalities. The logical statements are defined as

$$\text{Sum} = A \text{ xor } B \text{ xor } \text{Cin} \quad (3)$$

$$\text{Carry} = AB + BC_{\text{in}} + C_{\text{in}}A \quad (4)$$

Where A,B,Cin are inputs. Cin is carryin to the Full Adder. As shown in Table(4) the functionalities of ALU are defined at which s1 is the MSB and s0 is the LSB. In the 4x1 multiplexer makes necessary functionalities for the logics given. For the input s1=0 and s0=0 it do the anding operation. For s1=0 and s0=1 the ALU performs oring operation. For s1=1 and s0=0 the ALU gives EX-Or functionality. For s1=1 and s0=1 the ALU performs addition operation through Full Adder circuit. The Full Adder circuit gives two outputs as SUM and Carryout. Defined as y0 and Cout. The cout is connected as o cin the next ALU and then the second ALU cout to third ALU cin and third ALU cout to fourth ALU cin and at the edge the four bit gives y0, y1, y2, y3 and Cout. In this the y0, y1, y2, and y3 gets in parallel.

The four bit ALU looks like the ripple carry adder which the carry ripples from one to other. For some inputs it doesnot curls, for some the ripple occurs from LSB to MSB. In this advantage is the propagation delay optimized in a maximum manner. For logical functionality the delay is equal for every stage of ALU. Here the delay of carry will transfer from LSB to MSB. And defined as delay depends on number of bits in input words as and is given by the equation as

$$T_{\text{adder}} = (M-1) t_{\text{carry}} + t_{\text{sum}} \quad (5)$$

Where  $t_{\text{carry}}$  and  $t_{\text{sum}}$  are propagation delays from first stage to fourth stage. The ALU was designed in 130nm Mentor graphics tool with 1.8V power supply.

## III. RESULTS AND DISCUSSIONS

In the results session we explained the one bit and four bit simulated waveforms are visualized in Figure (9) and Figure(10). Mainly in this the aimed results like Power, area delay and PDP constraints are reduced at maximum. And these are designed with the 1.8V power supply. Here the constraints like power, area, delay and PDP are reduced because of the reduction in the transistor count at every module of the one bit design and Four bit ALU design.



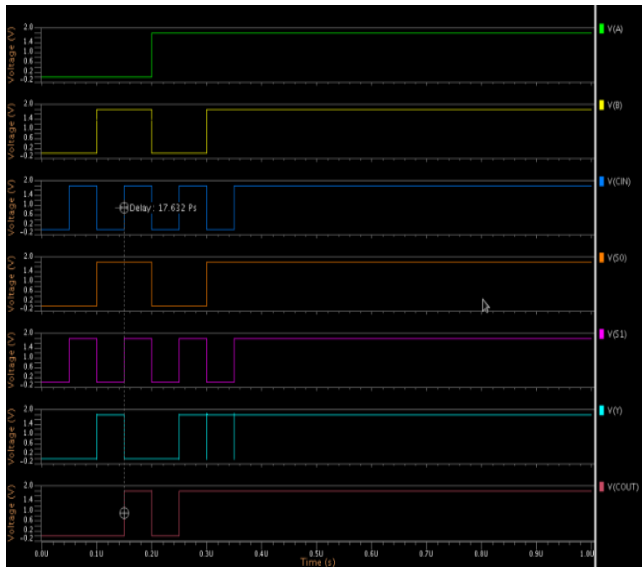


Figure (9): Simulated waveforms of one bit ALU design

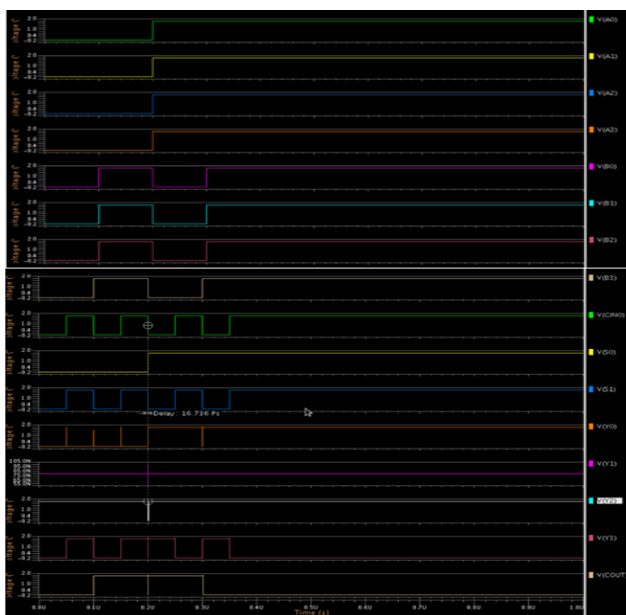


Figure (10): Simulated waveforms of Four bit ALU design

Table (5) Comparison table of one bit and Four bit ALU design

S.No	Logic used	Design	Power (nano watts)	Delay (nano seconds)	PDP (joules)
1	CMOS	One bit ALU	66.1784	49.810	3296.346 atto joules
2	Hybrid	One bit ALU	21.5749	0.017632	0.3804 atto joules

S.No	Logic used	Design	Power (nano watts)	Delay (nano seconds)	PDP (joules)
1	CMOS	Four bit ALU	2640.7135	49.5	130.715 atto joules
2	Hybrid	Four bit ALU	3780	0.016736	63.26 atto joules

#### IV. CONCLUSION

The outcomes visualizes the CMOS circuits involved with Pass transistor Logic(PTL) style gives good design with optimized power, delay and PDP. Here in this the transistor count has reduced such that automatically the power, delay and PDP are reduced. And the simulated outcomes visualizes that the proposed ALU is ----- more efficient when compared to the existed ALU design. The proposed design requires less power and delay such that PDP is also less. This proposed or implemented circuit has more advantages in VVLSI design that is especially in low power design. And moreover, it is tolerable for noise and gives better output.

#### REFERENCES:

1. Swaroop Ghosh, "Voltage Scalable High-Speed Robust Hybrid Arithmetic Units Using Adaptive Clocking", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 18, No. 9, Sept. 2010, pp. 1301-1309.
2. Aurangozeb, "Time-Domain Arithmetic Logic Unit with Built-In Interconnect", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 25, Iss. 10, Oct. 2017, pp. 2828 – 2841.
3. Shahram Babaie, "Design of an efficient Multilayer Arithmetic Logic Unit in Quantum-dot Cellular Automata (QCA)", IEEE Transactions on Circuits and Systems II: Express Briefs, Vol. 66, Iss. 6, June 2019, pp. 963 – 967.
4. Medina-Santiago, "Reconfigurable arithmetic logic unit designed with threshold logic gates", IET Circuits, Devices & Systems, Vol. 13, Iss. 1, 2019, pp. 21-30.
5. Prashanth Barla, "A Novel Low Power and Reduced Transistor Count Magnetic Arithmetic Logic Unit Using Hybrid STT-MTJ/CMOS Circuit", IEEE Access, Vol. 8, 2020, pp. 6876-6889.
6. Siavash Bayat-Sarmadi, "Concurrent Error Detection in Finite-Field Arithmetic Operations Using Pipelined and Systolic Architectures", IEEE Transactions on Computers, Vol. 58, No. 11, Nov. 2009, pp. 1553-1567.
7. S. Carrillo, "Design and Implementation of an Arithmetic Processing Unit Based on the Logarithmic Number System", IEEE Latin America Transactions, Vol. 8, No. 6, Dec. 2010, pp. 605-617.
8. Mikhail Dorojevets, "8-Bit Asynchronous Sparse-Tree Superconductor RSFQ Arithmetic-Logic Unit with a Rich Set of Operations", IEEE Transactions on Applied Superconductivity, Vol. 23, No. 3, June 2013.
9. T. Filippov, "8-Bit Asynchronous Wave-Pipelined RSFQ Arithmetic-Logic Unit", IEEE Transactions on Applied Superconductivity, Vol. 21, No. 3, June 2011, pp. 847-851.
10. Omid Sarbishei, "A Formal Approach for Debugging Arithmetic Circuits", IEEE Transactions on Computer-Aided Design of Integrated Circuits And Systems, Vol. 28, No. 5, May 2009, pp. 742-754.
11. Ankur Sarker, "Design of a DNA-Based Reversible Arithmetic and Logic Unit", IET Nano biotechnology, Vol. 9, Iss. 4, 2015, pp. 226 – 238.
12. Alexandru Fit-Florea, "A Discrete Logarithm Number System for Integer Arithmetic Modulo 2k: Algorithms and Lookup Structures", IEEE Transactions on Computers, Vol. 58, No. 2, Feb. 2009, pp. 163-174.
13. Botang Shao, "Array-Based Approximate Arithmetic Computing: A General Model and Applications to Multiplier and Squarer Design", IEEE Transactions on Circuits And Systems, Vol. 62, No. 4, April 2015, pp. 1081-1090.
14. Guang-Ming Tang, "4-bit Bit-Slice Arithmetic Logic Unit for 32-bit RSFQ Microprocessors", IEEE Transactions on Applied Superconductivity, Vol. 26, Iss. 1, Jan. 2016.
15. Sisir Kumar Garai, "A Novel All-Optical Frequency-Encoded Method to Develop Arithmetic and Logic Unit (ALU) Using Semiconductor Optical Amplifiers", Journal of Light wave Technology, Vol. 29, No. 23, Dec. 2011, pp. 3506-3514.
16. Guang-Ming Tang, "Logic Design of a 16-bit Bit-Slice Arithmetic Logic Unit for 32-/64-bit RSFQ Microprocessors", IEEE Transactions on Applied Superconductivity, Vol. 28, Iss. 4, June 2018.

17. Tung-Chou Chen, "Arithmetic Unit for Finite Field  $GF(2^m)$ ", IEEE Transactions on Circuits and Systems, Vol. 55, No. 3, April 2008, pp. 828-837.
18. Weng-Geng Ho, "Low power sub-threshold asynchronous quasi-delay-insensitive 32-bit arithmetic and logic unit based on autonomous signal-validity half-buffer", IET Circuits Devices Syst., Vol. 9, Iss. 4, 2015, pp. 309–318.
19. Mauro Olivieri, "Analysis and Implementation of a Novel Leading Zero Anticipation Algorithm for Floating-Point Arithmetic Units", IEEE Transactions on Circuits And Systems, Vol. 54, No. 8, Aug. 2007, pp. 685-689.
20. F. Kirichenko, "ERSFQ 8-bit Parallel Arithmetic Logic Unit", IEEE Transactions on Applied Superconductivity, Vol. 29, Iss. 5, Aug. 2019.
21. Ajay K. Verma, "Data-Flow Transformations to Maximize the Use of Carry-Save Representation in Arithmetic Circuits", IEEE Transactions on Computer-Aided Design of Integrated Circuits And Systems, Vol. 27, No. 10, Oct. 2008, pp. 1761-1774.
22. Yuanfan Yang, "Complementary Resistive Switch Based Arithmetic Logic Implementations Using Material Implication", IEEE Transactions on Nanotechnology, Vol. 15, Iss. 1, Jan. 2016, pp. 94-108.
23. T. Basu, "Arithmetic logic unit of a computer based on Spin-polarized single electrons", IET Circuits Devices Syst., Vol. 1, Iss. 3, 2007, pp. 194–199.
24. Kazuo Sakiyama, "Multicore Curve-Based Cryptoprocessor with Reconfigurable Modular Arithmetic Logic Units over  $GF(2^n)$ ", IEEE Transactions on Computers, Vol. 56, No. 9, Sept. 2007, pp. 1269-1282.
25. Salvador Manich, "Minimizing Test Time in Arithmetic Test-Pattern Generators With Constrained Memory Resources", IEEE Transactions on Computer-Aided Design of Integrated Circuits And Systems, Vol. 26, No. 11, Nov. 2007, pp. 2046-2058.
26. Shobha Vasudevan, "Automatic Verification of Arithmetic Circuits in RTL Using Stepwise Refinement of Term Rewriting Systems", IEEE Transactions on Computers, Vol. 56, No. 10, Oct. 2007, PP. 1401-1414.

## AUTHORS PROFILE



**Dr.C.Arunabala, M.Tech, PhD, Professor** is having 25 years of teaching experience. Presently she is working as Professor in Department of ECE, KKR&KSR Institute of Technology and Sciences (KITS), Guntur, Andhra Pradesh, India. Totally 15 publications are there in various journals. Her areas of interest are VLSI, Embedded systems, Digital systems and Image processing.



**Ch.Jyothirmayi**, Assistant Professor received her B.Tech degree from KKR & KSR Institute of Technology and Sciences, Guntur (D.t), Andhra Pradesh. And M.Tech degree from St.Mary's womens Engineering College. Guntur (D.t), Andhra Pradesh. And have 3 years of teaching experience as an Assistant professor in various engineering colleges, Currently working as an Assistant professor in Department of ECE in Hindu College of Engineering and Technology Amaravathi Road, Guntur (Dt), Andhra Pradesh, India. Totally 02 publications are there in various journals. Areas of interests are VLSI, Signal Processing, and wireless communication.