Low Noise and high linearity Wide-band Low Noise Amplifier for 5G Receiver Front End System

M. Ramana Reddy

Abstract*: This work Demonstrates a wideband LNA for 5G receiver front end modules with high linearity, Low noise reused topology has an inter stage wideband inductor based two common source cascade stages. The configuration provides the bias current; better Noise figure increases the forward gain. By providing RC Series network at gate terminal of second stage the return losses are reduced and stability will be increased. After pre and post simulation all parameters are better than the existing LNAS. After post simulation results, the Noise figure is achieved less than 1dB and forward gain as flat 16dB for wide band width of 1.5 – 5.5 GHz. At the 1dB compression point the output is 20dbm achieved and OIP3 IS +40dbm is achieved. The chip size of an LNA along with pad is 0.64mm2. The design is GaAspHEMT process at 50nm technology.

***Keywords*: LNA, OIP3, pHEMT, Noise figure, Forward gain .**

I. INTRODUCTION

Recent years the 5G communications systems are popular because of huge data rate, economical , high reliable small size. Theses all parameters are possible by chosen technology and selected band frequency. The preferable band frequencies for 5G IS SUB- 6 GHz and mw wave frequencies. Usually the mm wave frequencies are suitable for military applications. For 5G systems required many process steps for design and implementation to increase data rate, high reliable .increase the coverage area the transceiver required better sensitivity and more dynamic range.

The most important block in any receiver is LNA. The LNA can play an important role in the entire performance of receiver. The most important parameter in any LNA design and its performance forward gain S_{21}, Input and output matching network Noise Figure, linearity , IIP3 , OIP3 and 1dB compression point . The CMOS technology has drawback of highest Noise Figure, Small gain and less linearity. But low cost and better system integration [1] – [2]. The GA As, pHEMT process of technology of compound semiconductor (III –IV group periodic table components) process has Low Noise, high linearity advantages. This is widely used in in industry as well as academic fields [3]. In order to meet requirements the all existing published work papers authors suggested that different topologies andtechnology processes. In reference [4] the authors suggestedthe current reuse technology with cascaded inter stage resonance is demonstrated for the design of LNA, but design is restricted for 5.2 GHz frequency with minimum substrateresistance.

Similarly in gm boosting with current reusetechnique is implemented. Similarly in reference [6] a 5.7 GHz differential mode LNA is designed. In this proposedLNA a wideband low noise, high linearity GaAs pHEMT technology with two stage common source transistor cascaded current reused technique with enhanced matchingnetwork at inter stage.

II. PROCEDURE FOR PAPER SUBMISSION

The two stages cascaded common source (cs) current reused topology the bias current is shared in two stages, so that the power consumption is reduced .The different types of current reuse topologies are shown in figure below.

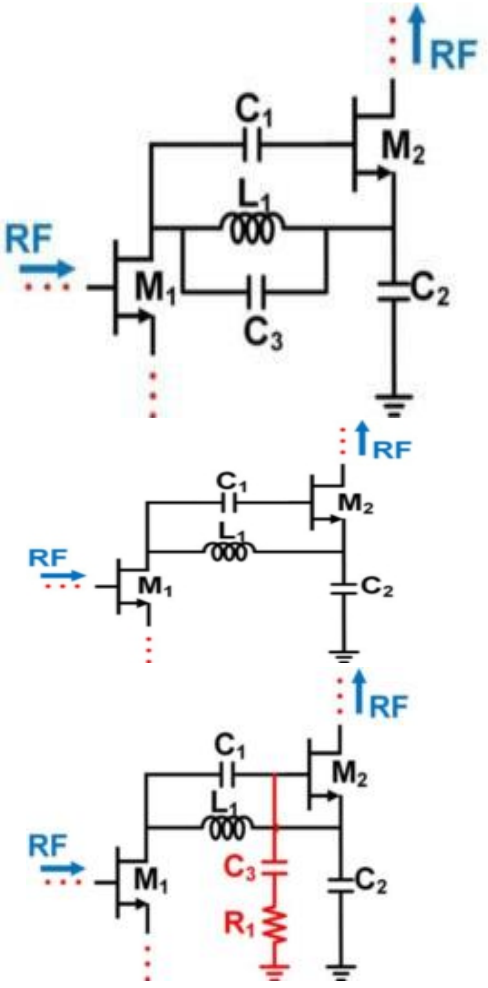

Figure: 1 Different Current reused topologies a) Resistive b) Inductive c) LC Resonant based d) The proposed topology

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From fig. 1.a resistance inter stage current reuse network reduces the voltage, but its noise characteristics increased the power consumption. Fig 1.b due to inductance the chip size will increase and it occupies large area, fig 1.c it also occupies more area but increases the gain. Fig 1.d the proposed two stages cascaded enhanced inters stage matching RC network helps to increases the gain, stability and return losses. The inter stage network can play an important role for better performance of the proposed wideband LNA design.

The proposed wideband LNA design schematic is shown in figure 2. An enhanced mode GaAs pHEMT process of 50nm technology achieved a better performance of parameters especially high linearity and Noise figure.

Table1: Proposed Values in wideband LNA design

PARAMETER	DESIGNED VALUE
M_1	8 × (0.75 µm)
M_2	8 × (0.75 µm)
C_{in}	100.0 pF
C_{out}	100.0 pF
R_b	2.0 kΩ
L_{dd}	18.0 nH
V_{bias1}	0.6 V
V_{bias2}	3.0 V
V_{DD}	5.0 V
I_{DD}	60.0 mA

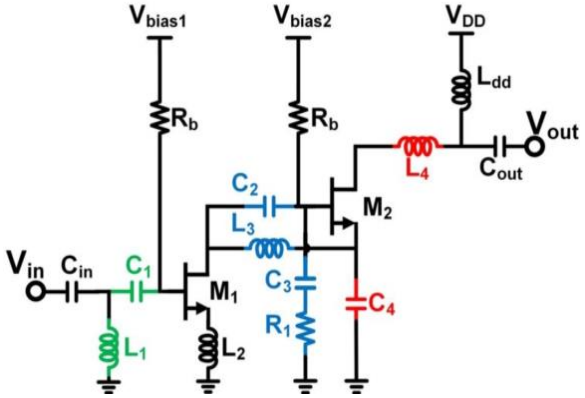


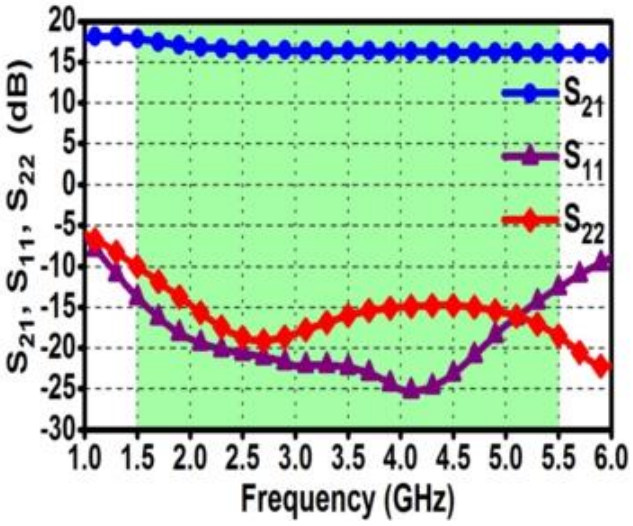
Fig 2: Proposed Wideband LNA

The depletion mode required a negative power supply. So it is replaced with enhanced mode, to provide negative supply to depletion mode the number of components are increased so that chip size will increased. Hence the enhancement mode pHEMT transistor is chosen with gate width of 75 µm and number of figures are 8 for both stages in order to get better noise and linearity performance and also with 5v,60ma current supply. In the schematic C_{in}, C_{out} and L_{dd} are the external connections. The L_1 and C_1 is used as a input matching network. The source degenerated inductor is used for better input matching, so that decrease the Noise. The output matching is achieved by L_4 and C_4 at the M_2 transistor of source terminal .The RC network at the gate of transistor M2 is to increase stability and also improves the return losses. The inductor to be chooses in small size in order to reduce the chip size.

III. SIMULATED RESULTS AND DISCUSSIONS

The post simulated results are achieved the better performance by EM simulator of Agilent ADS software. The proposed wideband LNA micrograph is shown in figure 3 and the occupied area of 0.64mm$^{2.}$ The proposed wideband LNA achieved better performance with single power supply 5V and it dissipates 300 mW. The S_{21}, S_{11} and S_{22} parameters are simulated and shown in figure 4. A stable flat forward gain (S_{21}) 16dB is achieved and shown in figure

5. The input / output return losses are less than -1db in the frequency range of 1.5GHz -5.5GHz. The reverse isolationis less than -25dB is achieved in the required band. The post layout simulation are shown figure infigure 5.



. Fig 3: Simulation results of S21, S11and S22

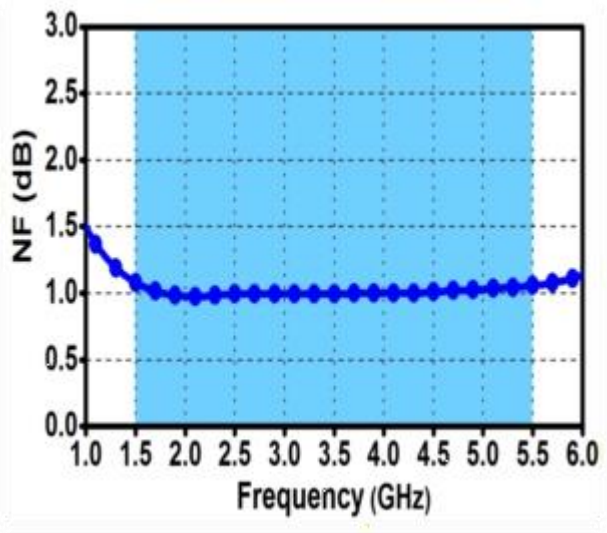


Fig.4: Simulation result of Noise Figure

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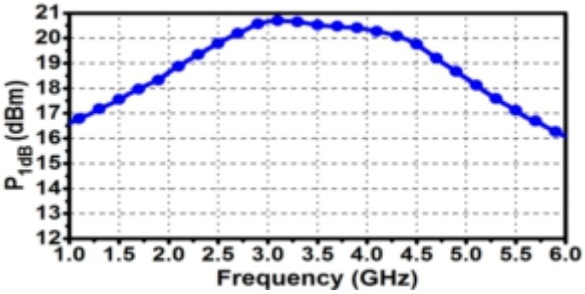

Fig.5: 1dB Compression point

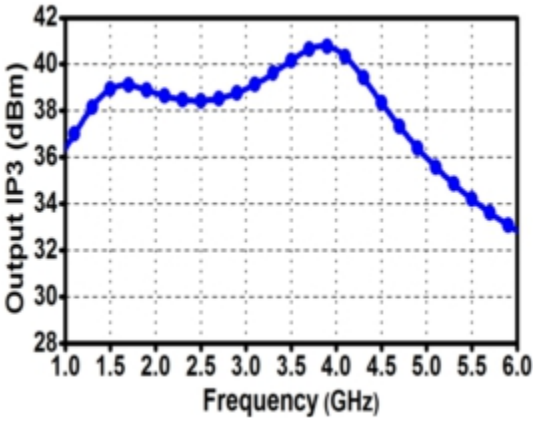

Fig.6: Output Interception Point (OIP3)

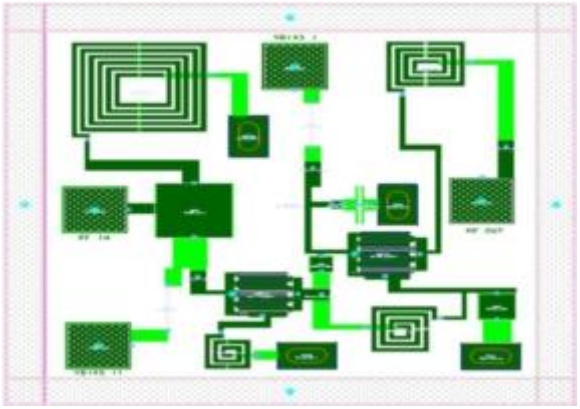

Fig.7: Micrograph for proposed Wideband LNA

Table: 2 Comparison of Parameters of references with present work

PARAMETER	[10]	[9]	[8]	[7]	**0.5 µm GaAs pHEMT**
Technology	0.35 µm	0.50 µm AlGaAs/GaAs	0.5 µm	0.25 µm	
	GaN HEMT	pHEMT	In GaAs	GaAs pHEMT	
			pHE MT		
Freq (GHz)	2 – 4.5	2.5 -5.0	3.5	1.5 - 2.7	**1.5 - 5.5**
BW (GHz)	2.5	2.5		1.2	**4.0**
Gain (dB)	17.2	17	16.7	17.5	**16**
NF (dB)	2.9	3.0	1.8	0.75	**1.0**
IRL/ORL(dB)	<-9.5	<-10	<-9		**<-15**
OIP3 (dBm)	-	-	-	>34	**>34**
P1db (dBm)		2.3	10		**17**
Pdc (mW)	230	33	11.4	300	**300**
Chip Area	2.25	1.5		1.948	**0.64**

other important parameter is Noise Figure (NF) is achieved the 1.5GHz - 5.5GHz wideband frequency range. The post layout simulation result of 1db compression point is 17dbm to 20.5dbm max over the frequency range of 1.5 to 5.5GHz as shown in figure 6. The OIP3 of the LNA is achieved up to 41dbm at 3.6GHz frequency. This wideband LNA of GaAs pHEMT achieved highest bandwidth, better Noise Figure, small chip size and achieve better linearity. Therefore this is very much suitable in 5G Communication receiver's front end

IV. CONCLUSION

The proposed Ga As pHEMT process of wideband LNA is performed and evaluated at 50nm using current reuse topology. The design is achieved better performance for all the parameters to propose for 5G front end systems. An inductor based inter stage matching network improved the bandwidth. The RC cascade series network is connected at second stage is performed the better return losses and stability of the system by choosing transistor size and its biasing provided better Noise Figure. The Simulation result at post layout process forward gain of 16dB flat and Noise Figure achieved 1dB at a wideband width of 1.5GHz to 5.5GHz. The linearity achieved a +40dbm and OIP3 is achieved 20dbm at 1dB compression point. The chip size including pad is 0.64mm^2.

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