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Surface Potential Modelling Based Performance Analysis of Gate Engineered Trapezoidal Trigate Tunnel FET

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Abstract: *In this paper, a three dimensional (3-D) analytical model of surface potential has been derived for gate engineered trapezoidal trigate Tunnel Field Effect Transistor (TFET). The model has been obtained by assuming parabolic approximation of the potential profile and solving 3-D Poisson equation using appropriate boundary conditions. The device considered in this work is silicon based TFET with gate composed of two materials with different work functions. The low work-function material is placed close to source and drain region while high work-function material is placed in between them. This will result in enhancing the tunneling in the source/channel interface region while reducing the electric field in the drain region. Trigate devices have been found to enhance the device performance at nanoscale, however, Trigate device fabricated by Intel have been found to have trapezoidal shape rather than expected rectangular shape. In this work, we have included the effect of different inclination angles of sides on the device performance. The model has been verified by comparing the results with the simulation results obtained in ATLAS software.*

Keywords: *Tunnel FET; Dual material Gate; Trigate TFET, Trapezoidal FET, Silicon-On-Insulator (SOI) Transistor.*

I. INTRODUCTION

The semiconductor device scaling has enhanced the transistor performance to an unprecedented level and revolutionizing telecommunication devices, processing units and biomedical electronics. However, the transistor at nanoscale faces lot of problems ranging from fabrication difficulty to performance degradation due to dominance of non-ideal effects [1].

One of the main problem in nanoscale FET device is energy efficiency as these devices dissipate more power in active state and suffer from increased leakages due to miniaturization. TFET with subthreshold swing less than 60 mV/dec and CMOS process compatible had been considered as a promising device for various low power and low voltage applications [2]. Silicon based TFET suffers from low Ion due to poor tunneling probability of carriers from valence band of P+ doped source into the conduction band of intrinsic channel region [3]. To overcome problems of low ion and high ambipolar current in TFET, various devices have been proposed incorporating narrow bandgap materials and structural modifications [4]. Dual material trigate TFET has been reported in [5] where the gate consists of two materials with low work function material close to source and high work function material towards drain.

In this work, the dual material work function is employed in such a manner that low work function materials are close to source and drain ends of the channel and high work-function material is in between them. Further, due to trapezoidal shape of trigate transistor, the width of the device varies from Wtop to Wbottom and this will affect the trigate device performance [6]. In this work, we have included the comparison of trapezoidal trigate device of different inclination angles with rectangular trigate device. The Silicon on Insulator (SOI) structural technique has been included to reduce bulk leakage current and other device parasitic [7] [8] [9]. The structure of gate engineered trapezoidal trigate TFET with various device parameters is presented in Section II. The analytical surface potential model derivation is presented in Section III while results are presented in Section IV. The paper is concluded in Section V.

II. DEVICE STRUCTURE

As illustrated in Fig.1, gate engineered trapezoidal trigate TFET consist of silicon buffer/substrate, buried oxide layer of SiO_2 separating substrate and active channel region. The hetero material gate and gate oxide surround the channel from two lateral sides in addition to top side as shown in Fig.1. The gate is composed of two types of materials with work functions $\emptyset_{m1} = 4.0\ eV$, $\emptyset_{m2} = 4.4\ eV$ and $\emptyset_{m3} = 4.0\ eV$ respectively.

The gate material M_1 and M_3 have been considered to be having same work function in this paper unless otherwise stated. The device channel region is divided into three regions corresponding to material positions such that $L_1{:}L_2{:}L_3 = 1{:}1{:}1$. L_1, L_2 and L_3 represent the region lengths corresponding to hetero gate materials. In this structure, the source region is doped with Na = $1\text{x}10^{20}\,cm^{-3}$, drain region is doped with Nd = $1\text{x}10^{-19}cm^{-3}$ and the channel is lightly doped with Na= $1\text{x}10^{-15}cm^{-3}$ while source/channel and drain/channel junctions are considered abrupt.

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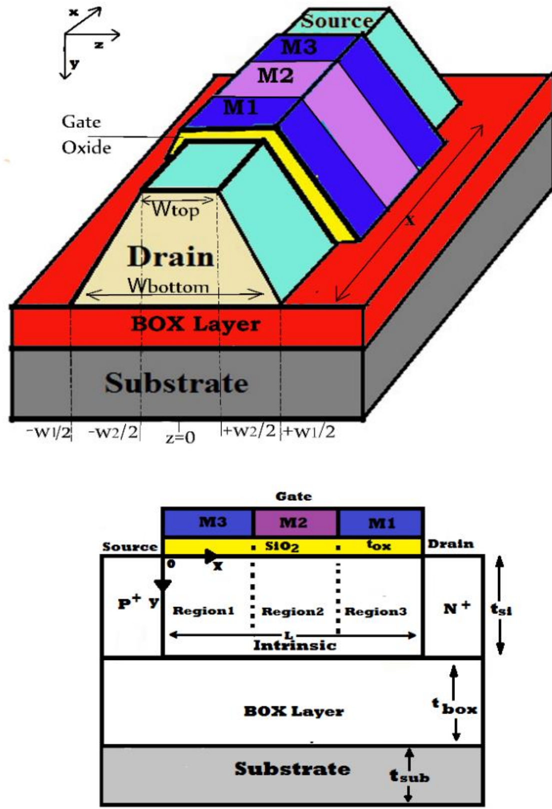

Fig. 1.3-D schematic and x-y sectional view of Gate engineered Trapezoidal trigate TFET.

The device parameters used in deriving the model and simulation results are channel length, L=30 nm, thickness of buried oxide layer, t_{box} = 40nm, thickness of front gate oxide(SiO_2), t_{ox} = 1 nm, thickness of channel, t_{Si} = 10 nm. Since the width of the device varies from top of the channel to the bottom as $-\frac{w_1}{2}$ to $+\frac{w_1}{2}$ and $-\frac{w_2}{2}$ to$+\frac{w_2}{2}$ on the z-axis, we have considered the inclination of side gates of 0^0, 5^0 and 10^0 in this work with W_{top} = 10 nm

III. ANALYTICAL MODEL DERIVATION

In the hetero-material gate, we assume each gate material will control the corresponding channel region electrostatics. M_1 will control channel electrostatics of region 1, M_2 will control region 2 and M_3 will be controlling region 3 of the channel. The channel regions can be defined as

Channel region 1

$$\left(0 \le x \le L_1, 0 \le y \le t_{si}, -\frac{w}{2} \le z \le \frac{w}{2}\right) \quad (1)$$

Channel region 2

$$\left(L_1 \le x \le L_2, 0 \le y \le t_{si}, -\frac{w}{2} \le z \le \frac{w}{2}\right) \quad (2)$$

Channel region 3

$$\left(L_2 \le x \le L, 0 \le y \le t_{si}, -\frac{w}{2} \le z \le \frac{w}{2}\right) \quad (3)$$

Where w is the equivalent device width and is calculated at orthocenter of device [10] as

$w = w_{top} + \frac{r}{r+1}\left(w_{bottom} - w_{top}\right)$, and r is the geometrical factor given by $r = \frac{2w_{bottom}+w_{top}}{2w_{top}+w_{bottom}}$.

The potential in the channel follows parabolic approximation [11] and can be expressed as 2nd order polynomial function written as

$$\psi_k(x,y,z) = \xi_{0k}(x,y)z^2 + \xi_{1k}(x,y)z + \xi_{2k}(x,y) \quad (4)$$

Where $k = 1,2,3$ and represent three channel regions. The coefficients of (4) can be found using following boundary conditions [12]

$$1.\ \psi_1(0,y,z) = V_{bi,p} \quad (5a)$$

$$2.\ \psi_3(L,y,z) = V_{bi,n} + V_{DS} \quad (5b)$$

$V_{bi,n}$ and $V_{bi,p}$ are the built-in potential at drain/channel and source/channel junctions respectively given by $V_{bi,n} = v_t \ln(N_{d,drain} \times N_{a,channel}/n_i^2)$, $V_{bi,p} = -v_t \ln(N_{a,source}/N_{a,channel})$.

Due to continuity in the flux at the gate oxide and Si channel boundary, we have

$$3.\ \frac{d\psi_k(x,y,z)}{dy}\bigg|_{y=0,z=0} = \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\left(\psi_{sk}(x) - V'_{GSk}\right) \quad (5c)$$

$$4.\ \frac{d\psi_j(x,y,z)}{dz}\bigg|_{y=t_{si,z=0}} = \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{box}}\left(V'_{sub} - \psi_{bk}(x)\right) \quad (5d)$$

Because of symmetry about the orthocenter (z=0) along the z-direction, we have

$$\psi_k\left(x,y,-\frac{w}{2}\right) = \psi_k\left(x,y,+\frac{w}{2}\right) \quad (5e)$$

ε_{ox}andε_{si} are the dielectric constant of oxide and silicon respectively. t_{ox}, t_{box} are the thicknesses of gate oxide and BOx layer respectively. $V'_{GSk} = V_{GS} - V_{FBk}$, where V_{FBk} represents channel flatband voltage of region 1, region 2 and region 3 under M_1, M_2 and M_3 respectively.$V'_{sub} = V_{sub} - V_{Fb,b}$, V_{sub} is the substrate bias and $V_{Fb,b}$ is the back channel interface flatband voltage. $\psi_{sk}(x)$and$\psi_{bk}(x)$ represent the surface potentials at front gate oxide-channel region interfaces and BOx layer-channel region interface.

Using above boundary conditions, the coefficients are obtained as

$$\xi_{0k}(x,y,z) = \left(\frac{4}{w^2}\right)\left(\psi_{sk}(x) - \xi_{2k}(x,y)\right) \quad (6)$$

$$\xi_{1k}(x,y,z) = 0 \quad (7)$$

The coefficient $\xi_{2k}(x,z)$can be derived by assuming the parabolic potential profile in vertical direction for low V_{ds} such that

$$\xi_{2k}(x,y) = \psi_{sk}(x) + \frac{\varepsilon_{ox}}{\varepsilon_{si}t_{ox}}\left(\psi_{sk}(x) - V'_{GSk}\right)y - \frac{\left[\left(\frac{t_{ox}}{t_{box}}+\frac{C_{box}}{C_{si}}+1\right)\psi_{sk}(x)-\left(1+\frac{C_{box}}{C_{si}}\right)V'_{GSk}\right]\frac{t_{box}}{t_{ox}}-V'_b}{t_{si}^2\left(1+2\frac{C_{si}}{C_{box}}\right)}y^2 \quad (8)$$

Where C_{box}, C_{si} represent the buried oxide capacitance and Si channel capacitance.

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The 3-D potential distribution function $\psi_k(x,y,z)$ for gate engineered trapezoidal trigate TFET can be calculated by solving three dimensional Poisson's equation [13]

$$\frac{\partial^2\psi_k(x,y,z)}{\partial x^2}+\frac{\partial^2\psi_k(x,y,z)}{\partial y^2}+\frac{\partial^2\psi_k(x,y,z)}{\partial z^2}=\frac{qN_c(x,y,z)}{\varepsilon_{si}} \quad (9)$$

q is electron charge, $N_c(x,y,z)=\left(N_{a,c}+n(x,y,z)\right)$ where $N_{a,c}$ is channel doping concentration, $n(x,y,z)$ is mobile electron charge density.

Considering full depletion approximation for the channel under zero bias condition such that $N_{a,c} \gg n(x,y,z)$ and $N_c(x,y,z) \approx qN_a$.

On solving (4) and (9) using the coefficients derived in (6), (7) and (8), we get

$$\frac{\partial^2\psi_{sk}(x)}{\partial x^2}-\alpha\psi_{sk}(x)=\beta_k-2\frac{C_{si}}{\delta t_{si}}[w^2+4(y^2+z^2)]V'_b \quad (10)$$

$$\alpha=\left\{8\frac{C_{ox}}{\delta}\left[t_{si}^2\left(1+\frac{C_{si}}{C_{box}}\right)\right]y+2\frac{C_{si}}{t_{si}}\left[\frac{t_{box}}{t_{ox}}+\frac{C_{ox}}{C_{si}}+1\right](w^2-4(y^2+z^2))\right\}$$

$$\beta_k=qN_{a,c}w^2\delta^{-1}\left(1+2\frac{C_{si}}{C_{box}}\right)t_{si}^2+4t_{si}^2\frac{\varepsilon_{ox}}{t_{ox}\delta}\left(1+2\frac{C_{si}}{C_{box}}\right)yt_{si}^2V'_{GSk}+\left(\frac{t_{box}}{t_{ox}}+\frac{C_{ox}}{C_{si}}\right)(w^2-(x^2+y^2))\frac{C_{si}}{t_{si}\delta}V'_{GSk}$$

$$\delta=\left(t_{si}^2\left(1+2\frac{C_{si}}{C_{box}}\right)\right)(w^2\varepsilon_{si}+C_{ox}(w^2-4z^2)y)+\left(\frac{t_{box}}{t_{ox}}+\frac{C_{ox}}{C_{si}}+1\right)(\varepsilon_{si}(4z^2-w^2)y^2)$$

The general form of surface potential distribution function $\psi_{sk}(x)|_{k=1,2,3}$ in gate engineered trapezoidal trigate TFET can be obtained by solving the second-order differential equation obtained in (10). Its solution is given as

$$\psi_{sk}(x)=R_k e^{\eta X_k}+S_k e^{-\eta X_k}-\sigma_k \quad (11)$$

where $\sigma_k=\beta_k/\alpha$, and X_k takes the value $X_1=x$, $X_2=x-L_1$ and $X_3=x-(L_1+L_2)$ in the channel region 1, 2 and 3 respectively. R_k and S_k are arbitrary constants to be determined by using the following boundary conditions;

1. $\psi_1(L_1,0,0)=\psi_2(L_1,0,0)$ (12a)
2. $\psi_{s1}(L_1)=\psi_{s2}(L_2)$ (12b)
3. $\left.\frac{\partial\psi_{s1}(x,y,z)}{\partial x}\right|_{x=L_1}=\left.\frac{\partial\psi_{s2}(x,y,z)}{\partial x}\right|_{x=L_1}$ (12c)
4. $\psi_2(L_1+L_2,0,0)=\psi_3(L_1+L_2,0,0)$ (12d)
5. $\psi_{s2}(L_1+L_2)=\psi_{s3}(L_1+L_2)$ (12e)
6. $\left.\frac{\partial\psi_{s2}(x,y,z)}{\partial x}\right|_{x=L_1+L_2}=\left.\frac{\partial\psi_{s3}(x,y,z)}{\partial x}\right|_{x=L_1+L_2}$ (12f)

Using the boundary conditions given in 12(a - f), the coefficients R_k and S_k are obtained as

$$R_1=\{(V_{bi,n}+V_{DS}+\sigma_3)-(V_{bi,p}-\sigma_1)e^{-\eta L}+(\sigma_1-\sigma_2)cosh(\eta(L_2+L_3))+(\sigma_2-\sigma_3)cosh(\eta L_3)\}\{sinh^2(\eta L_3)\}^{-1}$$

$$S_1=(V_{bi,n}-\sigma_1)-A_1$$

$$R_2=A_1e^{\eta L_1}-(\sigma_1-\sigma_2)/2$$

$$S_2=B_1e^{-\eta L_1}-(\sigma_1-\sigma_2)/2$$

$$R_3=A_2e^{\eta L_2}-(\sigma_2-\sigma_3)/2$$

$$S_3=B_2e^{-\eta L_2}-(\sigma_2-\sigma_3)/2$$

IV. RESULTS AND DISCUSSION

To verify the proposed analytical model, all the device simulations have been performed using TCAD device simulator ATLAS [14]. Device models like standard band-to-band tunneling, Lombardi (CVT) Model, Shockley-Read-Hall (SRH), band-gap narrowing and concentration and field dependent mobility were used in the simulation work.

Fig. 2 shows the variation of channel potential as a function of position along the channel length from source to drain for various values of Vgs. It can be observed that the increase in Vgs shifts the potential upwards and creates more band bending. This will result in increase in tunneling current at the source junction while also increasing the ambipolar current occurring at the drain junction. In order to decrease the unwanted ambipolar current and increase the tunneling current, gate work function engineering techniques have been incorporated in this work.

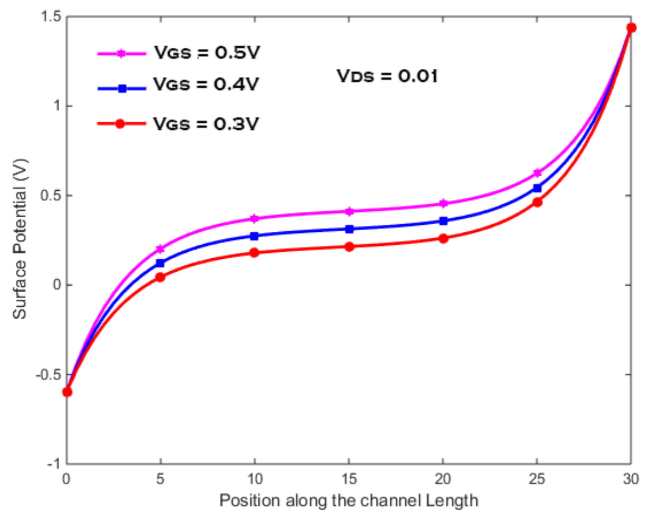

Fig. 2. Analytical and simulated surface potential variation is plotted versus position along the channel length for different gate voltage.

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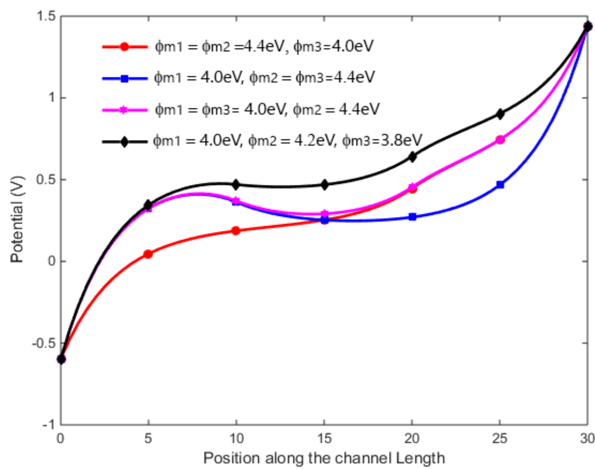

Fig. 3.Analytical and simulated surface potential variation is plotted versus position along the channel length for different gate work-functions.

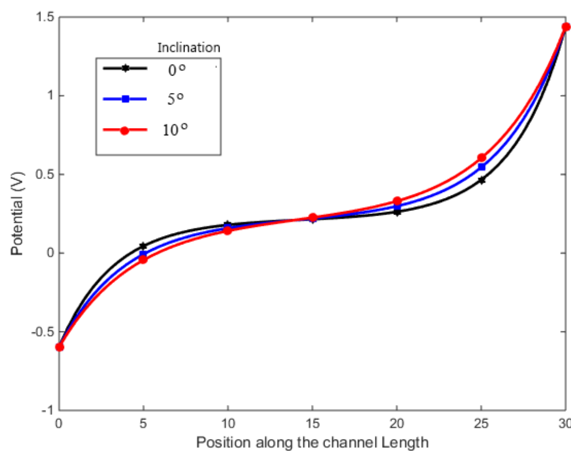

Fig. 4.Analytical and simulated surface potential variation is plotted versus position along the channel length for different device inclinations.

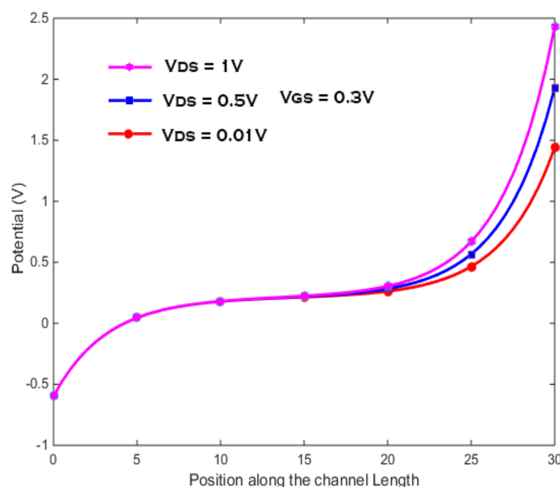

Fig. 5.Analytical and simulated surface potential variation is plotted versus position along the channel length for different Drain-Source Bias.

The gate has been composed of different work function materials and the impact of these materials has been shown in Fig. 3. In the first case, gate material M_1 and M_2 have been considered of same work function material while M_3 is considered of comparatively low work function material. In the second case, M_1 is low work function material, while M_2 and M_3 are of same material with comparatively higher wok function. In the third case, M_1 and M_3 are considered low work function materials while M_2 is high work function material. In the fourth case, M_1, M_2 and M_3 have been considered as different work function materials. The higher work function towards the source end reduces the band bending and it will result in lower drive current of the device. The higher work function towards the drain end will increase ambipolar current due to increased band bending. The case third and fourth represent optimum criteria to enhance drive current and reduce ambipolar current. Fig. 4 shows the effect of trapezoidal shape on the channel potential. It can be observed from the given figure that the increase in the inclination angles of the side gate will lower the band banding and hence degrade the device performance. The case of inclination = 0^0 represents the rectangular device and shows maximum band bending. The effect of increase of Vds on the device has been shown in Fig. 5., it can be seen that the increase in Vds has negligible effect on the source/channel tunneling junction.

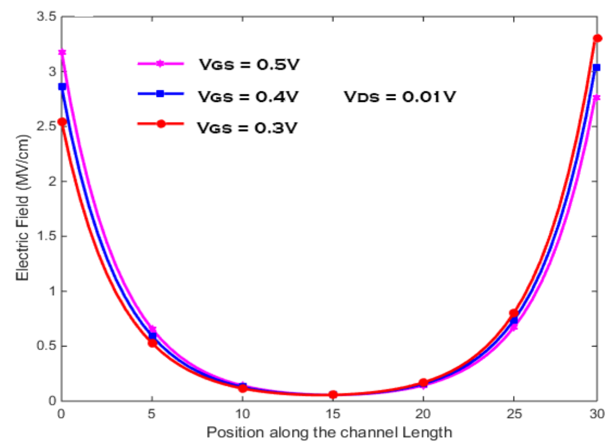

Fig. 6.Analytical and simulated surface potential variation is plotted versus position along the channel length for different values of Vgs.

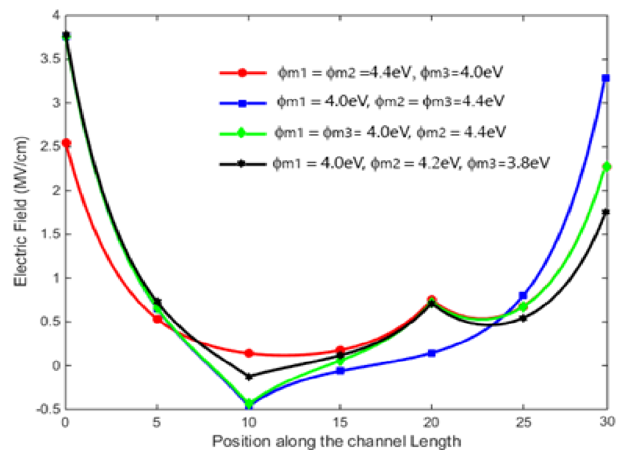

Fig. 7.Analytical and simulated surface potential variation is plotted versus position along the channel length for different gate work-functions.

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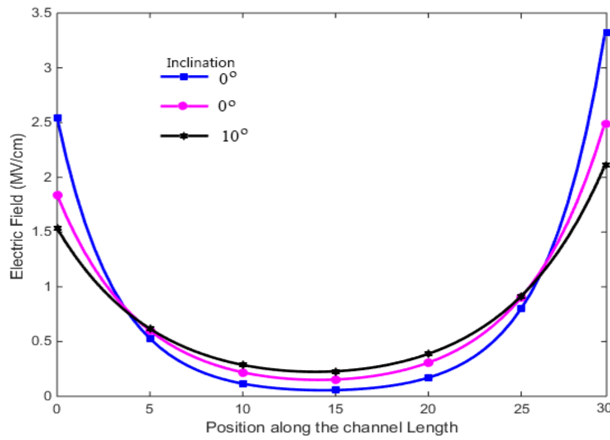

Fig. 8.Analytical and simulated surface potential variation is plotted versus position along the channel length for different device inclinations.

The electric field variations in the channel region has been shown in Fig. 6, Fig. 7 and Fig. 8. In the Fig. 6., the electric variation for increasing values of Vgs has been shown while the electric field variation for different gate material work functions has been shown in Fig.7. It can be observed that with M_1 composed of low work function materials while M_2 andM3 composed of high work function material shows higher electric field at the source/channel tunneling junction while reduced electric field at the drain/channel junction. The electric field can further be reduced by placing lower work-function gate material near the drain end to further reduce the ambipolar current and other parasitic effects. In Fig.8, the effect of inclination angle on the channel potential has been shown. The increase in inclination angles result in decrease in electric field near source/drain and channel junctions. The will reduce the current drive of the device. The use of gate work-function engineering can help to compensate for the low drive as already discussed.

V. CONCLUSION

In this work, a 3-D surface potential model of gate engineered trapezoidal trigate tunnel FET has been developed by solving three-dimensional Poisson's equation. The model takes into account the non-ideal effects of device geometry. The gate work-function engineering for the structure have been analyzed to overcome performance-degrading effects due to these non-ideal effects. The analytical model results have been compared with the simulation results obtained from ATLAS software. The close agreement between the simulation and analytical model results verifies the derived model.

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