International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-11 Issue-5, April 2022

Design of Various Low Power and Highspeed Full Adder Designs using 45nm Cmos Technology

Soniya Nuthalapati, Ch. Jyothirmayi, Galla. Saikiran, Chaitanya Prathikonda, Arigala Joseph Jagarlamudi Manikanta

Abstract: ***This project visualizes the different designs of Full Adder (FADDR) circuits. These FADDR circuits are designed mainly to reduce the power and delay factors. If these two factors are minimized then automatically the power delay product (PDP) gets minimized. In addition, to design the FADDR, we used multiplexer. So, that the FADDR transistor count gets reduced. Here in this FADDR implementation, it is designed with different transistors count and the factors like power consumption propagation delay and power delay product (PDP) constraints are tabulated with different transistor count of FADDR designs. Then the power consumption and propagation delay factors get reduced. The designs are simulated by using 45nm CMOS technology in Cadence Virtuoso tool.***

Index Terms: Power Consumption, Propagation Delay, 45nm Cmos Technology and Cadence Virtuoso Tool.

I. INRODUCTION

To boost the performance, a quasi-N-P domino logy structure was implemented & unique pipeline architecture were employed in the accumulator to scale back the overall latency & a special output buffer layout was introduced to accomplish 2 hundred MHz off- chip full CMOS logic levels. And a conventional 1.0 µm CMOS technology was designed and applied by 8- b adder made up of FADDRs with carry increment & effectively examine as much as 800 MHz logic flip flop technology is used in 8-b adder to reduce power consumption.

Manuscript received on 29 March 2022.
Revised Manuscript received on 04 April 2022.
Manuscript published on 30 April 2022.

* Correspondence Author

Soniya Nuthalapati*, Department of Electronics & Communication Engineering, Jawaharlal Nehru Technological University, Kakinada. Guntur (Andhra Pradesh), India. Email: nuthalapatisoniya@gmail.com

Ch. Jyothirmayi, Department of Electronics & Communication Engineering, Jawaharlal Nehru Technological University, Kakinada. Guntur (Andhra Pradesh), India. Email: jyothirmai.93@gmail.com

Galla. Saikiran, Department of Electronics & Communication Engineering, Jawaharlal Nehru Technological University, Kakinada. Guntur (Andhra Pradesh), India. Email: gallasaikiran65@gmail.com

Chaitanya Prathikonda, Department of Electronics & Communication Engineering, Jawaharlal Nehru Technological University, Kakinada. Guntur (Andhra Pradesh), India. Email: prathikondchaitanya900@gmail.com

Arigala Joseph Jagarlamudi Manikanta, Department of Electronics & Communication Engineering, Jawaharlal Nehru Technological University, Kakinada. Guntur (Andhra Pradesh), India. Email: josepharigala@gmail.com

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This research examines the overall result of single-bit FADDRs in CMOS technology & gives an improved execution analysis correlates the design with power, delay & charging functionality. Instead of CMOS counterparts, single flux Quantum circuits perform at better frequencies & consume much less power. Complicated multi-input SFQ logic gates can be developed & utilized to regulate the increase in total number of gates. The fully functional Boolean logic & arithmetic functions with 1T1R mode using a CMOS technology having improvements in non-volatility, computational velocity & design space. As well introduces the design of a new magnetic FADDR based on PMA (Perpendicular magnetic Anisotropy) STT-RAM. It offers advantageous energy efficiency & die area compared to traditionally CMOS only FADDRs. Basic topologies of one-bit FADDRs are evaluated and compared for speed, power consumption, and power-delay product in this work, including the most intriguing of those recently developed. Traditional CMOS and Mirror topologies are the most intriguing implementations in terms of power-delay tradeoffs and the more appropriate Figure of merit utilized. A commercial 90-nm CMOS technology, a 3-bit current-mode flash quantizer with current summing step & it is designed for continuous-time sigma–delta modulators with minimal power consumption. The new current-mode approach is faster and uses less power than the traditional voltage-mode flash approach. Also, a hybrid 1-bit complete adder architecture is presented in this study, which uses both CMOS logic and transmission gate logic. Compared to existing ones FADDR design found to be provided by current implementations significant improvements in power and speed. Mainly a two-tier 64 bit carry look lead adder using BICMOS gate of pass transistors was implemented, successfully a less delay time was recorded. This adder is quicker than the CMOS adder describes the variant CMOS technologies [1]-[10]. In the proposed NVFA (Non – Volatile FADDR), the MJT sharing approach using a demultiplexing technique to significantly minimize space & power as well as increase the speed & Sensing margin. Other types of NVM can potentially benefit from NVFA. A Technique named 8-bit NV-FA architecture in which all input signals are stored in MJT'S rather than CMOS registers to evaluate their capabilities and as compared their performance in phrases of energy consumption & Space etc. Mainly, the suggested hybrid FA circuit appears to be an appealing option for data path design in modern high – velocity CPU's & the design performance related to energy consumption & delay that causes low power delay product.

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New technique like Vertically Anisotropy Magnetic Tunnel Junction (MTJ) is one of the most promising candidates for building hybrid logic-in-memory architectures. Compared to the previous STT MTJ-based MFA, the proposed MFA reduces uptime for read and write operations and power consumption. As well In both memory and logic implementations, Domain Wall Nano Magnet (DWNM)-based devices have been widely researched as a possible alternative to standard CMOS technology. Over CMOS-based and MTJ based FA designs, the comparison results show area improvement, as well as improvement in device count complexity. A totally nonvolatile magnetic full-adder (MFA) circuit employs the spin-transfer torque (STT) approach, which is aided by the spin-Hall effect with no data loss that can be used for power gating to MTJ switching's delay and power consumption are greatly reduced. Multigate SETs are utilized as pass transistors in this architecture, which is based on pass-transistor logic. This demonstrates that in our approach, area reduction and speed improvement are compatible. And also discussed about topic of random-offset-charges and the prospect of large-scale integration. A FA reliability is extrapolated to get a reliability estimate from the device level. Such reliability analysis, in addition to known speed and power consumption will be used to better characterize FA designs in future Nano electronic technologies are needed. An effective analysis and modelling technique for evaluating the timing behavior of hybrid FADDR circuits at the block level and forecasting their performance in multistage circuits. The gain and selection factor are introduced as a criterion for precise selection and optimization of hybrid adder cells. The hybrid structure is faster and uses less power illustrates the new techniques for optimizing power and delay [11]-[19]. The QCA decimal FADDR consists primarily of multiple gates of full load and rarely contains PUM. QCA designer was used to design & examine the suggested circuits which showed an improvement in cell count, space & delay. A new XOR/XNOR and simultaneous XOR–XNOR circuit's features are introduced. In terms of power consumption and delay, the proposed circuits are extremely efficient. Each of the circuits proposed has its own set of advantages in terms of speed, energy consumption, power delay product (PDP), driving ability, and so on. A reverse carry propagate adder (RCPA) is used in this research to achieve improved stability in the presence of delay changes. The findings show that there were improvements in delay, energy, and energy-delay-product, while delivering improved levels of accuracy relates to the computational reduction [20]-[22]. The CNFET-SEA algorithm employs sensitivity analysis as a novel approach to produce better sizing results in less time. When compared to the referred FADDRs, the simulation results reveal a delay, power-delay product (PDP), and energy-delay product (EDP) improvement for the suggested FADDRs depicts the new algorithm [23]. In this study, we examine several of the most practicable FADDR topologies in terms of their delay reliance on supply voltage variations, which are a major contributor to delay uncertainty and, as a result, limit the speed performance of current VLSI circuits. As a result, it is demonstrated that in future technological nodes, the delay sensitivity to supply variations would rise the variant topologies [24]. Clutter data acquired with mid frequency sonar are subjected to a recently developed technique for predicting echo statistics. The information was separated into three groups: bottom structures, diffuse clutter, and compact nonstationary clutter distinguish about noises removal [25]. In terms of speed, power consumption, and space, we compared it to comparable full-adders that were stated to have a low PDP. Post-layout simulations show that the proposed FADDR is superior to the corresponding one, with an average PDP benefit and Relative area explains comparison among CMOS over BICMOS [26]. A Compact Adder & Reprogrammable logic method allows for reprogram ability while in use & considerably decreases the complexity of the digital logic design & successfully achieved the power consumption, Component optimization, Size reduction required for IoT applications related the CMOS technology with the IOT [27].

II. CMOS MODELLING

In this CMOS modelling design the circuit is designed using PMOS and NMOS transistors. Do that mainly the project concentrates as the power and delay factors resulted by the Projected CMOS circuit. The mean power dissipated in designed circuit is calculated by using the mathematical formulas as:

$W_{av}=W_{deg}+W_{sc}+W_{st}$

$=V_{DD}.f_{cl}\sum_k(V_{kswing}C_{kload}\alpha_k)+V_{DD}\sum_k I_{ksc}V_{DD}I_l$ (1)

The terms notate that

f_{clk}=clock frequency

V_{Kswing}=voltage swing at node R(approx. =V_{DD})

C_{Kload}=load capacitance at node K

α =activity constraint at node K

I_{ksc}=short circuit currents

I_l=leakage currents

While simulating the CMOS circuits,

In the limited region, the given voltage should be a minimized value when compared to the given restricted applied voltage given to the circuit. Because of this situation, the transistor channel will be never inverted when it is ON condition. With regard to limited region, there is a curve visualized with a exponential relation between voltage and current terms. This equation will be calculated with two models, those are weak and moderate modes. If the designed CMOS circuit is in weak mode then the equation can be modelled as

$I_{lim}=I_s.e^{\frac{V_G-V_{T0}-n.V_S}{n.U_T}}$ if $V_{DS}>4.V_T$ (2)

I_s= specific current

And the specific current can be notated as:

$Is=2.n.\eta_m(q).C_{ox}.\frac{W}{L}.U_T^2$ (3)

All voltages represented here are related in local substrate.

Where U_T=thermal voltage=$\frac{KT}{Lq}$

n= slope constraint

V_{T0}=zero related restricted voltage

$\eta_m(q)$=carrier mobility for n or p channel circuits

C_{ox}= oxide capacitance

W= width of channel

L=Length of channel

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III. EXISTENT FULL ADDER (FADDR) DESIGN

The existed FADDR(FA) design resembles the circuit that contains 28 number of transistors. The fundamental design for calculation is the one bit FA. This FA contains three inputs represented as A,B and Cin and two outputs represented as Sum(S) and carry out (Cout). The interaction between inputs and outputs can be drawn as

Sum(S)=A XOR B XOR Cin (4)

Carry(C_{out}) = A AND B + Cin AND (A XOR B) (5)

The equations (4) and (5) can be reassembled as

Sum(S)= C_{inbar} (A+B+Cin)+A.B.Cin (6)

Sum(S)= C_{inbar}(A OR B OR Cin) OR (A AND B AND Cin)

Carry (Cout)=(A.B)+(Cin.(A+B)) (7)

Carry(Cout) = (A AND B) OR (Cin AND (A OR B))

The FA circuit diagram with 28 transistor is shown in Figure 1. And there are various logical methods to design the schematics as per the requirement. But, while designing the schematic, the constraints like power consumption propagation delay and leakage currents are to be considered mainly. The second consideration is based on the application oriented the logical method should be selected. Every logical methods have various applications and its functionality will be differed. Coming to the work wide the schematic should work with reliability, stability over irrelevant given input effects. Looking at all these all parameters, it is difficult to design the logical method resulted with logic factor. Any logical method designed is not a competitive to the CMOS logical method because of its stability and flexibility. CMOS projected design will be with multibranded. And totally it consists of 28 transistors FADDR(FA) design.

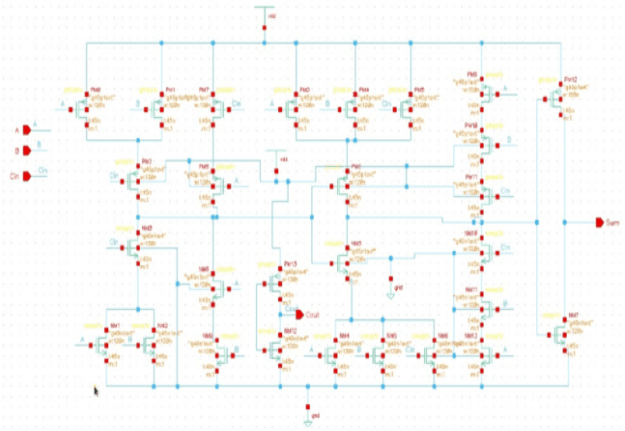

Figure1: Schematic Representation of Existed 28 Transistor Full Adder Design.

IV. PROJECTED FULL ADDER DESIGNS

A. 14 Transistor Full Adder Design:

Here in this FADDR design, we used the exclusive-OR and exclusive-NOR to result the sum(s) and carry out (Coot) signals. This design consists of 14 transistors. Along with the Exclusive-Or and Exclusive-NOR design there is a CMOS inverter to make the Exclusive OR as Exclusive NOR. And the schematic is conventionally analogized because of absolute FA circuit design. The enhanced 14 transistor FA is visualized in Figure 2.

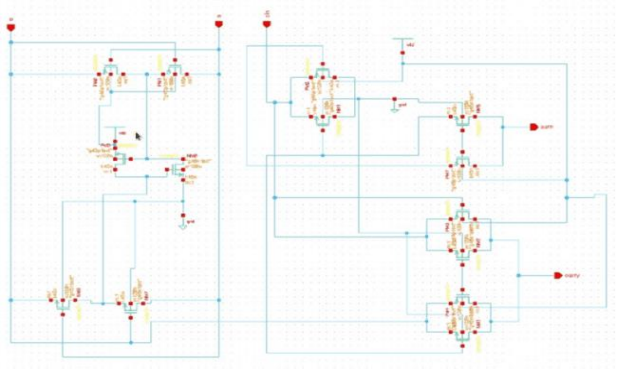

Figure2: Schematic Representation of 14 Transistor Full Adder Design.

B. 12 Transistor Full Adder Design

The schematic design of 12 transistor FADDR is overall designed by 2 by 1 multiplexer. This method is considered because of the factor power consumption. This is attained go result because of power minimization happens because of 2x1 mux. So, the 2x1 mux based FADDR is shown in Figure 3.

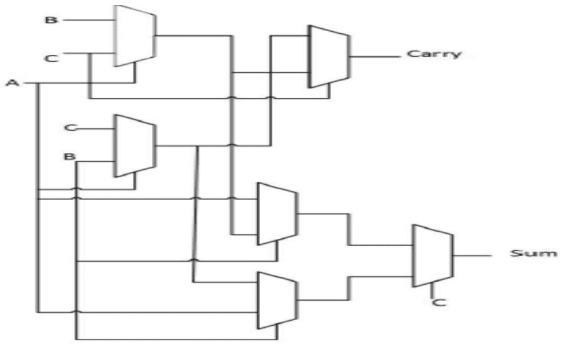

Figure3: Schematic Representation of 12 Transistor Full Adder Designed by using 2x1 Mux.

C. 8 Transistor Full Adder Design:

The 8 transistor FA is designed with the help of three choosers. In those two choosers each chooser consists of one Vdd and two PMOS and third chooser contains one CMOS invertor. This logical method is mainly used to result the minimum propagation delay that is it will generate the outputs with fastness those are Sum(s) and Carry (Cout). And the 8 transistor FADDR is visualized in Figure 4.

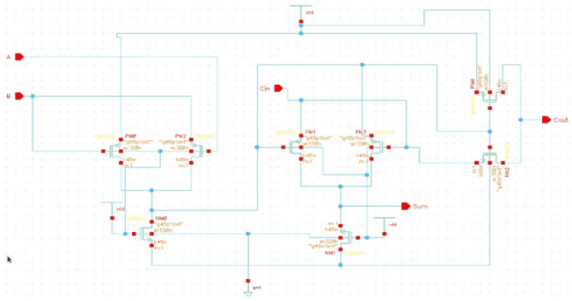

Figure4: Schematic Representation of 8 Transistor Full Adder Design.

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D. Low Power 10 Transistor Full Adder Design:

This schematic design comprises of 4 transistor Exclusive OR and. two 2 by 1 multiplexer and one CMOS inverter. Actually this 2x1 minimizes the propagation delay, multiple so that the Power minimization happens automatically. So the 10 Transistor Low Power FADDR design is visualized in Figure 5.

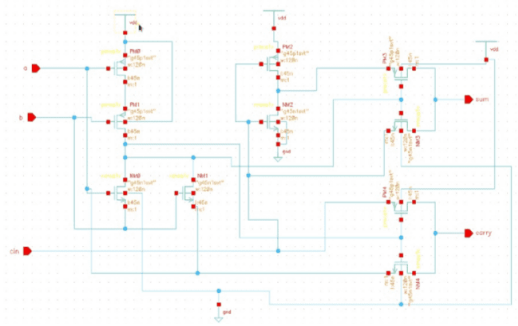

Figure5: Schematic Representation of Projected Low Power 10 Transistor Full Adder Design.

V. SIMULATION RESULTS

The tabulated out comes visualizes the affinity between Power consumption, propagation delay and power delay Product (PDP), Average Power, Maximum for 28T, 14T, 12T, 8T and Projected 10T Schematic FADDR design with Low Power. The outcomes are shown in the Tabular column 1. The 28T existed full adder simulated outcome is visualized in Figure6. And the Projected Full Adder (FADDR) with different transistor count like 14T, 12T, 8T and 10T simulated wave forms are shown in Figure7-10respectively.

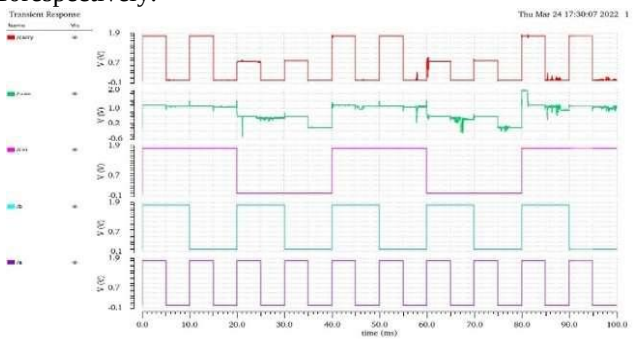

Figure6: Simulated Transient Outcome of Existed 28 Transistor Full Adder Design.

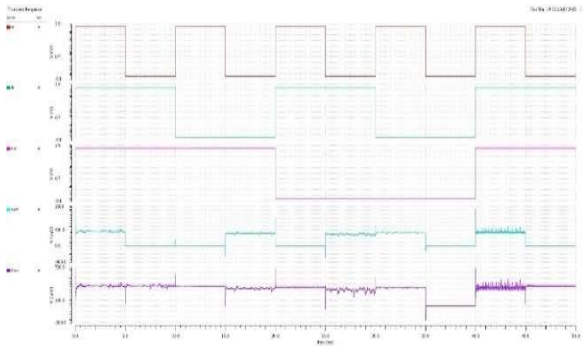

Figure7: Simulated Transient Outcome of 14 Transistor Full Adder Design.

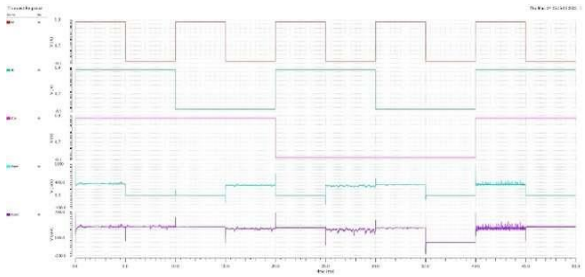

Figure8: Simulated Transient Outcome of 12 Transistor Full Adder Design.

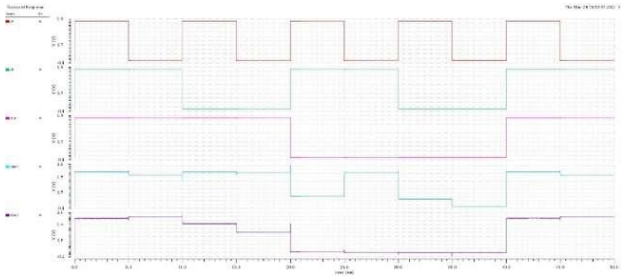

Figure9: Simulated Transient Outcome of 8 Transistor Full Adder Design.

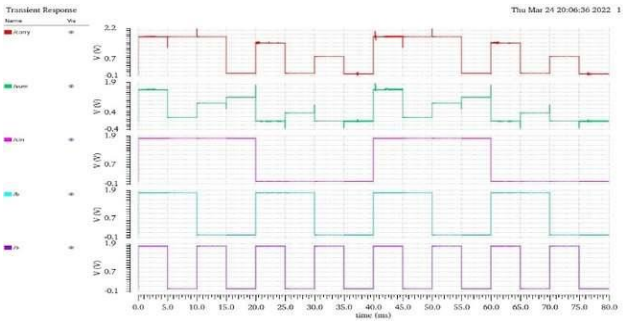

Figure10: Simulated Transient Outcome of Projected Low Power 10 Transistor Full Adder Design.

From the Figure10, the outcomes of Low power LOW FADDR attain effective design shows the good results analogize terms of Power consumption, Propagation delay and PDP. Table1 Visualizes the Analogy of Existed 28T and Projected 14T, 12T, 8T and Low Power 10T Full Adder designs.

TABLE 1: Analogy of CMOS 28T, 14T, 12T,8T and Low Power 10T Full Adder Designs.

PERFORMANCE PARAMETER	Existed 28T Full Adder	Proposed 14T Full Adder	Proposed 12T Full Adder using 2x1 Mux	Proposed 8T Full Adder	Proposed Low Power 10T Full Adder
TECHNOLOGY USED	45nm	45nm	45nm	45nm	45nm
SUPPLY VOLTAGE	1.8V	1.8V	1.8V	1.8V	1.8V
POWER DISSIPATION (nW)	6.9254	5.7924	4.4562	2.7653	2.4326
PROPAGATION DELAY (ns)	0.115	0.091	0.064	0.043	0.024
POWER DELAY PRODUCT (PDP) (femto joules 10^{-15})	0.796	0.527	0.285	0.118	0.058

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VI. CONCLUSION

The Projected Low Power FADDR design in 45nm CMOS technology with Cadence Virtuoso tool attains accurate and perfect results when related it to the existed 28T FADDR design. And this minimizes the certain percentage of power when compared to existed FADDR design. This design optimizes the power from 6.9254nw to 2.4326nw represents the reduction of 35.12%, while the propagation delay minimizes from 0.115ns to 0.024ns represents the minimization of 20.86%.

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AUTHORS PROFILE

N.Soniya, Assistant Professor received her B.Tech degree from KKR & KSR Institute of Technology and Sciences, Vinjanampadu, Guntur (D.t), Andhra Pradesh and M.tech from KKR&KSR Institute of Technology and Sciences, Vinjanampadu, Guntur(Dt), Andhra Pradesh. And have 3 years of teaching experience as an Assistant professor in various engineering colleges, currently working as an Assistant professor in Department of ECE in KKR&KSR Institute of Technology and Sciences, Vinjanampadu, Guntur (Dt), Andhra Pradesh, India. Totally 13 publications are there in various journals. Areas of interests are VLSI, Signal Processing, and wireless communication.

Ch.Jyothirmayi , Assistant Professor received her B.Tech degree from KKR & KSR Institute of Technology and Sciences, Guntur (D.t), Andhra Pradesh. And M.Tech degree from St.Mary's womens Engineering College. Guntur (D.t), Andhra Pradesh. And have 4 years of teaching experience as an Assistant professor in various engineering colleges, Currently working as an Assistant professor in Department of ECE in Hindu College of Engineering and Technology Amaravathi Road, Guntur (Dt), Andhra Pradesh, India. Totally 03 publications are there in various journals. Areas of interests are VLSI, Signal Processing, and wireless communication.
and wireless communication.

Galla. Saikiran, UG Scholar from KKR & KSR Institute of Technology and Sciences, Vinjanampadu, Guntur (D.t), Andhra Pradesh

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Chaitanya Prathikonda, UG Scholar from KKR & KSR Institute of Technology and Sciences, Vinjanampadu, Guntur (D.t), Andhra Pradesh

Arigala Joseph Jagarlamudi Manikanta, UG Scholar from KKR & KSR Institute of Technology and Sciences, Vinjanampadu, Guntur (D.t), Andhra Pradesh

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