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Design of Diversified Low Power and High-Speed Comparators using 45nm Cmos Technology

C.Arunabala, P.V. Sai Ranjitha, Bomminayuni Likhitha Gunturu Sravya, Bonagiri Navyasree, Arumalla Mounika

Abstract: ***At Present, portable battery-operated devices are enhancing due to low power consumption and high-speed applications, The designed circuit with feedback are used to design novel circuits. If the comparator having feedback are without clock signal. The comparators are mainly designed to minimize the power consumption and with good accuracy because of clock signal, if the clock signal is there, it is used to drive the circuit with low current. But in the existed design the circuit is with high power and current. These drawbacks are overcome by using the projected designed comparator. The Projected comparator design is with reduced power consumption, propagation delay, currents and with a smaller number of transistors. The comparators are useful in analog to digital converters. And this is simulated by using 45 nm CMOS technology Cadence Virtuoso tool.***

Keywords: Existed Dynamic Comparator, Projected comparator, 45nm CMOS technology and Cadence Virtuoso tool.

I. INTRODUCTION

In this paper, a Comparator was designed using CMOS to achieve fast computations and good performance, finally found it is capable of handling the desired results with power loss of 1.8mW. New design like successive-approximation-register was developed with 32nm CMOS and two comparators with different clocks were used to gain the perfection and found that it provides low power loss with small size. A dynamic-comparator with 1volt power supply was designed using 65nm CMOS method and found that it can successfully reduce the power and noise to a possible extent.

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* Correspondence Author

Dr. C. Arunabala*, Department of Electronics & Communication Engineering, Jawaharlal Nehru Technological University, Kakinada. Guntur (Andhra Pradesh), India. Email: arunabala4700@gmail.com

P.V.Sai Ranjitha, Department of Electronics & Communication Engineering, Jawaharlal Nehru Technological University, Kakinada. Guntur (Andhra Pradesh), India. Email: sairanjitha.pasupuleti@gmail.com

Bomminayuni Likhitha Gunturu Sravya, Department of Electronics & Communication Engineering, Jawaharlal Nehru Technological University, Kakinada. Guntur (Andhra Pradesh), India. Email: bomminayunilikhitha@gmail.com

Bonagiri Navyasree, Department of Electronics & Communication Engineering, Jawaharlal Nehru Technological University, Kakinada. Guntur (Andhra Pradesh), India. Email: navyasreebonagiri@gmail.com

Arumalla Mounika, Department of Electronics & Communication Engineering, Jawaharlal Nehru Technological University, Kakinada. Guntur (Andhra Pradesh), India. Email: mounikaarumalla602@gmail.com

Accordingly, a low voltage comparator was implemented using 0.5µm CMOS and the calculated results provided low response time and power dissipation. CMOS comparator was designed using less number of transistors that can handle many inputs and found that it gives fast response with negligible delay. And a binary comparator with single-clock pulse is developed using ST 90-nanometer CMOS method and successfully increased the speed with less transistors and low power dissipation. Concisely with 0.18µm CMOS method a rectifier that can transfer power wirelessly with comparator as its major part was implemented and finally achieved with 81.9% of power-conversion at high-frequencies. Mainly, to reduce the supply voltage a conventional-CMOS design with low-potential comparator was developed using 0.11µm CMOS technology and practically reduced the needed constraints with quality outputs. Done with 0.13µm CMOS process a low power comparator was fabricated and finally improved the speed and reduced the consumed power to the needed values. By using 65nm CMOS technology a comparator that gives amplified output was manufactured and the design provides low power-consumption, noise with best throughput. A perfect-activated peak configured comparator was designed using 40 nm CMOS method and concluded that it provides best outcomes with low power usage. And a well-matched comparator was demonstrated using CMOS technology and analysed with several methods, found that it gives perfect outcome at maximum samples [1]-[12]. A new method like the count depended equalizer was proposed that requires less comparators and low power loss. The data needed was gained successfully with this method.

A priority based encoding technique was presented and look-ahead method was also implemented to reduce the delay. Results shown were having good response with low loss. A method like, aperture-time-equalization method based on impulse of comparator with clock is developed and concluded that it provides best throughput. A comparator with high speed and accuracy was implemented using CMOS preamplifier with many stages and found that the implemented technique will provide the input of 33µV with the accuracy of 200µV. Along with that an automated method a comparator was developed and found that it exhibits fast throughput and error free data when single-event-transients were used. As well a comparator with double-tail technology was developed and studied, finally came up with successful outcome in minimizing power utility, area and improving speed.

A novel method like edge-race technique was used to design comparator which provides low-power and low noise to the greatest possible extent [13]-[19]. A comparator was developed in HSPICE software using 0.18µm technique and the results lead to decrease in feedback noise with accurate throughput. And also the HSPICE software was used to implement CMOS-comparator and found that parallel-prefix-arrangement decreases the power-dissipation and delay even at high frequencies [20]-[21]. In static RAM was used to design a comparator that can provide speed operation with less delay and came up with feasibility in achieving all the needed values. A modified delay-locked-loop was implemented using FET CMOS method for comparator design, which can calculate the data of its own with perfect figure-of-merit. The voltage-doublers with high speed comparators were designed with less size. Finally, resulted in low power consumption and propagation delay. Concisely double and triple-well process were used to fabricate the comparator in 90nm CMOS development and the results shows its exposure to power consumption and delay in a perfect manner. Mainly, for low power appliances, a circuit was demonstrated as comparator by taking inverted voltage as important term for input and concluded that it suits for desired throughput. A switched capacitor that uses comparator was studied and detected that it can replace the operational-amplifier in analog to digital converters with best outputs [22]-[27].

II. COMPUTATIONAL REALIZATION

The parameter, slew rate means modification caused at resultant, that can be overcome by the resultant of comparator. The propagation delay reacts oppositely accordance the given input. This states that if input voltage is more than the propagation delay try to enhance itself, then slew rate can be minimized. The constraints that show the effects on comparator are propagation delay and the time taken for the comparator to sieve. The propagation time is computed by taking the slew rate of comparator, then its time can be notated as:

t_d or $\Delta T = \Delta V / SR = V_{Houtput}\text{-}V_{Loutput}/2SR$

t_d(or) ΔT = Propagation delay

ΔV = change of the voltage at the resultant of the comparator

SR= slew rate

$V_{Houtput}$= upper limit of the comparator

$V_{Loutput}$= lower limit of the comparator

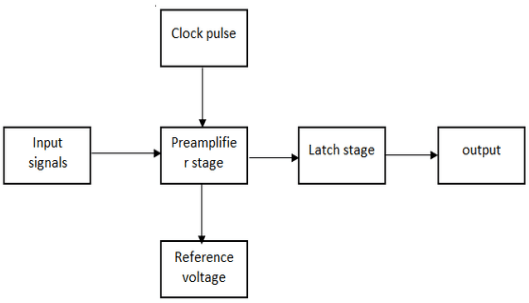

Figure1: Preamplifier Latch Comparator

For the comparator, at basic square wave to be applied with time T and frequency f then comparator current falls to VDD, because the input given is VDD. Power dissipation relates to clock frequency. In addition, if we add the dynamic logic to the comparator then there is reduction occurs at power dissipation. In case if switched capacitor is used then delay reduces. Sampling frequency can be inversely proportion to time period T. And f α 1/T and equal or greater than frequency bandwidth. For power dissipation that is noted as P=fcVDD2 where f is output frequency and c is output capacitance and VDD is power supply voltage and the comparator block diagram is shown at Figure 1. So, these all are applied to the existing methos to enhance the circuit design in terms of power dissipation and delay.

III. EXSISTENT STANDARD COMPARATORS

A. Comparator with Standard Dynamic Logic

The comparator with dynamic logic is visualized in Figure2 and mainly used for analog to digital convertors application. If clock is zero, then reset occurs and the transistor NM1 will be OFF condition and the transistors PM0 and PM3 called reset transistors gets ON and the resultants outp and outn occurs with VDD and goes to switch form. When clock is VDD then PM0 and PM3 are OFF and NM1 goes to ON, so that resultants outn and outp reduces slightly from VDD to various levels because of capacitors used. If Vinp is more than Vinn then voltage at outp will reduces with high speed when compared to voltage at outn. And the potential at outp is reduced because of NM2 transistor current potential becomes VDD-|Vthp|, ahead of voltage outn reduced because of NM0 transistor current, then in sequence PM2 transistor gets on. Then CMOS inverters connects oppositely to each other then it gives the latch and shows the potential at outn result shows VDD and potential at outp reduces to ground. For suppose Vinn potential is given more than Vinp, then design performs accordingly. The capacitors C0 and C1 gets reduced till the PM2 and PM1 transistor gets ON visualizes the propagation delay. If voltage potential at INP is more than INN that is Vinp>Vinn then NM2 current reduces with utmost speed at result outp. While analogized to outn result because of NM0 having less current resultants visualizes the propagation delay in overall. The design performs with high input impedance and very hard over clutters in the original signal. The power supply should be high to run the group of transistors with less propagation delay. At source NM3 and NM4 shows the positive feedback because of to reduce the potential for one resultant, while PM0 and PM3 used for consummate renewal. The propagation delay increases because of low transconductance.

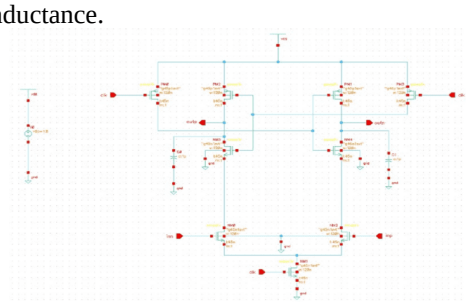

Figure2: Schematic representation of ordinary dynamic comparator.

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The drawback of this circuit is the current passes through the NM1 connected to differential amplifier in addition with back to back CMOS inverters.

B. Standard Double End Comparator

The schematic design of existed double end comparator is visualized in Figure3. The comparator contains less numbers of transistors and works with low power supplies. It activates the high amount of current to passes through NM1 at primary block. The working of comparator is explained as if clock is zero then NM6 and PM0 gets OFF and PM3 and PM4 potential and fn and fp reduces VDD and NM0 and NM3 reduces then outn and outp reduces to ground that is zero. At the time of designating if clock has given as input of VDD then NM6 and PM0 gets on and PM3 & PM4 gets off and potential at fn and fp rejects at the speed shown as product of current and NM6 to the fn of the capacitor, so that differential potential Vfn(p) get begins. The moderate block occurred due to NM0 and NM3 flows as Vfn(p) given as key to back to back CMOS inverters provides better protective due to input and output minimizes the clutters in signal. But the delay gets minimized when analogized to the previous designed comparator. At last NM0 and NM3 shows cutoff potential at the fn and fp decrease and reaches to ground, because it cannot enhances the transconductance of the latch.

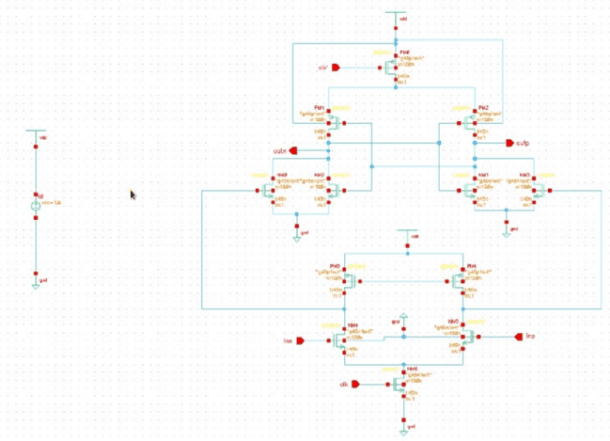

Figure3: Schematic representation of ordinary Double End comparator.

C. Existent Dynamic Comparator

The Figure4 visualizes the schematic design of the existent dynamic comparator. Due to latch revitaliser the comparator works with high speed when analogized over the precedent comparator. In addition two control transistors PM3 and PM4 are summed concurrently at the primary block and in connate PM2 and PM5 are connected back to back. And its working is substantiated as if clock is zero then NM8 and PM6 get OFF and PM2 and PM5 potential of fn and fp achieves VDD, and by neglecting nonmotile power dissipation the transistor PM5 and PM4 reduces to cutoff, while NM0 and NM3 rebegins the two latch resultants goes to ground. If clock is VDD then NM8 and PM6 gets on and PM2 and PM5 gets OFF. In the primary block, the control transistors is at the off condition, because the points fn and fp reaches to VDD. So that the potential at fn and fp points starts reducing with various speeds for the key potentials. The potential Vinp is more than Vinn then fn falls suddenly than fp. Still the potential reduces at fn point, the control transistor PM3 commences to respond by stating the potential at fp point to increase its stales and another control transistor PM4 gets OFF by substance the potential at fn point to be reduced. In the existed double end comparator, ratio of change in potential fn to the potential fp point is the key transconductance and it's the subtraction between potentials as shown in the design, so that the input ports fn reduces with speed and PM3 gets on and the point fp is used to increase its state. Such that, the subtraction between fn and fp enhances the exponential format, states to reutilization time. To get rid of static power dissipation, the two NM7 and NM5 are connected after the key transistors.

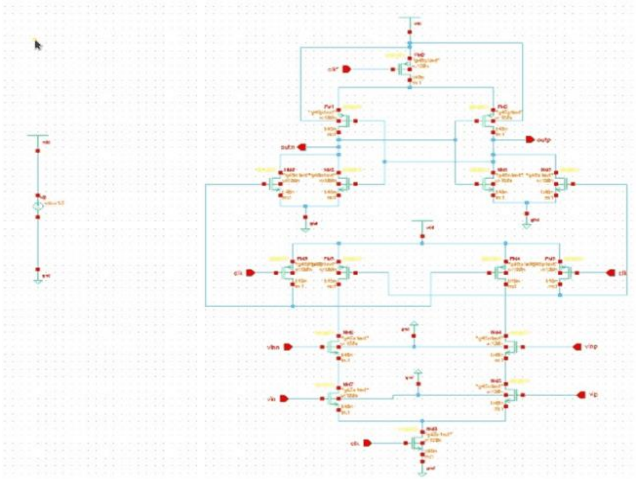

Figure4: Schematic representation of Existent Dynamic comparator.

IV. PROJECTED COMPARATOR:

The schematic design of projected comparator is visualized in Figure5. The objective of projected comparator is to minimize the power consumption, propagation delay to enhance the latch revival speed analogized over previous dynamic comparator. The working of this circuit is if the clock give as zero then NM6 gets OFF and PM4 and PM7 construct resultant points fn and fp goes to VDD, because PM5 and PM6 in cutoff. Next to the based aspect that is at the time of designing aspect, the PM5 and PM6 gets OFF on its own, and resultant points fn and fp reaches VDD and reduces with particular speeds as per the key potentials given. If the potential Vinp is higher than Vinn, So that fp reduces with high speed when compared to fn due to the transistor PM2 drags high current over PM0. At the phase of potential fp begins reducing then the other transistor PM5 gets on by changing the fn point to enhance its state. So another PM6 gets incoherent, by making fp to be reduced. While the comparator as certain if fp reduces vastly, when PMOS transistor PM5 enhances to the slack of fn. At beginning the decimating aspect, the two fp and fn points makes to VDD but after that it begins to reduces because of it is applied with to maintain the current to be taken from VDD. To get rid of the good precision, the clk' in previous comparator PM0 and PM2 are utilized in place of PM6.

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The characteristics or reliability of comparator improves the gain of the latch of intermediate block and clock running is note needed if single clock is used. If the offset reduces then resultant of gain is dragged from second stage of key transistors, and the current reduces to half of the end transistor current while analogized it to the precedent comparator and it is separated as PM0 and PM2 transistors.

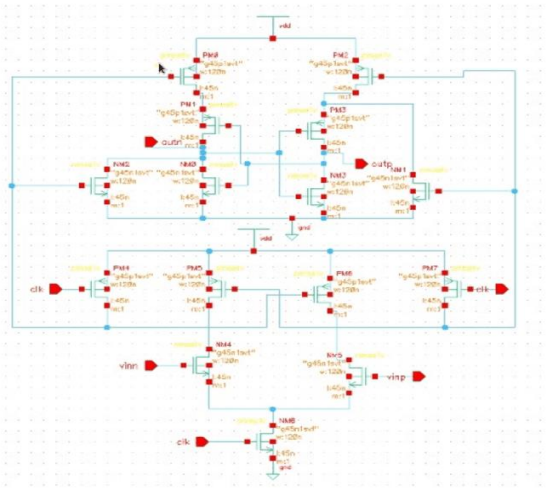

Figure5: Schematic Representation of Projected Comparator.

V. SIMULATED OUTCOMES

The presented schematic comparator is associated over the prevalent, dual end dynamic and flourishing comparator totally the designs are simulated in 45nm CMOS technology at VDD= 1.8V by utilizing cadence virtuoso tools. The projected comparator is while simulated and the results are obtained with low power, current less, propagation delay associated it over previous simulated designs are visualised in Figure 6-9.

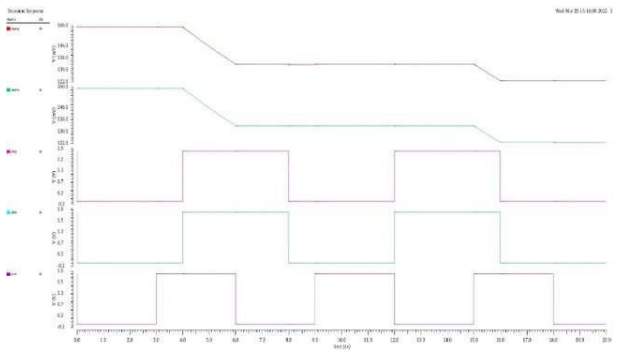

Figure6: Simulated outcomes of an ordinary Dynamic Comparator.

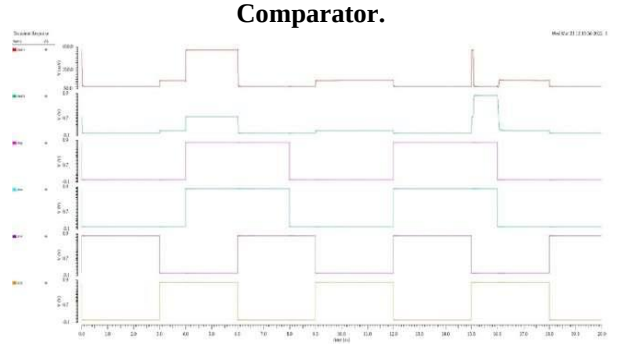

Figure7: Simulated outcomes of an ordinary Double End Comparator.

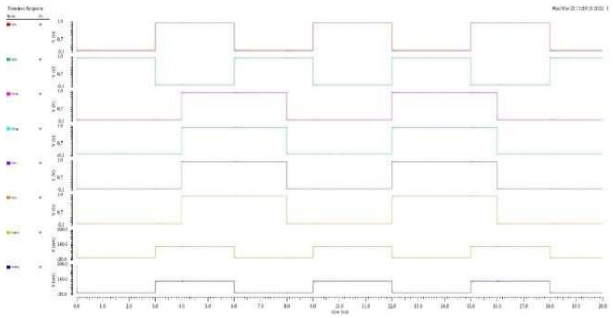

Figure8: Simulated outcomes of Existent Dynamic Comparator.

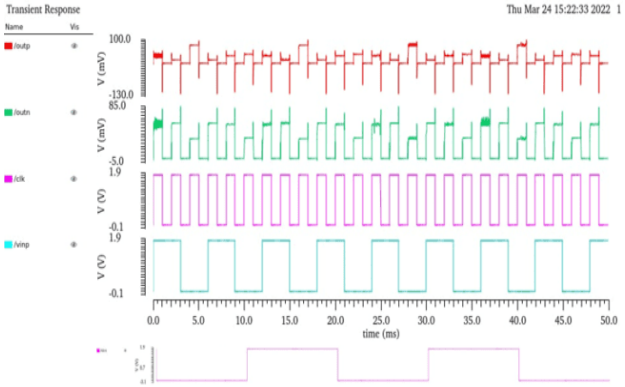

Figure9: Simulated outcomes of Projected Comparator.

Table1 Analogy of Variant Comparators

PERFORMANCE PARAMETER	Ordinary Dynamic Comparator	Double End Dynamic Comparator	Existent Dynamic Comparator	Projected Comparator
TECHNOLOGY USED	45nm	45nm	45nm	45nm
SUPPLY VOLTAGE	1.8V	1.8V	1.8V	1.8V
POWER CONSUMPTION (µW)	433.3	336.4	576.3	239.6
PROPAGATION DELAY (ps)	283	116.8	112.6	64.64
POWER DELAY PRODUCT (PDP) (femtojoules10^{-15})	122.6	39.2	64.8	15.5

VI. CONCLUSION

The projected comparator design is implemented by using cadence virtuoso tool. This design shows that it performs with less propagation delay and low Power consumption. This design optimizes the power from 576.3µw to 239.6µw represents the reduction of 41.6%, while the propagation delay minimizes from 112.6ps to 64.64ps represents the minimization of 57.4%.

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AUTHORS PROFILE

Dr. C.Arunabala, M.Tech, P.hD, Professor is having 25 years of teaching experience, presently she is working as professor in Department of ECE, KKR&KSR Institute of Technology and Sciences (KITS), Vinjanampadu, Guntur (Dt), Andhra Pradesh, India. Totally 15 publications are there in various journals. Her areas of interests are VLSI, Embedded Systems, Digital Systems and Image Processing.

P.V. Sai Ranjitha, Assistant Professor received her B.Tech degree from Chebrolu engineering college, Guntur (D.t), Andhra Pradesh and M.Tech from RVR & JC College of engineering, Guntur (Dt), Andhra Pradesh. And have 3 years of teaching experience as an Assistant professor in various engineering colleges, currently working as an Assistant professor in Department of ECE in Hindu College of Engineering and Technology Amaravathi Road, Guntur (Dt), Andhra Pradesh, India. Totally 02 publications are there in various journals. Areas of interests are VLSI, Signal Processing, and wireless communication. and wireless communication.

Bomminayuni Likhitha Gunturu Sravya, UG Scholar from KKR & KSR Institute of Technology and Sciences, Vinjanampadu, Guntur (D.t), Andhra Pradesh

Bonagiri Navyasree, UG Scholar from KKR & KSR Institute of Technology and Sciences, Vinjanampadu, Guntur (D.t), Andhra Pradesh

Arumalla Mounika, UG Scholar from KKR & KSR Institute of Technology and Sciences, Vinjanampadu, Guntur (D.t), Andhra Pradesh

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