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Design of Low Power and High-Speed Cmos D Flipflop using Supply Voltage Level (SVL) Methods

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Abstract: ***This Project details about the design of D Flip Flop (DFPFP). This D Flip Flop circuit is analyzed by using the supply voltage level methods. These methods are used mainly to suppress the power consumption caused due to leakage currents. In addition, because of this implemented technique, the time taken for battery backup, and the supply voltage given at standby mode gets minimized. The projected circuit uses a smaller number of transistors, such that power consumption and leakage currents are in prior limit. Mainly, the CMOS D Flip Flops are designed to use them in binary counters, shift registers, Analog and Digital circuit designs. And this circuit design is implemented in 45nm CMOS Technology Cadence Virtuoso Tool.***

Index Terms: Power Consumption, Leakage Current, 45nm Cmos Technology and Cadence Virtuoso Tool.

I. INTRODUCTION

The variant designs of D FlipFlop using CMOS technology are the voltage depended oscillator was developed using 0.7µm CMOS technique and a D flip flop that can handle data at high- frequencies with low power utility was implemented and succeeded. A CMOS process with 0.8µm was used to develop double module pre-scaler at high frequencies with a D flip flop and this method reduced the power usage. The circuit that works with 0.5V supply was designed using CMOS process and came out with high speed and stability related results perfectly. Also, the divide with 16.5 method was developed in 0.13µm CMOS method and the outputs provided accurate data at higher frequencies greater than previous techniques and with 18mW power usage.

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Concisely a D-flip flop that uses 2 feedbacks with no inductor was constructed using 90nm CMOS process and improved the fastness which can be used in communication systems. The proposed flip flop was built in a standard way in terms of contact, complexity and flexibility using 90nm CMOS method and found that it yields productive results when used with another circuitry. By using 130nm CMOS process, a mono-event D flip-flop was designed and measured using various techniques, concluded that it can be built in small size with the better performance [1]- [7].A new method to design D FlipFlop are 2-D cosine transform was used to develop the D-flip flop that is capable of handling data by 50% faster, 30% small in size as compared to previous techniques. And a D flip flop that is adaptable to electro-static discharge with fast raise was fabricated and found that it is capable of giving all parameters perfectly. Mainly, with the use of D flip-flop and comparator a speed based unsystematic number generator was implemented and the obtained results shows low power utility and fast propagation. Both positive and negative edge triggered D-flip-flop was designed with static and dynamic process and found that the proposed method showed high speed over a range of supply voltage. By using CAD 3-D methodology alike and unlike Fin-FET process was implemented at high quality method, resulted in the improvement of power dissipation, delay and on time successfully. A D flip flop that is adaptable for nano CMOS methods was demonstrated and equated with triple-tail latch, came up with an achievement in increasing the speed and reducing the input power at operating-frequencies. The experiments were done on a D flip-flop with the use of quick pipeline method and finally proved that by minimizing the capacitive-load speed can be increased even at high frequencies [8]-[14]. Different FlipFlops like, a magnetic-flip flop that uses power in an efficient way was built and concluded that it gives better output with low power utility as compared to ordinary CMOS flip-flop. And a hybrid magnetic D flip-flop that was fabricated using a novel method and after analysis, found that they provide delay less data with speed and small size. Concisely a magnetic D flip-flop that uses less power was demonstrated and designed using magnetic-tunnel junction diagram, finally provided standard results in flexibility, long life and stability. As well charge distribution in double interlocked cell with storage-based D flip-flop was implemented using monte carlo software and came up with successful effects in utilizing power in an efficient manner.

To design a flip flop monte carlo method was presented and calculated with large data, also compared with other methods and found its adaptability in giving all the needed values. An effective mono-event flip-flop was demonstrated and measured the overall parameters; the analysis showed its effectiveness in operating when evaluated with standard ones. Along, with the advent of a novel flip flop under mono-event calibrations were proposed and designed using 28nm CMOS process. Results shown large variations when the layout was designed in a fruitful way. Similarly, a temporary masking-based mono-event diagrams were analyzed and found that in order to minimize the event noise, the delay must be increased and input voltage must be decreased [15]-[22].

Applications like a D-flip flop that responds for both the positive and negative edges was implemented and found that it is adaptable to produce high-speed and noise free throughput. A single phased D flip-flop in time to digital converters was designed and the simulated throughputs show their capability in providing error free data with high stability [23]-[24].

II. D-FLIPFLOP SCHEMATIC IMPLEMENTATION

The Power Consumption in CMOS circuits are occurred because of three reasons those are due to the transistor, because of leakage current and also because of short circuit current which is passing from Vdd to ground. The more amount of leakage current acts as main part for power consumption to CMOS designs because threshold Potential and transistor width to length ratios have to be minimized. The FlipFlops are the main designs used for digital electronics and to find the place of data.

The result of DFlipFlop (DFPFP) will be same as input but with some delay. D denotes data, it stores the information given. In order to the D input, the clock signal should be active then only the correct output will be obtained. And this contains set (or) reset design with the CMOS inverter design.

There are two types of DFPFP those are single edge triggered (SET) and double edge triggered (DET) SET is uncomplicated and very easy to project the performance on enhancing and reducing edges of the clock pulse.

The implementation of TSPC DFPFP is with 5 transistors and it is visualized in the Figure 1. And this design consists of 3NMOS and 2PMOS transistors. This FlipFlop is designed with miniature in nature because of less number of transistors so that it reduces the power dissipation. Actually TSPC stands for true single phase clocked logic design uses one aspect of clock Pulse and avoid skew Problems while designing and performs well in digital structure. Because of this reason low power consumption is observed.

When the clock pulse and input D are employed then transistors P1, N3 gets off and unused transistors P2, N1, N2 gets ON. The result gets enhanced and highlighted. If the clock pulse is high or if it is ON state and the input is given then accordingly to the clock pulse given the output is changed. Figure 1 & 4 shows the schematic diagram and simulated outcomes of CMOS DFPFP utilizing supply voltage level methods.

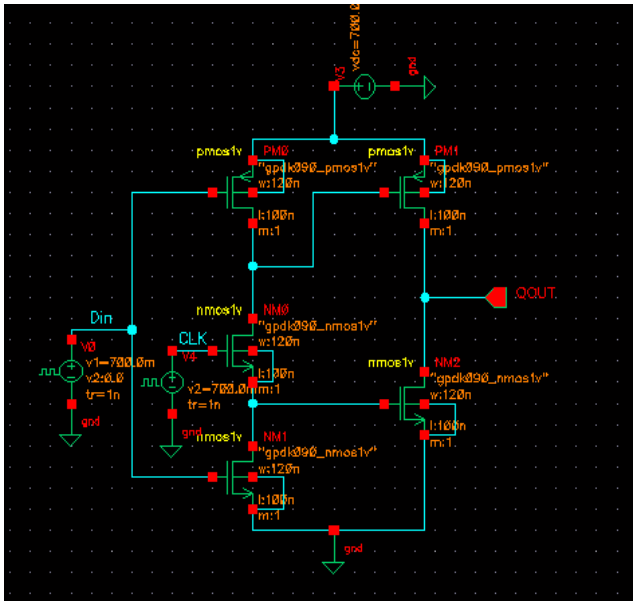

Figure1: Schematic Implementation of CMOS D FlipFlop.

III. LEAKAGE MINIMIZATION METHODS ENFORCED ON CMOS D-FLIPFLOP

A. SVL Method Enforced on CMOS D-FLIPFLOP:

SVL stands for Self-Voltage Level. This is utilized to minimize power dissipation for clocked structure as Flip-Flops at the time if it is working at standby mode.

If the clock is given to the ground that is zero Volts then Flip-Flops works as standby mode. These also follows pull up and pull down structure that is like the CMOS technology. While pull up joints to inversion of Pulse and pulls down to get joints to clock. This method will optimize Power dissipation because of clock pulse is utilized as control signal for limitation of Power supply connected. To DFPFP so that it is named as self-voltage level. If clock pulse is given as one and clock bar is zero and P1 gets on and N1 gets off and clocked structure joints to Power supply. If clock is zero, the design automatically works in standby mode. If even the power supply voltage is minimized then also the circuit operates in a good mode, such that minimizes power dissipation, mainly the leakage supply which is passing through transistors makes the transistors are in off condition so that leakage power will be minimized. If clock is zero, then N2 gets off. Here the throwback is this PMOS transistor show zero which is a bad logic and gives threshold voltage as result for pull down. If P2 is PMOS transistor joints in pull down in place of ground and gives some limited potential at virtual ground point.

The virtual ground is internally converts to power supply to take down to the NMOS transistor of limiter design. While moderate positive potential is given to source terminal of NMOS transistor and this transistor will dissipated current is optimised because of it is in standby mode.

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At the same way the pull up P1 is in OFF state and N1 in ON states the Figure2 shows bad logic because it is in pull up. And the clocked lap joints to virtual supply potential below to supply potential. So that standby mode with clocked lap will minimize the power dissipation.

The Figure5 visualizes the simulated outcomes of DFPFP by utilizing SVL method. And the DFPFP is designed with five transistors with two PMOS (P1 & P2) and three NMOS transistors (N1, N2, and N3). In this we discussed about two case, in first case if the clock given is '1' then the design acts in active condition such that P1 gets on, N2 gets ON, P2 gets off, N1 gets off then DFPFP joints to VDD and ground to normal design working. And D is in zero, then P1, N1, N3 gets ON and P2, N2 gets off, by joining Q to ground then Q becomes zero. If Din is '1' then P1, N3 gets off and N1, N2, P2 gets ON and output Q joints to Vdd then Q becomes one. The second case if the clock given is zero shows that the circuit operates in standby mode such that if Pl, N2 gets off then they act as open switches. N1 gets ON but utilized as Pull up gives the difference between supply potential and threshold potential, if the power supplies potential to DFPFP. And the NMOS transistor which is in pull up causes voltage drop because of robust quality. In the same way if P2 gets on which is in pull down gives limited positive potential rather than ground that is zero volts. The virtual ground positive potentials will be moderately reverse biased the NMOS transistors of DFPFP such that minimizes Power dissipation of DFlipFlop (DFPFP) in standby mode. And the PMOS transistors in DFlipflop (DFPFP), Power dissipation are optimized because the virtual supply is in standby mode. Figure 2 & 5 shows the schematic diagram and simulated outcomes of CMOS DFPFP utilizing supply voltage level methods.

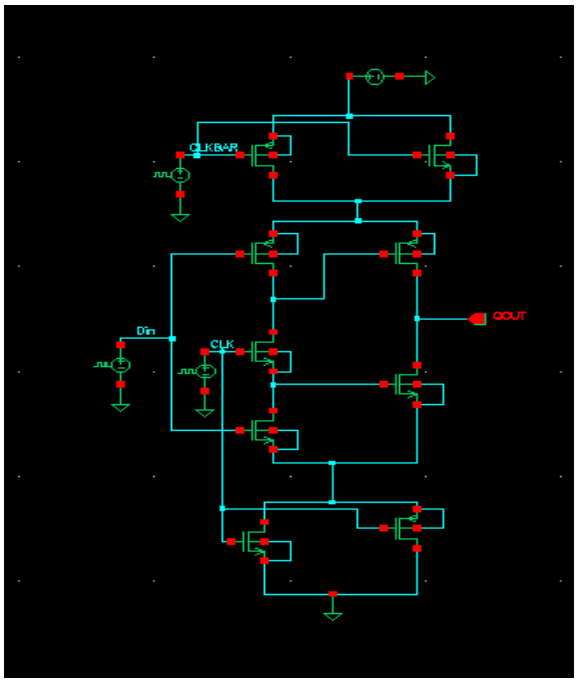

Figure2: Schematic Implementation of CMOS D Flip Flop enforced using SVL method.

B. Altered SVL Method Enforced on CMOS DFPFP:

The Figure 3 visualizes the Delay FlipFlop structure utilizing enhanced SVL method. The DFPFP is designed utilizing five transistors; those are two PMOS transistors (P1 & P2) and three NMOS transistors (N1, N2 &N3). This also contains two cases, the first case is if the clock given is '1' which is in active mode such that P1 gets ON, N2 gets ON, and P2,P3 gets OFF and N1, N2 gets OFF. Then DFPFP gets joints to Vdd and ground for normal circuit operation. And while Din is zero Pl, N1, N3 gets on and P2, N2 gets off, such that 'Q' connects to ground then a becomes Zero. And if Din is '1' ON then P1, N3 gets off and N1, N2 and P2 gets ON such that output Q joints to Vdd then Q becomes '1'. The second case is such that is clock given is '1' which operates in standby mode, so that P1, N3 gets off operates open switch. NI, N2 gets ON because of transistors in pull up it shows VDD - Vth as supply potential to Flip-flop (DFPFP). At the time of extra two NMOS transistors internally related to threshold current gets shortened. In the same way P2, P3 gets ON which are in pull down gets limited positive Potential rather than ground which is at zero volts. If the virtual ground positive potential is moderately reverse bias to NMOS transistors of DFPFP, such that optimizes power dissipation because of DFPFP, such that optimizes power dissipation because of DFPFP is in standby mode. The PMOS transistors of DFPFP leakage power gets optimized, because those are jointed to virtual supply which is in standby mode. In enhanced SVL method, the power dissipation gets optimized in addition leakage current flow also gets minimized because of the connection of extra two transistors. The basic is that supply potential for the flip-flop design is substantially optimized in static mode. The power dissipation at ideal condition is directly connected to supply potential and current, such that power dissipation is shortened for same value because of enhanced SVL method. Because of projected SVL technique the power dissipation gets optimized, in addition count of clocked transistors gets minimized. Hence working speed of design increases and also the dynamic power consumption gets optimized. So this method of DFPFP in standby mode is utilized to reduce power consumption The Figure 3 and 6 visualizes the schematic diagram and simulated outcomes of utilizing SVL method.

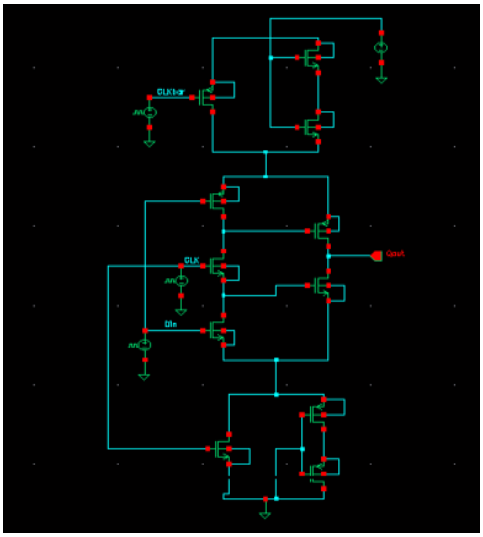

Figure3: Schematic Implementation of CMOS D Flip Flop enforced using Altered SVL method.

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IV. SIMULATED OUTCOMES

The simulated outcomes of CMOS DFPFP using Cadence Virtuoso tool using 45nm CMOS technology with supply potential of 0.7V. By using the projected techniques the power dissipation, propagation delay constraints get optimized. Specifically the enhanced SVL method for CMOS DFPFP design gives better results in terms of power dissipation, leakage current and propagation delay. Mainly by optimizing the width to length ratio of transistors the three constraints optimized automatically.

Power dissipation $P_{leak} = I_{leak}.V_{dd}$

Propagation delay = $0.69\ R_{eq} \times C_L$

C_L= Load capacitance

R_{eq}= equivalent resistance

And the Table 1 visualizes the analogy of different CMOS DFPFPs by using variant supply voltage level (SVL) techniques.

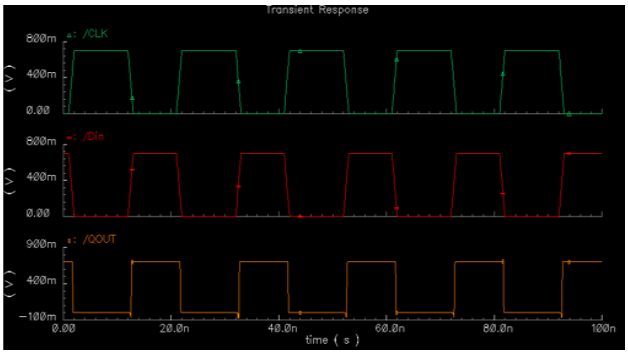

Figure4: Simulated Transient Outcome of CMOS D Flip Flop.

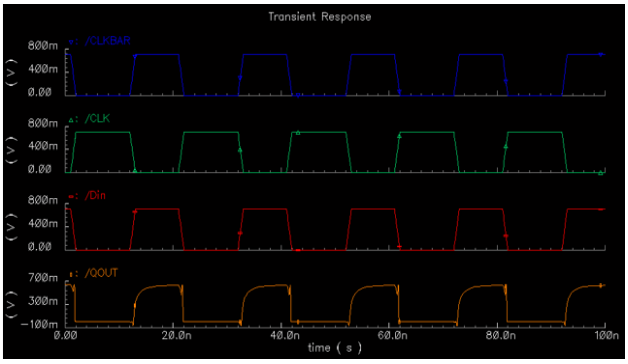

Figure5: Simulated Transient Outcome of CMOS D Flip Flop enforced using SVL method.

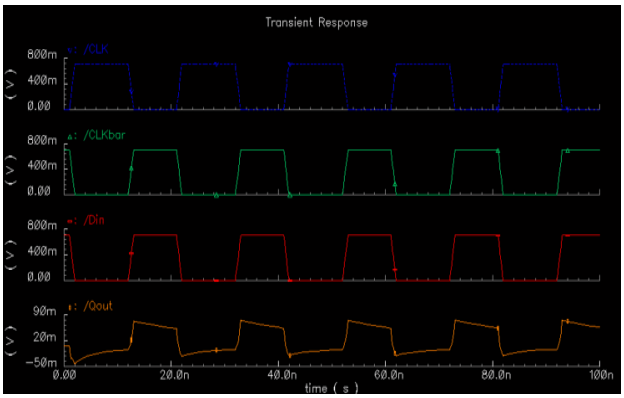

Figure6: Simulated Transient Outcome of CMOS D Flip Flop enforced using altered SVL method.

TABLE1: Analogy of CMOS DFPFP using variant Supply voltage level (SVL) methods

PERFORMANCE PARAMETER	CMOS DFPFP	CMOS DFPFP WITH SVL	CMOS DFPFP WITH ALTERED SVL	CMOS DFLIPFLOP	CMOS DFPFP WITH SVL	CMOS DFPFP WITH ALTERED SVL
TECHNOLOGY USED	90nm	90nm	90nm	45nm	45nm	45nm
SUPPLY VOLTAGE	1.8V	1.8V	1.8V	1.8V	1.8V	1.8V
POWER DISSIPATION	190.84nW	9.46nW	4.37nW	12.87nW	9.86nW	8.82nW
PROPAGATION DELAY	346.8nS	173.6nS	141.3ns	138.6ns	96.7ns	68.9ns
POWER DELAY PRODUCT (PDP) (femto joules 10^{-15})	66.18	1.64	0.62	1.78	0.95	0.61

V. CONCLUSION

Mainly CMOS DFPFP requires less Power consumption in VLSI technology mainly for battery required. Designs are main factors, so that we designed the low Power required CMOS DFPFP using SVL method, this circuit is improved by using this SVL method, so that Power dissipation, better backup, supply potential for the designed air is optimized. Altered SVL method enforced to CMOS DFPFP design optimizes Power consumption and also leakage currents in limited way. The projected schematic design consists of less number of clocked transistor count concurrently minimizes dynamic Power consumption, and also leakage current for required circuit. The implemented analogy discussion of SVL and Altered SVL methods. Explained mainly by using the constraints with data of reduced power dissipation at Voltage Potential of 1.8V and threshold potential of 1V and key control potential of 1.8V. The simulated outcomes show CMOS DFPFP with Altered SVL methods gives better results than normal SVL methods. This type of CMOS DFPFP is used at low power consumption designs. This design optimizes the power from 12.87nw to 8.82nw represents the reduction of 68.53%, while the propagation delay minimizes from 138.6ns to 68.9ns represents the minimization of 49.71%.

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