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Impact of Negative Capacitance Junctionless Nanowire (NCJLNW) MOSFET on Ring Oscillator Design and Analysis

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Abstract*: This work presents the analysis of NCJLNW for low-power analogue/RF applications. This device exhibits reduced power consumption, fewer SCEs, lower leakage, and a higher I_{on}/I_{off} ratio. The results indicate that the proposed device improves the intrinsic gain, cut-off frequency, and transconductance and reduces DIBL. The analysis of band energy, surface potential, and electric field has also shown promising results. A ring oscillator has been designed using this device; the study of the oscillator reveals a lower operating voltage, resulting in reduced power consumption and high noise immunity. The frequency of oscillation is found to be higher at 172.1 GHz at a channel length of 20 nm.

Keywords*: Drain Induced Barrier Lowering (DIBL), Ferroelectric, Negative capacitance Junctionless Nanowire (NCJLNW), Short Channel Effect (SCE).

I. INTRODUCTION

In the current scenario, there is a demand for low-power, high-performance integrated circuits to provide longer battery life and compact device size. To reduce the power consumption, supply voltage needs to be scaled, but due to 60 mV/dec subthreshold swing limitation in conventional MOSFETs, it can't be reduced in exact proportion as the other device dimensions [1]-[2]. The negative capacitance technique is employed to overcome the Boltzmann limit, thereby reducing power consumption. In this technique, a thin layer of ferroelectric material is used in the gate stack to generate negative capacitance [3]-[4]. Furthermore, at smaller dimensions, an abrupt change in doping concentration is required in conventional inversion-mode devices. This sharp change in doping concentration requires quite complex and costly fabrication steps.

To solve this difficulty, junctionless devices are being used in the fabrication of ICs at smaller dimensions [5]. Researchers have focused on junction-less transistors over the past few years due to their ease of fabrication and enhanced short-channel performance at smaller dimensions.

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There are fewer chances of the doping concentration variation due to the diffusion of doped impurities during thermal annealing [6]. Furthermore, the device's Nanowire structure enables better gate electrode control over the channel and reduces the impact of the drain electrode on the channel's electrostatics. As a result, the short-channel effects in Nanowire, such as the hot carrier effect, velocity saturation, and DIBL, are reduced [7]. Negative capacitance can thus be used as an option to improve sub-threshold swing while consuming less power. The source, channel, and drain of the junctionless transistors are uniformly doped, eliminating the need for changes in doping concentration. They are depleted due to the work function difference between the channel and gate material in the off state. For complete depletion of the channel in off condition, JLT devices are made thinner, and for sufficient O, the N current doping concentration is kept high [8]-[9]. A recently proposed concept, known as the negative capacitance FET (NCFET), offers a substantially high surface potential for low-voltage and low-power applications. Recent years have seen the emergence of NCFETs as an appealing alternative to CMOS devices, allowing for decreased dynamic power with substantially less leakage due to exceptionally low subthreshold swing (SS) in comparison to conventional FETs [10]. Higher surface potential is made possible by ferroelectric material in the gate stack because of internal voltage amplification [11]. Ferroelectric materials exhibit spontaneous polarization and hysteresis when subjected to an external electric field. SBT (Strontium Bismuth Tantalite, $SrBi_2Ta_2O_9$), PZT (Lead Zirconate Titanate), and Barium Titanate ($BaTiO_3$) are examples of ferroelectric materials. Due to fabrication benefits and better electrostatic behaviour, Si-doped HfO_2 is favoured over other ferroelectric materials found in literature [12]. Varying the

The doping concentration of Si-doped HfO_2 can change its ferroelectric properties. Negative capacitance usually appears in the ferroelectric's unstable state; thus, to use it in semiconductor devices, we need to stabilize the ferroelectric's negative capacitance state [13]. The employment of a dielectric in stack with the ferroelectric material is the most popular strategy for stabilizing the negative capacitance state. To improve control over the gate in the channel, multi-gate and surrounding gate devices are drawing the attention of researchers. Nanowire is the structure of choice due to its symmetrical structure and excellent control over the channel, resulting in reduced short channel effects and improved reliability [14].

The negative capacitance-based junctionless Nanowire provides improved ON current due to increased gate capacitance. It reduces leakage current, DIBL, and subthreshold swing, resulting in low power consumption and enhanced performance.

Furthermore, to analyse the performance of the proposed NCJLNW in analogue circuits, a ring oscillator using CMOS inverters is designed using the mixed-mode technique in Silvaco Atlas. Ring oscillators are used to produce high-speed clock signals for both analogue and digital applications, as well as high bandwidth. Static and transient analysis of the NCJLNW-based inverter and ring oscillator is performed, and various key parameters related to the circuits mentioned above are analysed. The simulation details follow the introduction section of the presented manuscript in Section 2. Section 3 contains the analogue RF analysis of NCJLNW. The study of mixed-mode circuits, such as inverters and ring oscillators, is discussed in Section 4. The concluding remark of the analysis is given in section 5.

II. DEVICE STRUCTURE AND SIMULATION SETUP

Figure 1 shows a 3D schematic depiction of the NCJLNW. To incorporate the adverse capacitance effect in the junctionless transistor, a 4nm-thick ferroelectric layer is placed over a 1nm-thin SiO_2 layer. The device's channel length is 20 nm. Table 1 shows the device dimensions and other material parameters. The JLNW and NCJLNW have been analysed using the Silvaco Atlas 3-D device simulator.

A 5-nm-radius n-type ultrathin Si layer with a doping concentration of 1 × 10^19 atoms/cm^3 is used in the device. To determine the channel's potential distribution and carrier concentration, ATLAS solves a set of fundamental equations for charge carriers. To get realistic results, appropriate physical models and carrier statistics are used. Fermi-Dirac statistics, field-dependent carrier mobility, velocity saturation, and the Auger model for generation and recombination are included—the model LKFERRO is used to incorporate the Landau-Khalatnikov ferroelectric interface model into the simulation. To simulate the ring oscillator, Mixed-Mode analysis is performed in Silvaco Atlas. Mixed-mode analysis can include the proposed devices in the circuit, along with compact circuit models. SPICE and ATLAS syntax are used together for Input file specification.

Table. I: Device parameters used for simulation

Ser. No.	Parameter	Value
1	Channel length	20 nm
2	SiO_2 thickness	1 nm
3	Ferroelectric thickness	4 nm
4	Si diameter	10 nm
5	Silicon film doping	$1x10^{19}$atoms/cm^3
6	Gate work function	5.2 eV
7	Source/Drain work function	4.1eV
8	Remnant polarization (P_r)	5 μC/cm^2
9	Coercive field (E_c)	1.1 MV/cm
10	Saturation polarization (P_s)	9.5 μC/cm^2
11	Ferroelectric permittivity	30.25

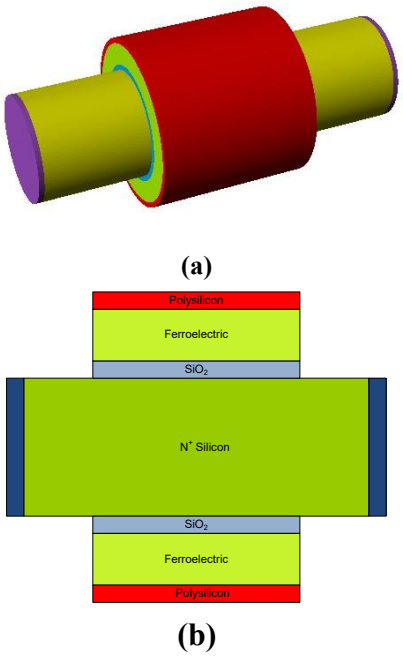


Fig. 1. (a) 3D view of NCJLNW, (b) 2D cross-section of NCJLNW

III. ANALOG RF ANALYSIS OF NCJLNW

To evaluate the performance of NCJLNW compared to JLNW in analogue and digital circuit applications, a device-level analysis of these devices is undertaken first. The device properties of individual JLNW and NCJLNW have been investigated in this section. To examine the usefulness of the negative capacitance phenomenon in circuit applications, all device parameters obtained for NCJLNW are compared with those of JLNW. The device-level study of JLNW and NCJLNW has then been extended to the circuit level in Section 4 by employing these devices to create a CMOS inverter and ring oscillator. Table I lists the device parameters used throughout the analysis. Figure 2 shows the energy band diagram of JLNW and NCJLNW at Vgs = 0 V and Vds = 0 V. We find that the use of negative capacitance increases the barrier height, resulting in reduced leakage current.

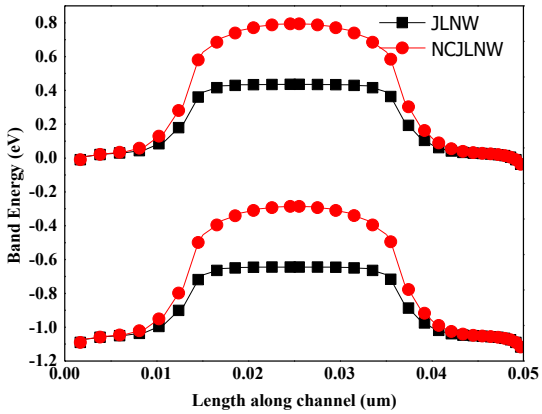


Fig.2. Band energy in JLNW and NCJLNW at V_{ds}=0 and V_{gs}=0

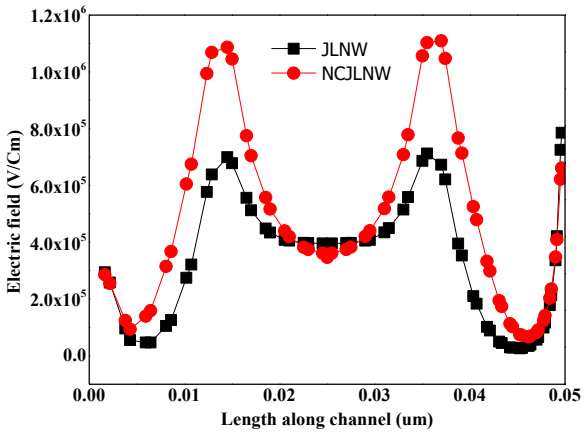


Fig.3. Electric field in JLNW and NCJLNW

Figure 3 depicts a rise in the electric field in the channel of NCJLNW due to increased surface potential. Enhanced surface potential and reduced subthreshold swing because of ferroelectric material enhance the electric field at the source channel and channel drain interfaces [15]. The increased electric field causes carriers in the ON state to drift faster, resulting in an elevated I_{on} and improved I_{on}/I_{off} ratio.

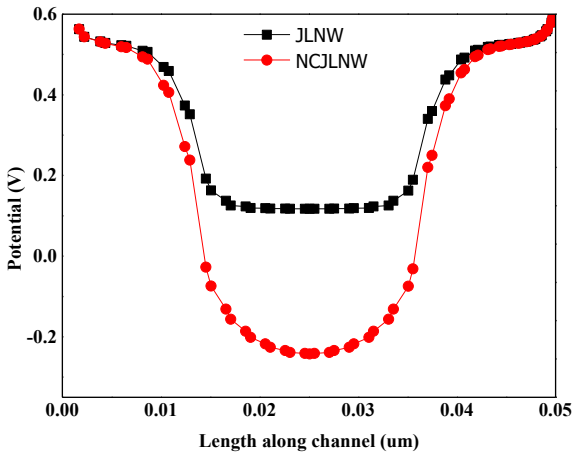
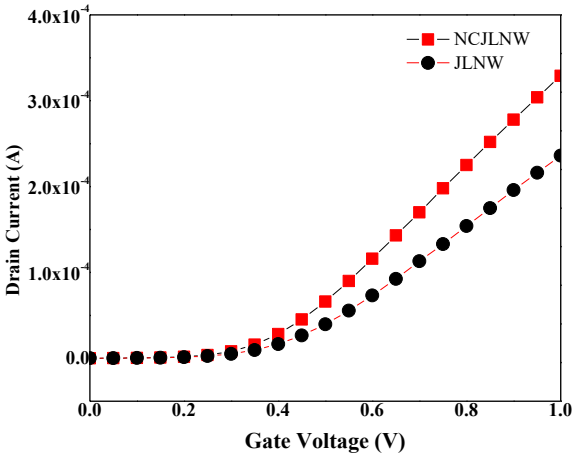
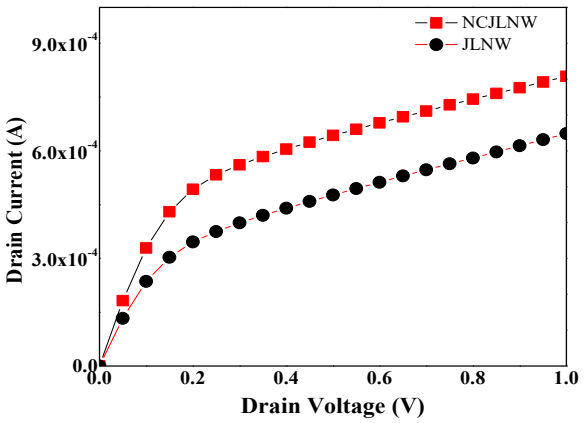


Fig.4. Potential in JLNW and NCJLNW

The variation of surface potential in JLNW and NCJLNW is shown in Figure 4. NCJLNW has a substantially lower surface potential in the channel region than JLNW in the off state, resulting in a smaller amount of leakage current.



(a)



(b)

Fig.5. (a) Id vs. Vgs and (b) Id vs. Vds in JLNW and NCJLNW

NCJLNWs have a smaller surface potential in the subthreshold region, resulting in a higher potential barrier and reduced leakage. Additionally, in comparison to JLTs, the drain current curves for NCJLTs become sharper, indicating enhanced switching. The increase in I_{ON} and reduction in I_{OFF}, subthreshold swing and DIBL are indicated in Table II. Further, the device properties of NCJLNW and its conventional counterpart have been thoroughly discussed. Drain current (I_d), gate capacitance (C_{gg}), and transconductance (g_m) are used to derive device analogue and RF characteristics. At a given drain bias, transconductance is defined as the ratio of the change in drain current to the gate-to-source voltage ($gm = Id/V_{gs}$). It represents the gain, and its high value implies that the device is performing well. The cut-off frequency is the highest frequency at which a device can function as an amplifier. The drain current equals the gate current at this frequency, and the small-signal current gain equals unity. ($f_T=g_m/2\pi(C_{gs}+C_{gd})$) It is its mathematical expression. Here, Cgs and Cgd are the gate-to-source and gate-to-drain capacitances, respectively. The ratio of the device's transconductance (g_m) to its output conductance (gd) is known as intrinsic gain ($Av = gm/g_d$). It shows the device's voltage gain, and a greater inherent gain value suggests better performance [16]. The transconductance generation factor (TGF) is the ratio of transconductance (g_m) to the output current (I_d). Higher TGF enables the circuit to work efficiently at lower supply voltages and to consume less power. The TGF mathematically illustrates the power-delay trade-off. The product of transconductance and cut-off frequency is the Transconductance frequency product (TFP = TGF × fT).

Table. II: DC parameter values in JLNW and NCJLNW

Ser No	Parameter	JLNW	NCJLNW
1	Threshold voltage (V)	0.22	0.26
2	Subthreshold swing (mV/dec)	64.7	44.2
3	On current (A)	$2.36x10^{-4}$	$3.29x10^{-4}$
4	Off current (A)	$8.11x10^{-10}$	$1.47x10^{-12}$
5	I_{on}/I_{off} ratio	$2.91x10^{5}$	$2.23x10^{8}$
6	DIBL (mV)	28	16

It indicates a trade-off between power and bandwidth [17][18].

For JLNW and NCJLNW, Figures 5(a) and 5(b) show drain current vs. gate voltage and drain current versus drain voltage, respectively. The ability of NCFETs to enhance surface potential with respect to the gate voltage is represented by the peak in current for NCJLNW in Figure 5.

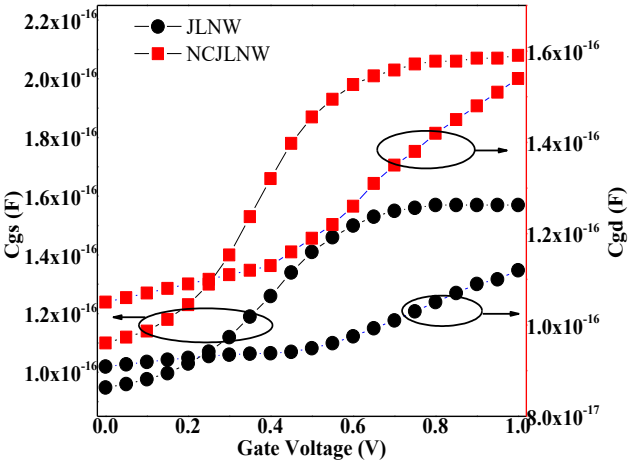


Fig. 6. Cgs vs Vgs and Cgd vs Vgs in JLNW and NCJLNW

For JLNW and NCJLNW, Figure 6 illustrates how the gate-to-source capacitance (Cgs) and gate-to-drain capacitance (Cgd) change with the gate voltage. When comparing NCFETs to standard JLTs, the improvement in gate capacitance is noticeable. The use of ferroelectric material results in a considerable increase in gate capacitance. These high gate capacitance values result in improved switching behavior of NCFETs, which is critical in digital circuit applications.

The fluctuation in intrinsic gain and cut-off frequency with regard to V_{gs} for JLNW and NCJLNW is shown in Figure 8.

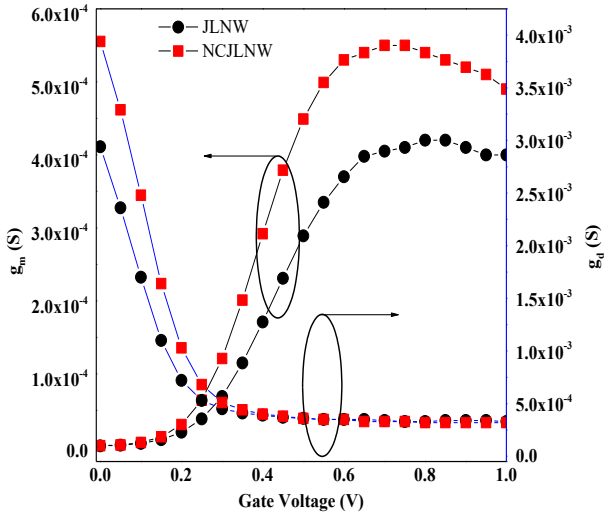


Fig.7. gm vs Vgs and gd vs Vgs in JLNW and NCJLNW

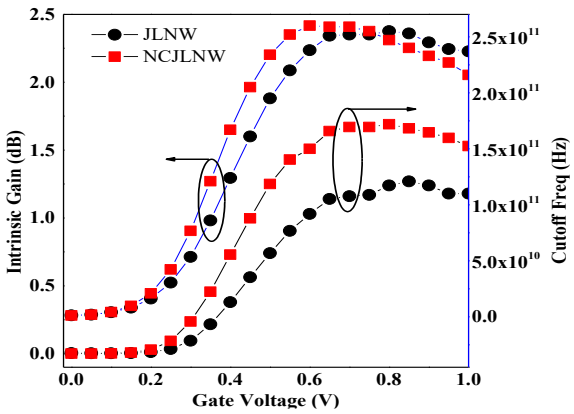


Fig.8. Av vs Vgs and fT vs Vgs in JLNW and NCJLNW

The intrinsic gain of NCJLNW is larger than that of JLNW and has a greater cut-off frequency than JLNW at lower V_{gs} levels. NCJLNW, on the other hand, has a lower cut-off frequency than JLNW at larger V_{gs} levels.

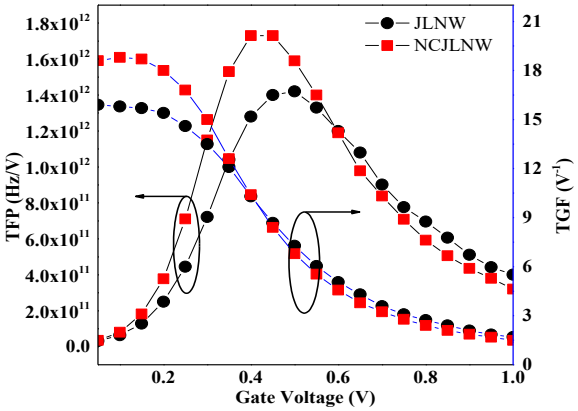


Fig. 9. TGF vs Vgs and TFP vs Vgs in JLNW and NCJLNW

For high-frequency applications, the transconductance frequency product (TFP) is an essential characteristic. Figure 9 shows TFP as a function of V_{gs}. For a lower gate voltage value, NCJLNW has a higher TFP than JLNW; as Vgs increases, the TFP value drops. TGF is highest at the device's sub-threshold area, as seen in Fig. 9. NCJLNW

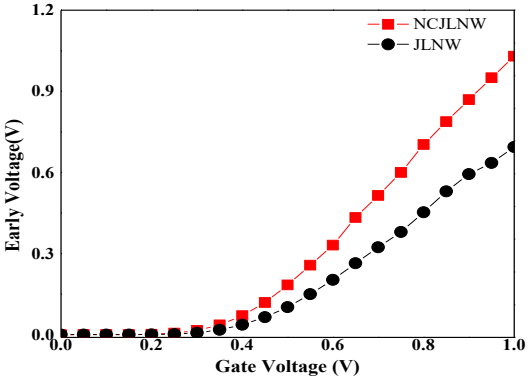


Fig.10. Early Voltage vs. Vgs for JLNW and NCJLNW at Vds=1V

has a larger TGF than JLNW at lower gate voltages, indicating a high gain per unit of power dissipation [19]. Both devices have virtually identical TGF when V_{gs} is increased.

Table. III: Analog / RF Parameter Values

Ser No	Parameter	JLNW	NCJLNW
1	Transconductance (S)	$4.2x10^{-4}$	$5.5x10^{-4}$
2	Output conductance (mS)	3.02	4.16
3	Intrinsic gain	2.39	2.43
4	Cutoff frequency (Hz)	$1.35x10^{11}$	$1.71x10^{11}$
5	Transconductance generation factor (V^{-1})	16.9	19.5
6	Transconductance frequency product (Hz/V)	$1.42x10^{12}$	$1.73x10^{12}$
7	Early voltage (V)	0.69	1.03

Early voltage (VEA = Id/g_d) is the ratio of drain current to output conductance. The device's output conductance should be low, resulting in a greater early voltage value. For proper device operation, this should be as high as possible. Figure 10 shows the early voltage variation, indicating that NCJLNW's value is 26.8% greater than JLNW's, demonstrating better analogue performance. Table III presents the peak values of various analogue parameters. Negative capacitance increases transconductance by 30.9 %, intrinsic gain by 1.6 %, cut-off frequency by 26.6 %, TGF by 15.3 %, TFP by 21.8 %, and early voltage by 49.2%. The improved performance metrics of the NCJLNW device suggest that it is a suitable choice for analogue applications.

IV. RING OSCILLATOR CIRCUIT USING NCJLNW

In this section, a high-performance and power-efficient ring oscillator circuit is designed using the negative capacitance-based JLNW. As shown in Figure 11, a ring oscillator is made up of three inverter stages in cascade. The performance of individual inverter stages is analysed in the next part of Section 3 of the manuscript. All three inverter stages are assumed to be identical, and the output load capacitances are expected to be equal with the value (C_{L1}=C_{L2}=C_{L3}=C_L=6fF). Furthermore, the output load capacitance affects the delay computation in a CMOS inverter. The entire parasitic capacitances between the output node and the ground can be combined to compute the accurate value of the output load capacitance [20]. The parasitic capacitances in nano-scaled transistors are C_{gs}, C_{gd}, C_{sb}, and C_{db}. Furthermore, because the source-substrate potential is kept at zero in P-type and N-type JLNW, the source-to-bulk capacitance (C_{sb}) has essentially little effect on the transient characteristics of CMOS inverters. The drain-to-bulk parasitic capacitance (Cdb), the gate-to-source capacitance (Cgs), and the gate-to-drain parasitic capacitance (C_{gd}) will all be included in the computation.

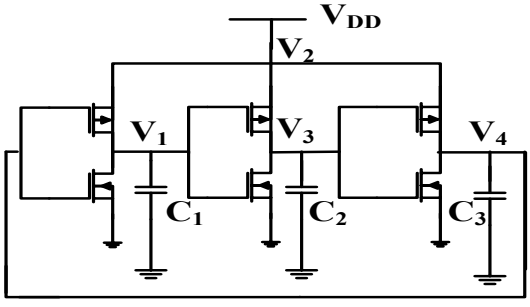


Fig.11. Three-Stage Ring Oscillator Circuit Designed Using Proposed NCJLNW

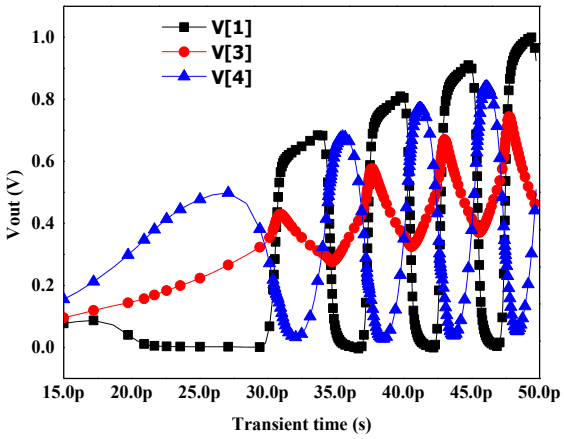


Fig.12. Ring Oscillator Output

For L = 20 nm, the maximum output load capacitance (C_L = $C_{gd,p}$ + $C_{gd,n}$ + $C_{gs,p}$ + $C_{gs,n}$ + $C_{db,p}$ + $C_{db,n}$) is calculated as 3.257 fF, and it significantly reduces with channel length scaling. To investigate the parasitic behavior of the proposed device at smaller dimensions, we used the maximum value of parasitic load capacitance C_L = 6 fF. The transient and DC analysis of the proposed individual inverter stage has been performed in the next section using the ATLAS Silvaco numerical simulator.

The frequency of the generated output of the oscillator, as simulated, is 172.1 GHz. Its value, calculated using the formula in Equation 1, is found to be 171.3 GHz, as shown in Table IV. This result indicates that the NCJLNW can be used in high-frequency analogue applications. The frequency of oscillation in a ring oscillator is given by:

$$f_{osc} = \frac{1}{2\,N\,\tau_{pNCJLNW}} \quad (1)$$

Where N is the total no of stages and $\tau_{pNCJLNW}$ indicates the propagation delay of an individual inverter stage.

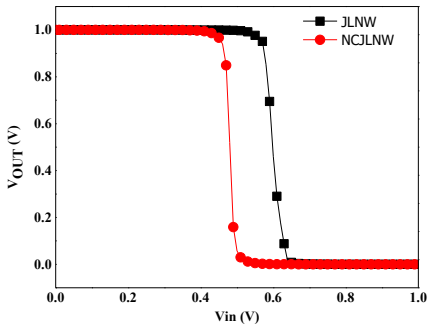


Fig.13. DC Characteristics of Inverter using JLNW and NCJLNW

A CMOS Inverter designed using NCJLNW is used as the basic building block of a three-stage ring oscillator. The sensitivity of integrated circuits to noise is crucial, as they operate at extremely low signal levels. The noise margin (NM) is the amount of noise that a circuit can tolerate. Furthermore, the logic circuit may not function properly, raising a concern about its reliability.

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As a result, the NMs must be as high as possible [21]. High NMs, on the other hand, cause huge voltage excursions, resulting in longer delays and increased power dissipation. As a result, a trade-off must be maintained between NMs, latency, and power.

$$NM_L = V_{IL} - V_{OL} \quad (2)$$

$$NM_H = V_{OH} - V_{IH} \quad (3)$$

Based on equations (2) and (3), NMs are calculated for the proposed inverter circuit. NM_L and NM_H are Low and high NMs, respectively. Furthermore, VIL and VOL in Eq. (4) represent low-level input and output voltages, respectively, while VIH and VOH denote high-level input and high-level output voltages, respectively. It is worth mentioning here that the value of VOL can be assumed to be low, tending to 0 V, and VOH is equal to VDD (i.e., 1 V). From simulated VTC (figure 13), we find $V_{OL,\ NCJLNW}$ = 0V, $V_{OH,\ NCJLNW}$ =1V, $V_{IL,\ NCJLNW}$ =0.44V and $V_{IH,\ NCJLNW}$ =0.52V. Therefore, from Equations 2 and 3, NML and $_{NCJLNW}$ are 0.44 V and 0.48 V, respectively. Similarly, for JLNW, it is found that VOL, JLNW = 0 V, VOH, JLNW = 1 V, VIL, JLNW = 0.42 V, and VIH, JLNW = 0.54 V. Therefore, from Equations 2 and 3, NML, JLNW, and $NM_{H,\ JLNW}$ are 0.42 V and 0.46 V, respectively. A smaller noise margin indicates that a circuit is more sensitive to the noise.

Table IV: Oscillation Frequency of 3-Stage Ring Oscillator

Ser No.	Device for ring oscillator	Oscillation Frequency (GHz)
1	JLNW	137.4
2	NCJLNW	172.1

Based on propagation delays, the transient analysis of the proposed inverter circuit is discussed. The propagation delay affects both dynamic power dissipation and frequency [22]-[23]. As a result, the IC designer's primary concern is timing analysis. The time it takes for a circuit to produce an output as soon as the input is applied is known as propagation delay. The average of two forms of propagation delays that must be encountered to evaluate the timing limitations of the proposed circuit is the propagation delay of a CMOS inverter. These delays depend on the transition from low to high voltage levels and vice versa. The first one is P_{HLJLNW}, which is calculated based on the transition from high to low (1 • 0). For the transition from low to high (0–1), P_{LHJLNW} is considered.

Table- V: Inverter Delay in JLNW and NCJLNW

Ser No.	Device	Propagation Delay (ps)
1	JLNW	2.04
2	NCJLNW	1.18

From Table V, it can be seen that the NCJLNW has a relatively minor propagation delay of 1.18 ps compared to 2.04 ps for the JLNW-based device. The reduction in delay is due to the reduced subthreshold swing achieved by using the negative capacitance technique. This results in faster switching from the off state to the ON state, yielding a quicker transition and a steeper curve. The reduction in propagation delay makes NCJLNW a suitable candidate for high-performance, low-power, low-noise, and high-speed analogue circuits.

V. CONCLUSION

The analogue performance of metal ferroelectric insulator semiconductor (MFIS)-structured NCJLNW has been investigated. The negative capacitance approach reduces the subthreshold swing and OFF current, while increasing the ON current. Furthermore, it improves the GM, fT, TGF, and TFP of the device, indicating better analogue performance. The proposed NCJLNW-based CMOS inverter has a high noise margin and closely follows the supply voltage scaling trends. The intended ring oscillator has an individual inverter delay of 1.18 ps, and the oscillation frequency is calculated to be 172.1 GHz. Thus, the investigated nano-scaled device could be a suitable alternative for designing high-density ICs with low power and high performance in biomedical and sensor applications.

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Availability of Data and Material/ Data Access Statement	Not relevant.
Authors Contributions	All authors have made substantial contributions to the conception and design, or acquisition of data, or analysis and interpretation of data; have been involved in drafting the manuscript or revising it critically for important intellectual content, and have given final approval of the version to be published. Each author has participated sufficiently in the work to take public responsibility for appropriate portions of the content. All authors read and approved the final manuscript.

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