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Quantum Circuit Optimization of Arithmetic Circuits using ZX Calculus

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Abstract: ***Quantum computing is an emerging technology in which quantum mechanical properties are suitably utilized to perform certain compute-intensive operations faster than classical computers. Quantum algorithms are designed as a combination of quantum circuits that each require a large number of quantum gates, which is a challenge considering the limited number of qubit resources available in quantum computing systems. Our work proposes a technique to optimize quantum arithmetic algorithms by reducing the hardware resources and the number of qubits based on ZX calculus. We have utilized ZX calculus rewrite rules for the optimization of fault-tolerant quantum multiplier circuits where we are able to achieve a significant reduction in the number of ancilla bits and T-gates as compared to the originally required numbers to achieve fault-tolerance. Our work is the first step in the series of arithmetic circuit optimization using graphical rewrite tools and it paves the way for advancing the optimization of various complex quantum circuits and establishing the potential for new applications of the same.***

Keywords: ***Circuit Optimization, Quantum Circuit, Quantum Computing, T-count, ZX-calculus.***

I. INTRODUCTION

In classical computing, vast amounts of data cannot be computed simultaneously which makes it impractical to model and solve problems of such data-intensive nature. The large-scale fault-tolerant realization of quantum computers on the contrary, is promising due to its ability to compute these amounts of data simultaneously, opening up a wide range of applications like prime factorization of large numbers, molecular structuring to find new drugs and cybersecurity. Quantum circuit computations are performed using quantum algorithms, which make use of various arithmetic circuits such as subtraction, multiplication, and addition.

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Any implementation of these circuits is conditional to keeping the overall resources consumed at an acceptable level, which is achieved by the process of Quantum circuit optimization, usually at a gate level as a collection of gates generally contains all one-bit quantum gates and hence the 2-bit quantum ex-or gate or exclusive-or gate can also be represented as a combination of these gates [1][15][16][17]. Quantum circuit optimization is a vital topic in the study of quantum circuits and can be defined as the transformation of given computations into novel circuits using fewer or simple gates while maintaining their functionality. Since the beginning, when quantum circuits were designed using quantum algorithms, research has been carried out for the compilation and optimization of these circuits. The techniques used target various facets like minimizing the qubits count [2, 3], ancilla bits and garbage bits, reduction in the limitations due to hardware resources [4] and in the number of gates that are more expensive when simulated in error-corrected hardware [5]. For instance, the ancilla constant inputs and outputs are used for computation but are not useful since the input or output is garbage bit [6] and therefore the circuit overhead such as the ancilla and garbage outputs need to be minimized. An example of these optimization was the implementation of a reversible quantum integer multiplier that was a garbage output optimized circuit which achieved an efficiency of sixty to ninety per cent compared to the existing designs [7]. Despite research in this field, the optimizations were costlier to implement in error-corrected hardware error [5] and correction protocols were not investigated in the early work. When assessing optimal circuit constructions, these protocols place constraints on the cost metrics. Many papers have begun to recognize that to implement fault-tolerant circuits, Clifford + T universal gates can be utilized to overcome noise-error imposed limits. By avoiding uncontrollable errors caused by the quantum-bits interaction, also known as Quantum fault-tolerance, the circuits are more robust and accurate in design. The presented concept underlays the framework for large-scale quantum circuit optimization of fault-tolerant quantum circuits. The techniques like gate substitution, calculation 2 of small (false-)normal forms for distinct families of circuits, and optimization of phase polynomials are the most common approaches for quantum circuit optimization [5]. A novel method of quantum circuit optimization, formulated from the ZX-calculus is presented here. The circuits are first interpreted as ZX-diagrams, which provide a flexible, low-level language graphical description of quantum calculations [8].

Using the rules of ZX-calculus, a strategy for simplification can be devised and to demonstrate that the final reduced diagram obtained can be translated back into a quantum circuit. This optimization method provides a new normal form which is desirable in size and reduces the T-gate count of quantum circuits. For Clifford + T gate circuits, this method helps us to investigate or explore gates that interfere with the Clifford architecture [8]. The above is demonstrated by implementing a fault-tolerant 6-qubit multiplier, followed by the optimization of the same. The paper is organized as follows. In section 2, the methodology behind the implementation of quantum gates is discussed, followed by a brief overview of ZX calculus.

The section concludes by discussing the implementation of the Multiplier circuit. Section 3 highlights the key steps of the execution and optimization results. Section 4 discussed the results and Section 5 provides the conclusion to the work.

II. PRELIMINARIES

Quantum gates act as building blocks to quantum circuits. They operate using qubits, also known as quantum bits, which have quantum information encoded in them. The entanglement property helps the quantum gate to avoid loss of information since the qubits are entangled inside a quantum gate. The Clifford gate sets are utilized to carry out the fault-tolerant circuit implementation. It is already shown that the Gottesman Knill theorem allows efficient classical simulation of quantum circuits composed of gates in the Clifford set[9][18][19]. This makes it possible to simulate circuits with several gates in the order of 1000[10, 11]. This however needs a quantum computer that needs to use gates outside of the Clifford set so that the speed is maintained. It is commonly noted for most models to have Clifford group with an efficient set of generators while the non-Clifford group gates require more expensive procedures to implement [12].The most popular non-Clifford gate to use in conjunction with the Clifford set is the T gate. The gates included in the set, along with a few other elementary gates are described below it.

A. Quantum Gates

- *Hadamard Gate:* The Hadamard gate is used to create superposition of states in a single qubit. It is represented as shown in Fig 1. A superposition of |0 > and |1 > states can be visualized as the displacement away from the polar point of a Bloch sphere. The gate can be defined as follows –

$$H = \left(1/\sqrt{2}\right) \times \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \quad (1)$$

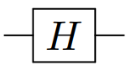

Fig. 1: Hadamard Gate

- *T Gate:* The T gate is used to induce a π/4 phase on a single qubit and can be related to the Phase gate and the fourth root of Pauli-Z. However, it is not a Clifford gate. It is represented as shown in Fig 2. The gate can be defined as follows –

$$T = \begin{matrix} 1 & 0 \\ 0 & e^{\left(\frac{i\pi}{4}\right)} \end{matrix} \quad (2)$$

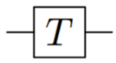

Fig. 2: T Gate

- *Hermitian of T Gate:* The Hermitian of T gate is used to induce a negative π/4 phase on a single qubit and can be related to the S gate as well (as the product of the S gate with itself). The gate can be defined as follows –

$$T^T = \begin{matrix} 1 & 0 \\ 0 & e^{\left(\frac{-i\pi}{4}\right)} \end{matrix} \quad (3)$$

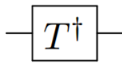

Fig. 3: Hermitian of T Gate

- *Phase Gate:* The Phase gate induces a 90-degree rotation about the Z-axis. It is represented as shown in Fig 4. The gate can be defined as follows –

$$S = \begin{matrix} 1 & 0 \\ 0 & i \end{matrix} \quad (4)$$

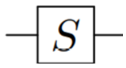

Fig. 4: S Gate

- *Hermitian of Phase Gate:* The Hermitian of Phase gate induces a 90-degree rotation about the Z-axis. It is represented as shown in Fig 5. The gate can be defined as follows –

$$S^T = \begin{matrix} 1 & 0 \\ 0 & -i \end{matrix} \quad (5)$$

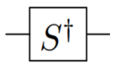

Fig. 5: Hermitian of S Gate

- *NOT Gate:* Similar to a classical NOT gate, the quantum NOT gate also reverses the state of a qubit. It is represented as shown in Fig 6. The gate can be defined as follows –

$$NOT = \begin{matrix} 0 & 1 \\ 1 & 0 \end{matrix} \quad (6)$$

Fig. 6: NOT Gate

- *CNOT Gate:* The CNOT gate is a 2-qubit gate, where one qubit is a control qubit and the other is a target qubit, upon which the X gate is applied to if the control is true. It is represented as shown in Fig 7. The gate can be defined as follows –

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$$CNOT = \begin{matrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{matrix} \qquad (7)$$

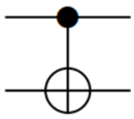

Fig. 7: CNOT Gate

B. ZX-Calculus

Having gone over the basic quantum gates and their function, the other concept that requires some background is ZX-Diagrams and their Calculus. ZX-diagrams are essentially a graphical representation of complex matrices of size 2n × 2 m. This notation allows calculations to be done with it, which can simplify the effort that it would otherwise take. A ZX-diagram consists of spiders and wires, which constitute the basic building blocks of ZX-Calculus. The thin lines are called wires, where the ones that are present on the left of the dot are inputs and any wires that are to the right side of the same are outputs [8]. Spiders, also known as generators are linear maps with the probability of having many inputs or outputs. There are two types of spiders: the Z spider illustrated as a green dot and the X as a red dot where each represents a complementary set of bases. This can be seen in Fig 8.

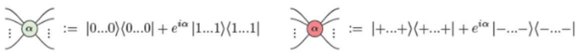

Fig. 8: Z and X Spiders

This linear mapping built using spiders is used to model different quantum gates. ZX-Calculus has been used in the simplification of circuits in the past as well. One popular method combines the 'sum-of-stabilisers' method with an automated simplification strategy based on the ZX calculus. They adapted these techniques from the original setting of Clifford circuits with magic state injection to generic ZX-diagrams and show that, by interleaving this" chunked" decomposition with a ZX-calculusbased simplification strategy, stabilizer decompositions can be obtained that are many orders of magnitude smaller than existing approaches [13]. Similarly, the usability of ZX-Calculus for small computations on quantum circuits and states is already discussed along with the Clifford computation and graphical proof of the Gottesman-Knill theorem, and the recent completeness theorems for the ZX-calculus that show that, in principle, all reasoning about quantum computation can be done using ZX-diagrams [14] There are two main differences between ZX diagrams and quantum circuits. ZX-diagrams need not conform to a rigid topological structure of circuits and hence can be deformed continuously. The second is that there are a set of rewrite rules for ZX-diagrams like the copy rule, Bi-algebra rule, and fusion rules collectively referred to as the ZX-calculus. An example of simplification of a ZX-diagram is demonstrated below – Let us begin with a ZX-diagram with 3 CNOT gates as shown in Fig 9.

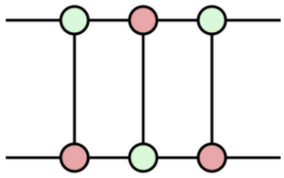

Fig. 9: ZX-Diagram of Circuit with 3 CNOT Gates

We can apply the bi-algebra rule to this.

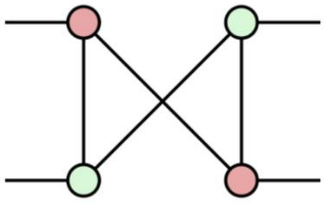

Fig. 10: After Bi-Algebra Law is Applied

Next, we can pull the gate through the swap as shown in Fig 11.

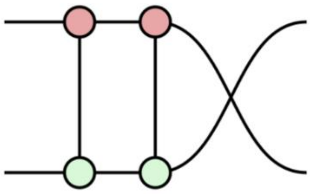

Fig. 11: Circuit After Swap Gate

This is followed by merging the two red nodes and two green nodes.

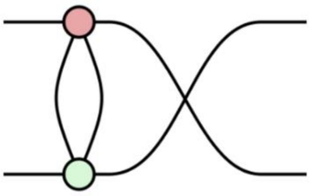

Fig. 12: Merging the Nodes

To this, we can apply the Hopf law as shown in Fig 13

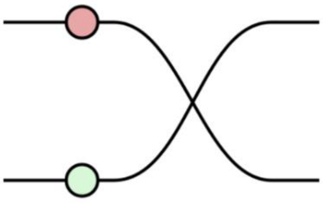

Fig. 13: Circuit after Hopf Law is Applied

Finally, passing this through the swap gate removes the blank spider and gives us the simplified diagram as shown Fig 14

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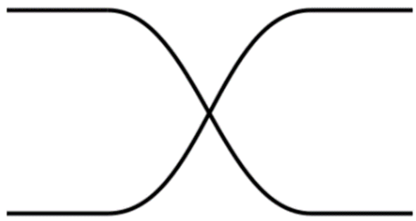

Fig. 14: ZX-Diagram of Simplified Circuit

III. METHOD

The fault tolerant implementation of quantum arithmetic circuits is gaining a lot of attention from the research community because of their fundamental use in a variety of applications and the need to adjust for physical quantum computers' proclivity for noise error. There are various such implementations, such as Integral multiplication, Integral Divider, Non-restoring square root. These form a class of fundamental arithmetic circuit implementations. For instance, one implementation of the Integral Multiplier is by Thapliyal et al.,2019. The modules do not produce any garbage outputs and also restore inputs to their starting value and therefore is an efficient implementation in terms of Qubit use and T-gates. Other implementations include Galois Squaring and Exponentiation, Bilinear Interpolation and Reversible Square. All of these can be optimized for their T-count or T-depth in their fault-tolerant implementations as the quantum T gate, which is a non-Clifford gate, used to obtain a universal gate set

A. Integer Multiplier Circuit

For the implementation of Quantum Multiplier circuit using Shift and Add algorithm, conditional Adder circuits are utilized. In conditional adder circuit, two sets of input signals A and B are given, along with the 'ctrl' input. Quantum registers are used to store the following qubits, i.e., for a n bit conditional adder, a quantum register for first input A with n qubits and 2 qubits, a second quantum register for input B with n qubits and another quantum register with a single qubit for control input are used. Registers form the basis of quantum circuit. Quantum operations are forced sequentially on quantum bits to generate the result. The nth qubit in first Quantum Register is transformed to MSB and the n qubits in the second quantum register transforms to the other bits of the sum. All the other qubits are unchanged at the output. The circuit is as shown in Fig 15. The conditional Adder circuits are placed in a shifted manner to perform multiplication. For the multiplication of two n bit numbers, n conditional adders are used. The first stage of adder can be replaced by an array of Toffoli gates, which helps to reduce the overall T-count in the circuit. The T gate count in a 6-bit conditional adder is 140, whereas Toffoli gate array has only 42 T gates. There are 25 qubits in this quantum circuit, 6 of which correspond to the first input, 6 again to the second input and 13 ancilla inputs initialized to zeroes. Each of the 6 qubits in the second input acts as the control input to a corresponding conditional adder. At the end of computation, 12 ancilla bits contain the 12 product bits and the final ancilla input is unchanged

B. ZX Optimization

ZX calculus is a graphical language which can be used to create graphical representations of quantum circuits. The calculus works by using Z and X functions, which allows us to modify the quantum circuit model while maintaining soundness of reasoning. By this way, the properties of circuits, protocols, and entanglement states, can be depicted in a visually clear and logically complete order. ZX optimization begins with the ZX-diagrams being converted to graph-like form where every spider is only of the Z type which can be achieved using twisting and re-definition, and every spider is associated with some output and no non-zero phases. This is followed by the process of removing as many internal spiders in the graph-like form by pivoting and inverting allowed by a set of rules in ZX-calculus. These core rules of ZX-calculus help in simulating the Clifford + T gate set easily. We can simulate simplified ZX-diagrams that do not have an equivalent quantum circuit as ZX-diagram has the ability to flexibly portray quantum calculations than any other circuit [7]. The extraction of the circuits is also a direct procedure, where spiders are unfused and replaced with Clifford gates and CZ gates on the inputs and outputs as per requirement. These are not just mere flexible circuits but contain rich equational theory: the ZX-calculus and can be deformed arbitrarily. The core parameters of the ZX-calculus give a thorough theory for Clifford circuits, which can be efficiently classically simulated.

IV. RESULTS

To introduce the resistance to noise, in our integer multiplier circuit we have replaced the Toffoli gate with Clifford + T gate architecture. The circuit is then converted into a quantum gate using Python commands. The quantum gate is appended to the multiplier code replacing the Toffoli gate thereby making the circuit fault tolerant. The multiplier circuit using the Clifford gate is shown in Figure (15). To perform the ZX calculus, we import an open-source Python library called "PyZX" in jupyter notebook. Firstly, we change the multiplier code into QASM code and transform it into basic quantum gates. The next step is to identify the gates present in the non-optimized multiplier circuit, followed by the conversion into a graph. The graph-like state is a crucial step before simplifying as it allows the optimization to result in a minimum number of internal spiders. The final step is the extraction of the optimized circuit and printing of the gates present in the circuit after optimization. In the end, we have verified the functionality of the circuit. For measuring the cost-effectiveness of our resultant optimized circuit, we perform a cost analysis in which T-gate count and ancilla inputs are the primary factors considered, the results of which have been tabulated in Table 1. The T gate count reduced from 742 to 488 after optimization which is shown in Fig 16.

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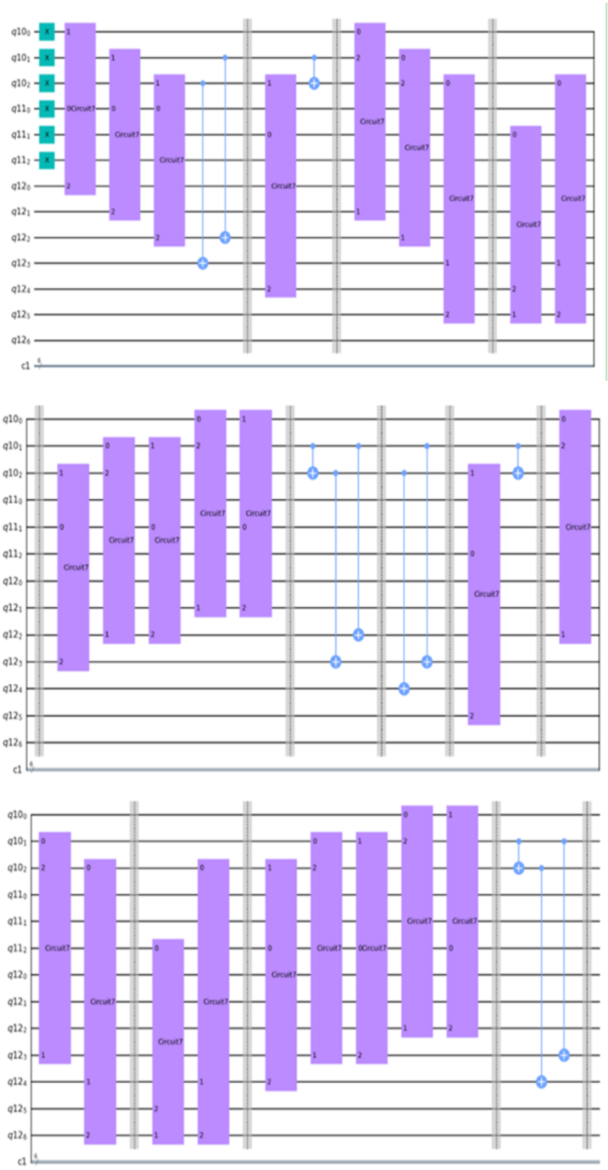

Fig. 15: Integer Multiplier Circuit

Table- I: Comparison of Multiplier Circuit Before and after Optimization for 6-Bit Multiplier

Features	Before Optimization	After Optimization
Number Of Qubits	25	25
Number of Gates	1786	2416
T-gate count	742	488
Clifford Gate count	1044	2328

The Clifford gate count increases from 1044 to 2328. Where n is the number of bits for which the adder is designed, in a conditional adder circuit, the T gate count is given by 21n + 14, and the Toffoli gate array uses 7n T- gates. This brings the total T-count to

$$21n^2 - 14 \quad (8)$$

The total ancilla inputs used in the design are given by

$$2n + 1 \quad (9)$$

For a 6-qubit circuit design, the T count is 742, with an ancilla count of 13.

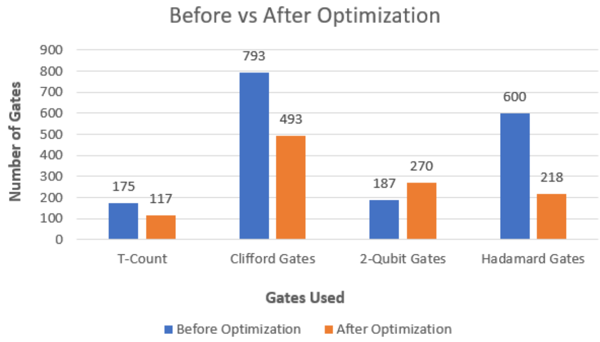

Fig. 16: Optimization Results

V. CONCLUSION

In order to introduce the resistance to noise, in our integer multiplier circuit we have replaced the Toffoli gate with Clifford + T gate architecture. The circuit is then converted into a quantum gate using Python commands In this work, a new method of optimizing quantum arithmetic circuits using ZX calculus is introduced. In particular, the fault-tolerant implementations of these circuits are considered and the trade-offs required with regard to the hardware cost are minimized by the use of this method. For the fault-tolerant implementation of the 6-qubit multiplier circuit, the optimization resulted in a 34% reduction in the T-gate count with a trade-off of an increase in the Clifford gate count. The T-gate count is reduced when compared with the previous designs without any increase in the number of qubits which yielded an overall cost reduction for the hardware implementation of the circuit.

DECALARION STATEMENT

Funding	No, I did not receive.
Conflicts of Interest	No conflicts of interest to the best of our knowledge.
Ethical Approval and Consent to Participate	No, the article does not require ethical approval and consent to participate with evidence.
Availability of Data and Material/ Data Access Statement	Not relevant.
Authors Contributions	Reena Monica P conceived the idea, proposed, and reviewed the work. Aravind Joshi, Akshara Kairali, Renju Raju and Adithya Athreya carried out the work and documented the initial draft. Adithya Athreya perfected the manuscript based on the reviewers' comments.

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