



Comparative Analysis of PWM and Neural Network-Based Modulation Techniques for a 5-Level CHB Inverter

Amrita Baruah, Aditya Bihar Kandali, Pankaj Borah

Abstract: This paper compares the performance of conventional Pulse Width Modulation (PWM) with an optimised Neural Network (NN)-based modulation strategy for inverter control. Although PWM remains one of the most widely used modulation techniques because of its simplicity and reliability, its performance is inherently limited by fixed linear switching schemes. An NN-based controller offers a different approach by learning switching patterns from the system, enabling better overall performance. To investigate this, we developed and evaluated both modulation methods in the MATLAB/Simulink environment under identical nominal operating conditions. The results indicate that the proposed NN-based controller provides a higher output RMS voltage, improved output waveform quality and lower Total Harmonic Distortion (THD) than conventional PWM. Together, these improvements lead to a cleaner output waveform and more effective use of the available DC source, without requiring any hardware modifications. The present study is limited to simulation and does not account for practical hardware non-idealities. Even so, the results suggest that the neural network's learning capability can improve performance under nonlinear operating conditions. Future work will focus on real-time implementation using DSP/FPGA platforms, further optimisation of the learning algorithm, and exploring hybrid modulation techniques for multilevel inverters.

Keywords: 5-level Multilevel Inverter, Pulse Width Modulation, Neural Network, THD, RMS Voltage

Nomenclature:

NN: Neural Network
THD: Total Harmonic Distortion
PWM: Pulse Width Modulation
CHB: Cascaded H-bridge
ANNs: Artificial neural networks
MLI: Multilevel inverter
MSE: Mean squared error
FFT: Fast Fourier Transform
RMS: Root Mean Square

Manuscript received on 17 July 2026 | First Revised Manuscript received on 23 July 2026 | Second Revised Manuscript received on 08 August 2026 | Manuscript Accepted on 15 August 2026 | Manuscript published on 30 August 2026.

*Correspondence Author(s)

Amrita Baruah*, Department of Electrical Engineering, Jorhat Engineering College, Dibrugarh (Assam), India. Email ID: amritabaruah624@gmail.com, ORCID ID: 0009-0008-5643-3629

Dr. Aditya Bihar Kandali, Professor, Department of Electrical Engineering at Jorhat Engineering College, Dibrugarh (Assam), India. Email ID: abkandali@gmail.com

Dr. Pankaj Borah, Assistant Professor, Department of Power Electronics and Instrumentation Engineering at Jorhat Institute of Science and Technology, Dibrugarh (Assam), India. Email ID: pankajofcit@gmail.com

@ The Authors. Published by Blue Eyes Intelligence Engineering and Sciences Publication (BEIESP). This is an open-access article under the CC-BY-NC-ND license (<http://creativecommons.org/licenses/by-nc-nd/4.0/>)

I. INTRODUCTION

Multilevel inverters have become an essential technology in modern power electronics because they deliver better voltage waveform quality, reduced harmonic distortion, and higher efficiency than conventional two-level inverters [1]. Among the classical topologies, the cascaded H-bridge (CHB) inverter is especially attractive, as its modular structure and flexibility make it a common choice in high-power applications such as flexible AC transmission systems. The topology is built by connecting several H-bridge modules in series, each capable of generating +Vdc, -Vdc, and zero, giving it a modular, scalable character that suits high-voltage operation well [2]. When two such cells are cascaded, a five-level output voltage is synthesised, and this waveform lies considerably closer to a sine wave while carrying less total harmonic distortion than the output of a single H-bridge inverter [6].

The quality of the inverter output depends largely on the modulation technique employed. Among the commonly used high-frequency modulation methods, carrier-based pulse width modulation (PWM) is widely adopted because of its relatively simple implementation and control [3]. Despite the advantages of multilevel topologies and PWM techniques, harmonic distortion remains an important concern in power electronic converters. Total harmonic distortion (THD) is therefore commonly used to evaluate the harmonic content and overall quality of the output waveform [9]. Conventional two-level inverters, in particular, suffer from high THD, increased switching stress, and limitations in high-voltage applications; multilevel designs aim to overcome these shortcomings [5].

To achieve better harmonic performance than conventional PWM techniques, researchers have increasingly turned to intelligent control strategies. Among them, artificial neural networks (ANNs) have shown considerable potential to tackle the control challenges related to multilevel inverters, especially for harmonic mitigation. The payoff is visible in the reported results: a neural-network-designed multilevel inverter has been demonstrated with a THD of about 2.75%, comfortably within the IEEE 5% limit [4]. Likewise, ANNs trained on the optimum switching angles derived from selective harmonic elimination have been used to curtail lower-order harmonics and THD in cascaded H-bridge inverters [7].

Based on these developments, both conventional PWM and ANN-based techniques provide useful approaches for controlling multilevel inverters and improving their output-voltage quality. In this work, a five-level cascaded H-



bridge multilevel inverter is investigated using conventional carrier-based PWM and ANN-based modulation. The performance of the two approaches is evaluated in terms of total harmonic distortion (THD) and RMS output voltage to determine the effectiveness of ANN-based modulation in improving the power quality of the five-level CHB inverter.

II. SYSTEM ARCHITECTURE

The proposed inverter is based on a five-level Cascaded H-Bridge (CHB) topology, one of the most commonly used multilevel inverter configurations because of its modular design and the high-quality output voltage it can produce. The framework produces a stepped AC output waveform by connecting the AC outputs of individual full-bridge power cells in series; two H-bridge cells in series produce the five output voltage levels [8]. Separate, symmetrical DC voltage sources feed the inverter, each maintaining an identical potential of $V_{dc} = 100V$. Each H-bridge consists of 4 IGBTs. By controlling the switching patterns of the complementary switch pairs in each bridge, the output voltage of an individual cell (V_{H1} or V_{H2}) can be set to one of the three discrete levels: $+V_{dc}$, 0 or $-V_{dc}$. Since the AC terminals of the cells are connected in series, the overall instantaneous output phase voltage is obtained as the algebraic sum of the voltages generated by each cell.

$$V_{out} = V_{H1} + V_{H2}$$

By coordinating the switching states across both H-bridges, the system combines these individual states to yield five discrete output levels: $+2V_{dc}$, $+V_{dc}$, 0, $-V_{dc}$, and $-2V_{dc}$.

A. Pulse Width Modulation

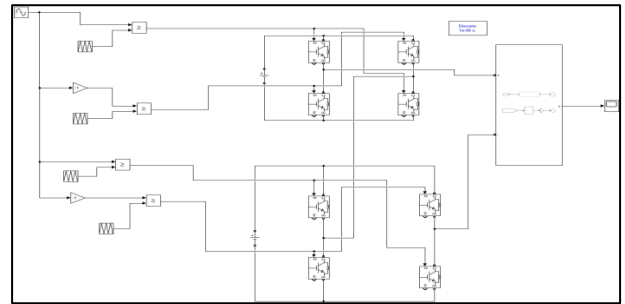
The Pulse Width Modulation (PWM) technique is used as the conventional modulation method for the proposed five-level multilevel inverter (MLI). In this work, a level-shifted carrier-based PWM scheme is selected to generate the switching pulses for the inverter switches. This method is fairly common in multilevel inverter applications because it

is easy to implement and gives satisfactory output performance without adding much complexity.

The modulation process is based on four synchronised triangular carrier waves: C1, C2, C3, and C4. These carrier signals have the same switching frequency and are vertically stacked from -2.0 to +2.0. C1 and C3 define the $+100V$ and $+200V$ bands, while C2 and C4 are inverted via a -1 gain to generate $-100V$ and $-200V$. This arrangement makes it possible to identify the voltage level that should be generated at any instant.

A sinusoidal reference signal then controls the switching process. For the proposed inverter, the reference wave has an amplitude of $A = 2.0$ and a fundamental frequency of 50 Hz. As the reference signal moves through the stacked carrier bands, it crosses different carriers at different instants. These crossing points, in a way, decide how the inverter switches should operate.

To generate the gate signals, the reference sine wave is continuously compared with each of the four carrier waves using relational logical comparators. Every comparison produces a logical output of either 1 or 0, depending on whether the reference signal is above or below the corresponding carrier. These logic signals are then combined according to the switching strategy to generate the final gate pulses for the IGBTs. As the switching sequence keeps changing throughout the cycle, the inverter produces the required five-level stepped output voltage, which closely follows the shape of a sinusoidal waveform.

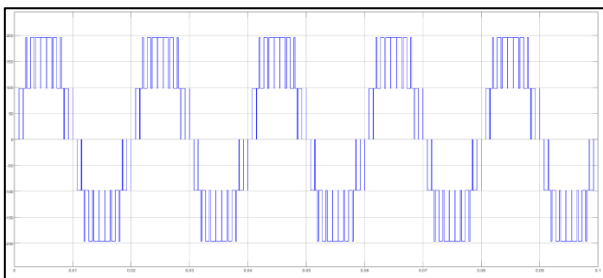


[Fig.1: Simulink Model of PWM-based 5-Level CHB Inverter]

Table I: Switching States of 5-Level CHB Inverter

Output Voltage	S1	S2	S3	S4	S5	S6	S7	S8
$+2V_{dc}$	ON	OFF	OFF	ON	ON	OFF	OFF	ON
$+V_{dc}$	ON	OFF	OFF	ON	OFF	ON	OFF	ON
0	OFF	ON	OFF	ON	OFF	ON	OFF	ON
$-V_{dc}$	OFF	ON	ON	OFF	OFF	ON	OFF	ON
$-2V_{dc}$	OFF	ON	ON	OFF	OFF	ON	ON	OFF

The PWM pulses are fed to the switch gates to produce a 5-level stepped output voltage waveform. The generated output waveform closely resembles a sinusoidal waveform.



[Fig.2: Output Voltage Waveform of PWM-Based 5-Level CHB Inverter]

B. Neural Network-Based Modulation

To improve power quality by reducing Total Harmonic Distortion (THD) while increasing the output RMS voltage, a multilayer feed-forward Artificial Neural Network (ANN) is proposed and evaluated against conventional PWM modulation. The ANN controller is designed to learn the relationship between a sinusoidal reference signal and the corresponding 8-bit switching states required to control the two cascaded H-bridge inverter cells. Unlike conventional PWM, which produces switching pulses by comparing a reference signal with carrier signals, the ANN learns the



switching pattern from training data.

The training dataset was generated in MATLAB using a 50 Hz sinusoidal reference waveform sampled over one complete cycle. A total of 1000 samples were created with the reference signal varying between -2 and $+2$. Based on predefined threshold values, each input sample was assigned an 8-bit switching vector representing the gate signals of the eight IGBTs in the CHB inverter.

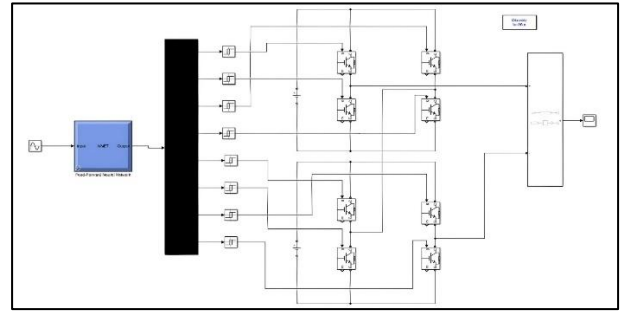
A feedforward neural network with one hidden layer consisting of 15 neurons was selected for the proposed modulation scheme. The network contains one input neuron representing the reference signal and eight output neurons corresponding to the inverter gate signals (S1–S8). The network was trained using the Levenberg–Marquardt backpropagation (trainlm) algorithm. During training, the dataset was automatically divided into 70% for training, 15% for validation, and 15% for testing, and the network weights were updated iteratively to minimise the mean squared error (MSE).

Table II: Parameters For Neural Network Training

Structural Parameter	Specification
Network Architecture	Feedforward Artificial Neural Network
Input Layer Nodes	1 Node (Reference sinusoidal signal, V_{ref})
Hidden Layer Configuration	1 Hidden Layer with 15 Neurons
Output Layer Nodes	8 Nodes (Gate signals S1-S8 for the eight IGBTs)
Training Algorithm	Levenberg-Marquardt backpropagation (trainlm)

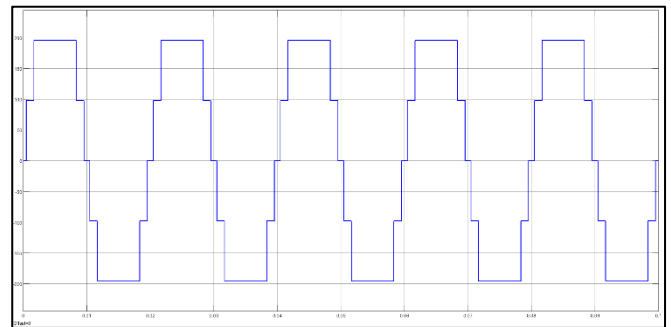
The trained ANN was evaluated using the training performance, regression analysis, and error histogram generated by the MATLAB Neural Network Toolbox. The network completed training after 58 epochs, with the best validation performance achieved at epoch 52. The regression results showed good agreement between the predicted outputs and the target switching states, while the error histogram indicated that most prediction errors were concentrated close to zero. These results confirm that the ANN learned the relationship between the reference signal and the required switching states and can generate reliable switching commands for the proposed inverter.

After training, the network was saved and integrated into the proposed CHB inverter model in MATLAB/Simulink. A continuous sinusoidal signal is applied to the network input, while the resulting 8-bit output vector is separated using a Demux block. Each output is then processed through relay blocks with hysteresis thresholds of 0.5 (turn-on) and 0.5 (turn-off). This hysteresis-based implementation converts the Demux's continuous outputs into binary signals, which drive the IGBT gates. The performance of the ANN-based modulation technique was then compared with the conventional PWM method in terms of Total Harmonic Distortion (THD) and RMS output voltage.



[Fig.3: Simulink Model of Neural Network-Based Multilevel Inverter]

The system Scope verifies that the network successfully synthesises a perfectly symmetrical 5-level staircase output voltage waveform operating between peak amplitudes of $+200\text{V}$ and -200V .



[Fig.4: Output Voltage Waveform of NN-based 5-level CHB Inverter]

III. SYSTEM CONTROL PARAMETERS AND SIMULATION SETUP

To evaluate the performance of the proposed Neural Network (NN)-based control strategy, a comparative analysis was carried out with the conventional carrier-based Pulse Width Modulation (PWM) technique. Both control methods were implemented under identical operating conditions using a 5-level Cascaded H-Bridge (CHB) inverter with a total DC-bus voltage of 200 V to ensure a fair comparison. The performance evaluation focuses on two key performance parameters: Total Harmonic Distortion (THD) and RMS output voltage. These parameters provide a reliable basis for assessing each control technique's effectiveness in output waveform quality and overall inverter performance. The results offer clear insight into the improvements achieved by the proposed NN-based approach, particularly in reducing harmonic distortion and improving RMS voltage.

A. Total Harmonic Distortion Profile

Total Harmonic Distortion (THD) is one of the most important parameters used to evaluate the quality of the output voltage produced by a multilevel inverter. It indicates how much the waveform deviates from an ideal sinusoidal wave due to the presence of harmonic components. In general, a lower THD value means better waveform

quality, improved power delivery, and lower harmonic losses, while higher THD can negatively affect the performance of electrical equipment.

In this work, the THD performance of the conventional PWM technique and the proposed Neural Network (NN)-based modulation method is compared using a 5-level Cascaded H-Bridge (CHB) inverter. The output voltage waveforms of both methods were analysed using the Fast Fourier Transform (FFT) tool available in the MATLAB/Simulink Power GUI environment. The corresponding harmonic spectra were then examined to evaluate the improvement in output power quality achieved by the proposed approach.

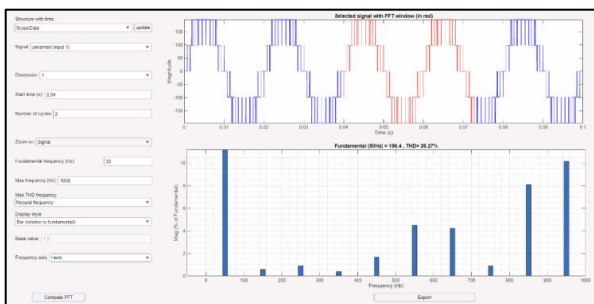
The Total Harmonic Distortion is calculated using the following expression:

$$THD \% = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots}}{V_1} \times 100$$

where V_1 is the RMS value of the fundamental voltage component, and $V_2, V_3, \dots, V_n$ represent the RMS values of the higher-order harmonic components.

▪ Spectral Analysis and Harmonic Profile under Conventional PWM

The baseline system uses a conventional carrier-based PWM technique for controlling the multilevel inverter. To ensure a fair comparison, the same operating conditions were maintained throughout the analysis. The inverter was operated at a fundamental frequency of 50 Hz, while the FFT analysis was started at 0.04 s to avoid the initial transient response. The harmonic spectrum was then calculated over two cycles of the fundamental waveform.



[Fig.5: FFT Harmonic Spectrum and THD of the Output Phase Voltage Under PWM Control]

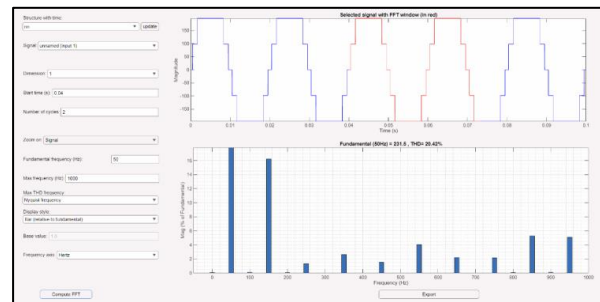
Under these specific modulation constraints, the 5-level Cascaded H-Bridge (CHB) inverter yields a fundamental peak voltage magnitude ($V_{1, \text{peak}}$) of 196.4V and a total harmonic distortion (THD) of 26.27%.

The spectral distribution reveals significant harmonic distortion concentrated within the high-frequency range of 500–1000 Hz. Furthermore, the persistence of lower-order harmonics further reflects the limitations of conventional carrier-based modulation, motivating the development of advanced optimisation techniques for improved harmonic suppression.

▪ Spectral Analysis and Harmonic Profile under Neural Network Control

To analyse the power quality of the neural network-driven cascaded multilevel inverter, a Fast Fourier Transform (FFT) analysis is conducted using the Power GUI environmental tool. The start time (0.04 seconds), fundamental frequency (50Hz), and analysed cycle count of 2 are kept identical to the PWM-modulated inverter to ensure a direct comparison.

The spectrum evaluation shows that the network-driven system delivers a fundamental peak voltage component of 231.5V. Without external filters connected to the power stage, the raw, unfiltered line output voltage yields a Total Harmonic Distortion (THD) of 20.42%.



[Fig.6: FFT Harmonic Spectrum and THD of the Output Phase Voltage Under NN Control]

The spectrum shows that the distortion is mainly concentrated at lower frequencies. The remaining higher-order harmonics are greatly reduced and contribute only minor distortions. Small traces of high-frequency harmonics still appear because of the abrupt voltage step changes in the waveform.

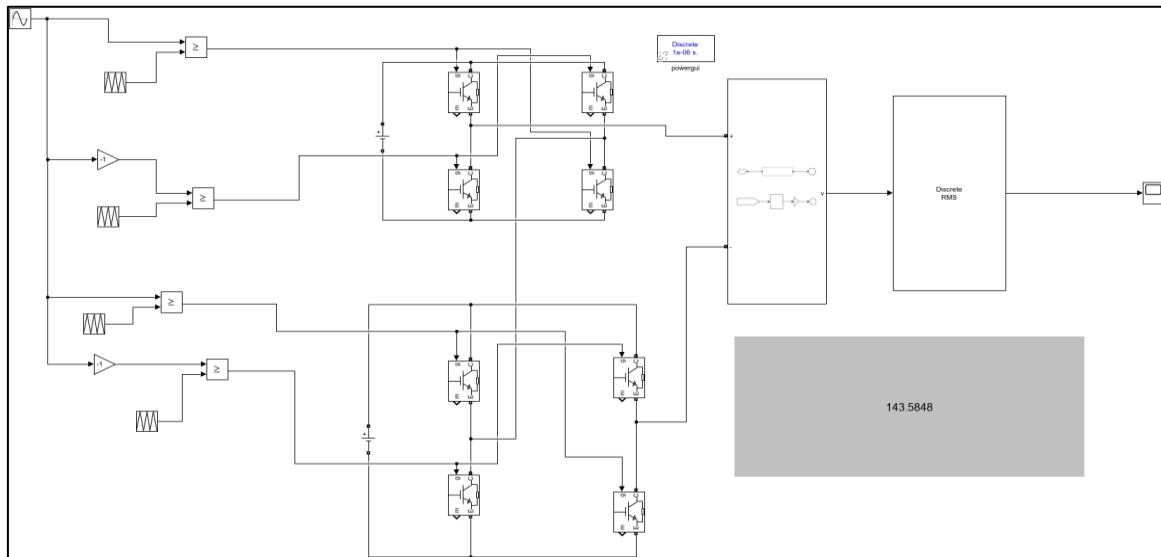
B. RMS Output Voltage Analysis

In addition to harmonic reduction, the control method's ability to maximise root mean square voltage is a crucial performance metric. The Root Mean Square (RMS) output voltage evaluates the voltage quality and power delivery capability of a multilevel inverter. The modulation strategy, switching pattern, and the inverter's voltage synthesis capability influence the RMS voltage. Generally, a higher RMS voltage indicates better use of the available DC bus voltage and stronger power transfer capacity.

The fundamental Root Mean Square (RMS) voltage was monitored using a Discrete RMS block operating at a fundamental frequency of 50Hz. To ensure accurate documentation of the RMS measurement, a Display block was used to extract and record the RMS output voltage at the simulation stop time of 0.1 seconds.

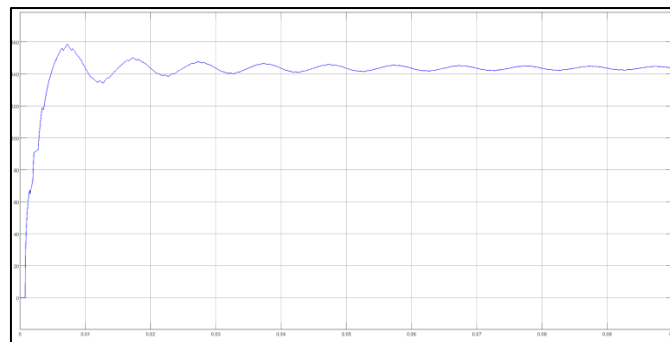
▪ RMS Tracking under Conventional PWM Regulation

Under conventional carrier-based PWM control, the output fundamental voltage reaches a stable steady-state value of 143.5848V. The fundamental amplitude remains constrained by the fixed intersections of the carrier waveforms, limiting the maximum attainable voltage output.



[Fig.7: Simulink Implementation of the Discrete RMS Measurement Under PWM Control]

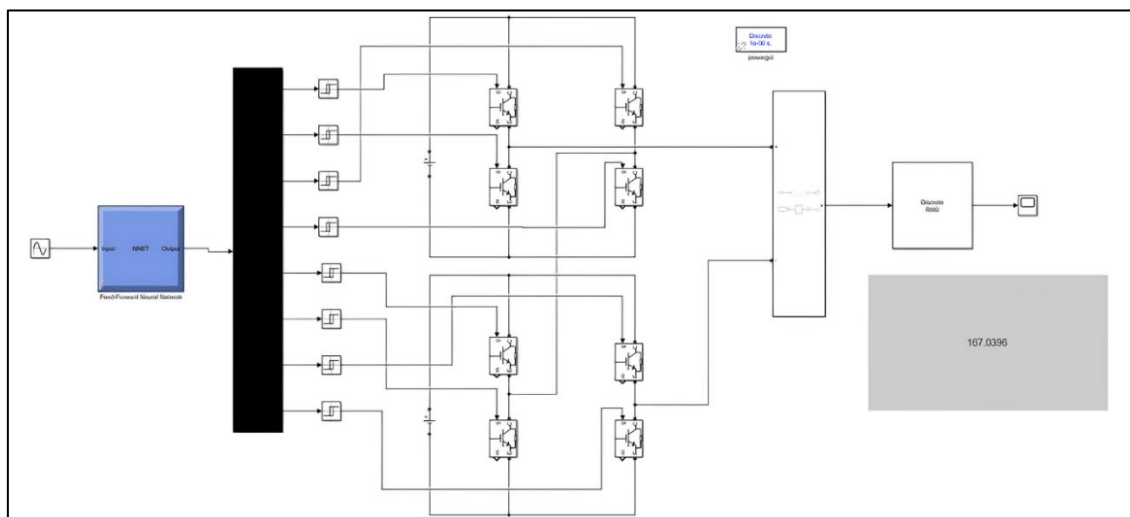
The following figure illustrates the RMS voltage waveform obtained during the simulation. The waveform shows the variation of the RMS voltage with time and its progression towards a steady-state value.



[Fig.8: Steady-State RMS Output Voltage Waveform Under PWM Control]

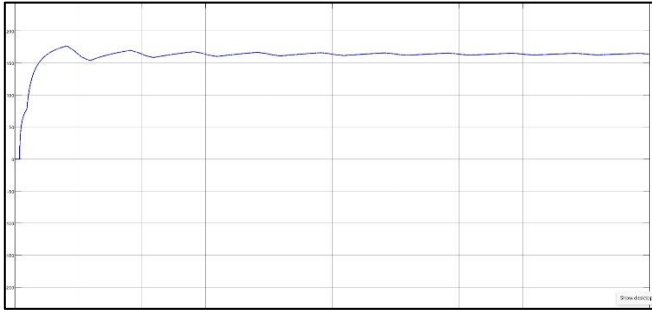
▪ RMS Tracking under Proposed Neural Network Regulation

The RMS value of the fundamental output voltage is determined in real time through a Discrete RMS measurement block that tracks the synthesised staircase waveform. Under steady operating conditions, the neural network-based controller produces a stable RMS output voltage of **167.0396V**, as verified by the system display block.



[Fig.9: Simulink Implementation of the Discrete RMS Measurement Under NN Control]

The transient response of the calculated RMS voltage waveform shows an exceptionally fast and stable settling profile over the simulation time.



[Fig.10: Steady-State RMS Output Voltage Waveform Under NN Control]

At startup, the voltage increases smoothly with a short rise time and reaches its steady-state value with minimal overshoot. The lack of heavy oscillations or severe voltage dipping confirms that the neural network maintains reliable, consistent switching behaviour and consistent performance across successive fundamental cycles.

IV. RESULTS AND PERFORMANCE COMPARISON

This section presents a comprehensive evaluation and comparison of the two control strategies applied to the 5-level CHB inverter. Performance is evaluated through certain quantitative metrics obtained from the Simulink simulation environment. A direct performance comparison is established to evaluate the percentage improvement in voltage quality and overall system efficiency.

A. Performance Parameters

i. Total Harmonic Distortion

THD of PWM modulation = 26.27%

THD of NN modulation = 20.42%

Based on the FFT results, the THD obtained with the conventional PWM technique was 26.27%. When the proposed ANN-based modulation was applied, the THD decreased to 20.42%, giving an improvement of about 22.27%. This reduction indicates that the ANN selected switching states more effectively than the conventional approach. As a result, fewer harmonic components were present in the output voltage, making the waveform closer to a sinusoidal shape. These findings suggest that the proposed controller can improve the output power quality of the 5-level Cascaded H-Bridge inverter while providing better harmonic performance than the conventional PWM method.

ii. Output RMS Voltage

V_{rms} of PWM modulation = 143.5848V

V_{rms} of NN modulation = 167.0396V

The conventional PWM method produced an RMS voltage of 143.5848 V, whereas the ANN-based modulation achieved 167.0396 V, representing an approximate 16.3% improvement in RMS output voltage. The higher RMS value obtained with the ANN indicates improved effective output voltage, suggesting

that the proposed modulation technique utilises the inverter output more effectively while maintaining better waveform quality.

B. Robustness and Dynamic Performance Discussion

The robustness of the proposed NN-based modulation technique was evaluated under two disturbed operating conditions: DC-link voltage imbalance and additive band-limited white noise. The analysis used THD to compare the responses of the conventional PWM and NN-based modulation techniques.

For the DC-link voltage imbalance, 10% and 20% imbalance conditions were considered. The NN-based technique resulted in THD values of 20.91% and 21.56%, respectively, while PWM produced 31.79% and 30.71%. Under the noise test, noise power levels of 2×10^{-8} and 5×10^{-8} were applied. The corresponding THD values were 21.86% and 23.89% for the NN-based method, compared with 34.67% and 36.56% for PWM. The results show that the NN-based modulation maintained lower THD under all the tested disturbance conditions.

Table III: Robustness Test Results

Test Condition	PWM THD (%)	ANN THD (%)
10% DC imbalance	31.79	20.91
20% DC imbalance	30.71	21.56
Noise: $2e-8$	34.67	21.86
Noise: $5e-8$	36.56	23.89

V. LIMITATIONS OF THE STUDY

Although the proposed neural network-based modulation scheme shows promising performance improvements, some limitations should be considered when interpreting the results:

- Lack of experimental hardware validation: The proposed method is validated only through MATLAB/Simulink simulations, and experimental hardware verification has not been performed.
- Limited operating conditions: The performance evaluation is limited to selected operating conditions, while its robustness under wider voltage and parameter variations remains to be investigated.
- Embedded implementation not evaluated: The computational complexity, memory requirements, and execution time of the neural network for real-time DSP or FPGA implementation have not been evaluated.

VI. FUTURE SCOPE

To build on these findings, future research can prioritise implementing and experimentally validating the neural network strategy on real-time hardware platforms such as DSPs or FPGAs to confirm its practical feasibility. Further investigations can include comprehensive robustness analysis under varying operating conditions such as wider DC-link voltage imbalance, parameter uncertainties and dynamic modulation amplitudes. Alongside these physical tests, the neural network architecture itself can be optimised to minimise computational complexity and memory usage for efficient embedded execution. Additionally,



hybrid modulation approaches combining conventional PWM techniques with intelligent control methods may be developed to further enhance inverter performance in terms of efficiency, harmonic reduction, and dynamic response.

VII. CONCLUSION

This study successfully evaluated and compared the performance of an optimised Neural Network (NN)-based modulation technique with the conventional Pulse Width Modulation (PWM) method using a MATLAB/Simulink simulation environment. The performance of both techniques was assessed based on Total Harmonic Distortion (THD) and RMS output voltage.

The simulation results show that the proposed NN-based modulation technique improves the inverter's overall output performance. The NN controller produced a higher RMS output voltage while reducing Total Harmonic Distortion (THD). A lower THD indicates that the output voltage waveform is closer to a pure sinusoidal wave, improving power quality. The increase in RMS voltage shows that the inverter output is being utilised more effectively. The robustness analysis also demonstrated that the NN-based method maintained lower THD under both DC-link voltage imbalance and additive noise. Overall, the results indicate that the proposed NN-based modulation technique provides improved output waveform quality and better harmonic performance under the tested operating conditions.

ACKNOWLEDGEMENT

The author expresses sincere gratitude to Dr Aditya Bihar Kandali, Professor, Department of Electrical Engineering, Jorhat Engineering College and Dr Pankaj Borah, Assistant Professor, Department of Power Electronics and Instrumentation, Jorhat Institute of Science and Technology, for their invaluable guidance, enduring support, and intellectual mentorship throughout this research.

Appreciation is also extended to the Department of Electrical Engineering, Jorhat Engineering College, for providing the essential computational resources and infrastructure that made this work possible.

DECLARATION STATEMENT

After aggregating input from all authors, I must verify the accuracy of the following information as the article's author.

- **Conflicts of interest:** Based on my understanding, this article has no conflicts of interest.
- **Funding/Grants/Financial Support:** This article has not been sponsored or funded by any organisation or agency.
- **Ethical Approval and Consent to Participate:** The data provided in this article are exempt from ethical approval or participant consent requirements.
- **Data Access Statement and Material Availability:** The adequate resources of this article are publicly accessible.
- **Author's Contribution:** The authorship of this article is contributed equally to all participating individuals.

REFERENCES

1. T. A. Taha, M. Shalaby, N. I. A. Wahab, H. I. Zaynal, M. K. Hassan, S. Al-Sowayan and M. A. Alawad. "Recent Advancements in Multilevel Inverters: Topologies, Modulation Techniques, and Emerging Applications". *Symmetry* 2025, 17, 1010. DOI: [10.3390/sym17071010](https://doi.org/10.3390/sym17071010)
2. N. Subramanian and A. A. Stonier. "An Extensive Investigation on Intelligent-Based Control Techniques for the Performance Improvement in Multilevel Inverters". *IEEE Access*, 2025, vol. 13. DOI: [10.1109/ACCESS.2025.3576380](https://doi.org/10.1109/ACCESS.2025.3576380)
3. K. N. D. V. S. Eswar, M. A. N. Doss, P. Vishnuram, A. Selim, M. Bajaj, H. Kotb, and S. Kamel. "Comprehensive Study on Reduced DC Source Count: Multilevel Inverters and Its Design Topologies". *Energies* 2023, 16(1), 18. DOI: [10.3390/en16010018](https://doi.org/10.3390/en16010018)
4. R. Venkadesh, Dr R. Anandha Kumar and Dr G. Renukadevi. "A Neural Network-Designed Multilevel Inverter with Reduced Switches and THD". *International Journal of Engineering Research & Technology (IJERT)*, Vol. 13, Issue 10, October 2024. DOI: [10.5281/zenodo.18130946](https://doi.org/10.5281/zenodo.18130946)
5. C. Savitri and Prof. C. Jambhulkar. "Development of Artificial Intelligence Based Multilevel Inverter Using MATLAB/Simulink". *International Journal of Novel Research and Development (IJNRD)*, vol. 8, Issue 9, September 2023. URL: <https://ijnrd.org/papers/IJNRD2309299.pdf>
6. X. Fu, S. Li, A. Al Hadi, and R. Chaloo. "Novel Neural Control of Single-Phase Grid-Tied Multilevel Inverters for Better Harmonics Reduction". *Electronics* 2018, 7(7), 111. DOI: [10.3390/electronics7070111](https://doi.org/10.3390/electronics7070111)
7. S. Padmanaban, C. Dhananjayulu and B. Khan. "Artificial Neural Network and Newton Raphson (ANN-NR) Algorithm Based Selective Harmonic Elimination in Cascaded Multilevel Inverter for PV Applications". *IEEE Access*, 2021, vol. 9. DOI: [10.1109/ACCESS.2021.3081460](https://doi.org/10.1109/ACCESS.2021.3081460)
8. B. Sharma, S. Manna, V. Saxena, P. K. Raghuvanshi, M. H. Alsharif and Mun-Kyeom Kim. "A comprehensive review of multi-level inverters, modulation, and control for grid-interfaced solar PV systems". *Scientific Reports* 15, Article number: 661 (2025). DOI: [10.1038/s41598-024-84296-1](https://doi.org/10.1038/s41598-024-84296-1)
9. M. Mathews, B. Ramesh, Dr T. Sreedhar. "Minimization of THD in Nine Level Cascaded H- Bridge Inverter Using Artificial Neural Network". *International Journal of Innovative Works in Engineering and Technology (IJWET)*. Vol. 4, No. 1, Feb 2018. DOI: [10.48550/arXiv.2205.13366](https://doi.org/10.48550/arXiv.2205.13366)

AUTHOR'S PROFILE



Amrita Baruah received a B. Tech degree in Power Electronics and Instrumentation Engineering. She is currently pursuing the M. Tech degree in Electrical Engineering at Jorhat Engineering College, Assam, India. Her areas of interest include power electronics, instrumentation and control.



Dr. Aditya Bihar Kandali is a Professor in the Department of Electrical Engineering at Jorhat Engineering College, Assam, India. He received the PhD degree from the Indian Institute of Technology, Kharagpur. He has made major research contributions in pattern recognition, machine learning, and neural networks.



Dr. Pankaj Borah is an Assistant Professor in the Department of Power Electronics and Instrumentation Engineering at Jorhat Institute of Science and Technology, Assam, India. He received the PhD degree from Tezpur University, Assam, India. His work includes major contributions to advanced research in power electronics and solar photovoltaic (PV) systems.

Disclaimer/Publisher's Note: The statements, opinions, and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of the Publisher /Journal and/or the editor(s). The Publisher /Journal and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions, or products referred to in the content.

