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Design of Power Efficient divide by 2/3 Counter using E-TSPC based Flip Flops

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Abstract*: *High speed and low power are two major challenges for modern communication circuit designs. A frequency divider is a good example that requires balance between the two sides. An extended true-single-phase-clock (E-TSPC) based divide-by-2/3 counter design is proposed in this paper which can be used for low supply voltage and low power consumption applications. By using a wired OR scheme only one transistor is needed to implement both the counting logic and the mode selection control. This can enhance the working frequency of the counter due to a reduced critical path between the E-TSPC flip flops.

Keywords; D flip-flop (DFF), frequency divider, frequency synthesizer, Extended TSPC

I. INTRODUCTION

The high-speed frequency divider is a key block in frequency synthesis. The prescaler is the most challenging part in the high-speed frequency-divider design because it operates at the highest input frequency. True-single-phase-clock (TSPC) dividers are well known for their low power consumption comparing to the current mode logic (CML) implementation, but their application is limited to relatively low frequencies. With the development of CMOS Technologies, the improvement of the intrinsic speed of a device make it possible for the TSPC logic gates to replace CML even in high frequency applications. The prescaler is a synchronous circuit which is formed by D flip-flops and additional logic gates.

Due to the incorporation of additional logic gates between the flip-flops to achieve the two different division ratios, the speed of the prescaler is affected and the switching power increases.

Conventional high speed FF based divide-by counter designs use current-mode logic (CML) latches and suffers with large load capacitance. This not only limits the maximum operating frequency and current-drive capabilities, also increases the total power consumption. Alternatively, FF based divide-by designs adopt dynamic logic FFs such as true-single-phase clock (TSPC). The designs can be further enhanced by using extended true-single-phase-clock (E-TSPC) FFs for high speed and low power applications. E-TSPC designs remove the transistor stacked structure so that all the transistors are free of the body effect. They are thus more sustainable for high operating frequency operations with low voltage supply.

Previous optimization efforts on prescaler designs focused on simplifying the logic part to reduce the circuit complexity and the critical path delay. For example, an E-TSPC design embedded with one extra pMOS/nMOS transistor can form an integrated function of FF and AND/OR logic. Moving part of the control logic to the first FF to reduce unnecessary FF toggling yields another version of prescaler design. These two classic designs each contains 16 transistors only and the mode control logic uses as few as 4 transistors. To achieve such circuit simplicity, it calls for a ratioed structure in the FF design. Despite its distinct speed performance, the incurred static and short circuit power consumptions are significant.

Due to the quadratic dependence of power consumption on supply voltage, lowering is a very effective measure to reduce the power at the expense of speed performance. In this design, ratioed E-TSPC FFs are employed due to its circuit simplicity and speed performance. Only one pass transistor is needed to implement the mode control logic.

II. EXISTING E-TSPC 2/3 PRESCALER DESIGNS

The E-TSPC divide-by-2 unit has the merit of high operating frequency compared with the traditional TSPC divide-by 2 unit. Since thedivide-by-2/3 unit consists of two toggle DFFs and additional logic gates, one way to effectively reduce the delay and power consumption is to integrate the logic gates to the divide-by-2/3 unit.

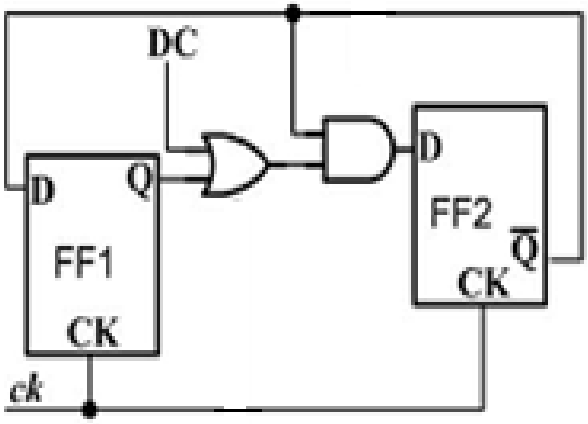

Fig.1. E-TSPC divide by 2/3 counter using AND-OR logic

Divide-by-2/3 counter design is given in Fig. 1(a) consists of two E-TSPC-based FFs and two logic gates, an OR gate and an AND gate.

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When the divide control signal is “0”, the OR gate (merged into output of FF1 stage) is disabled. This corresponds to a divide-by-3 function. Note that state 10 is a forbidden state. If, somehow, the circuit enters this state, the next state will go back to a valid state, 11, automatically. When “1” is the output of FF1 will be disabled and FF2 alone performs divide-by-2 function. Since the input toFF1 is not disabled, FF1 toggles as usual and causes redundant power consumption in the divide-by-2 mode operation.

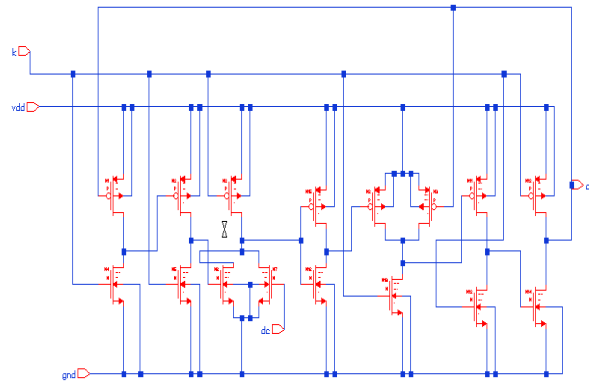

Fig.2. MOS Schematic of AND-OR logic divide by 2/3 counter

To overcome this problem, another divide-by-2/3 counter design presented in is shown in Fig. 2. By pushing the divide control logic from the output of FF1 to its input, the output of the first stage inFF1 is frozen when during divide by-2 This refrains the following stages from many switching activities for the purpose of power saving.

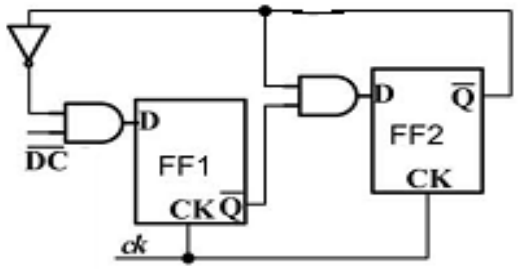

Fig.3. E-TSPC divide by 2/3 counter using pushed control

To reduce the unnecessary power consumption, a new divide-by-2/3 unit, which can effectively block the switching activities and the short circuit, is proposed as shown in Fig.3. Different from the previous method in this topology, two AND gates are used instead of one OR gate and one AND gate, to achieve a symmetrical architecture. By changing the *DCB*-controlled nMOS at the output of DFF1 to a controlled PMOS, DFF1 is blocked at the input when *DCB* is high. As a result, nodes *S*1, *S*2, and *S*3 of DFF1, which have the logical

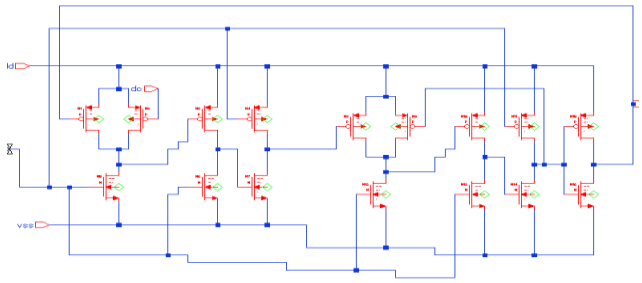

Fig.4. MOS Schematic of pushed contol logic divide by 2/3 counter

values of “1,” “0,” and “1,” respectively, are blocked. DFF1 only has the short-circuit path in the first stage, while the following stages have no switching activities or short circuits while DFF2 functions as a toggled divide-by-2 unit. Hence, the proposed divide- by-2/3 unit has a significant power-consumption reduction in the divide-by-2 operation. Even for the divide-by-3 operation, due to the complementary logic type, the power consumption is also slightly reduced due to the reduction of short-circuit power consumption in DFF1.

As a result, the divide-by-2 unit dissipates more power even only if one toggled DFF is needed. Such a topology introduces unnecessary power consumption, which is a significant part of the total power consumption. Moreover, during a quarter of the period, the short-circuit power still exists in DFF1.

The prescaler proposed in this paper eliminates only the switching power in DFF1 during the divide-by-2 mode but does little to the short circuit power making the circuit not suitable for ultra-low power applications.

III. IMPROVED E-TSPC 2/3 PRESCALER

The logic structure of the proposed design is shown in Fig.2. The two FFs and the AND gate are common in previous designs. The OR gate for the divide control is replaced with a switch. Note that there is a negation bubble at one of the AND gate’s input. The output of FF1 is thus complemented before being fed to FF2. When the switch is open, the input from FF1 is disconnected and FF2 alone divides the clock frequency by 2.When the switch is close, similar to the design in, FF1and FF2 are linked to form a counter with three distinct states. Fig. 3

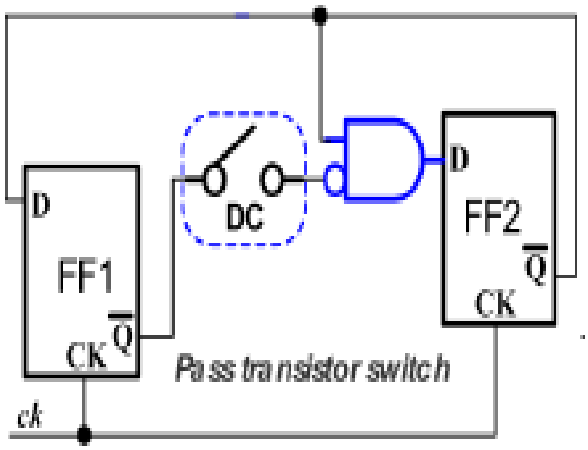

Fig.5. Logic structure of Proposed E-TSPC divide by 2/3 counter

Shows the circuit implementation. According to the simulation results given in, E-TSPC design shows the best speed performance in various counter designs including the one using conventional transmission gate FFs. Besides the speed advantage, E-TSPC FFs are particularly useful for low voltage operations because of the minimum height in transistor stacking. Other than the two E-TSPC FFs, only one pMos transistor is needed.

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The pMOS transistor controlled by the divide control signal serves as the switch. The AND gate plus its input inverter are achieved by way of wired-AND logic using no extra transistors at all.

The proposed design scheme is far more sophisticated than the measure of simply adding one pass transistor may suggest. First of all, unlike any previous designs, the E-TSPC FF design remains intact without any logic embedding. Both speed and power behaviors are not affected, which indicates a performance edge over the logic embedded FF design.

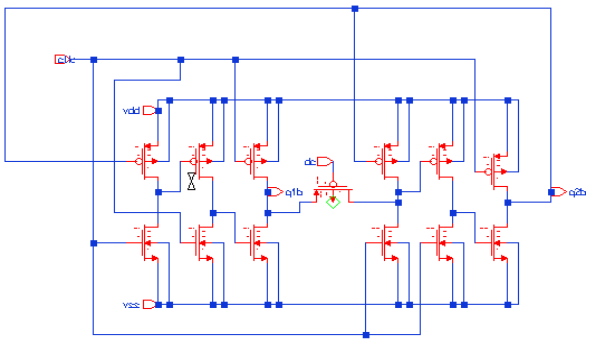

Fig.6. MOS schematic of proposed divide by 2/3 counter

The working principle of the proposed design is elaborated as follows. When is "1", the pMOS transistor is turned off as a switch should behave. A single pMOS transistor, however, presents a smaller capacitive load to FF1 than an inverter does in design. When is "0", the output of FF1, , is tied with the output node of the 1st stage inverter of FF2 through the pMOS transistor. In an E-TSPC FF design, the output of the first stage inverter can be regarded complementary to the input, Therefore, a wired-OR logic is in fact implemented. Either being "0" or being "1" pulls the output node of the inverter

IV. SIMULATION RESULTS AND PERFORMANCE COMPARISONS

Post-layout simulations in MENTOR GRAPHICS are conducted to compare the performances between the proposed design and the two divide-by-2/3 counter designs which are considered two of the best prior arts.

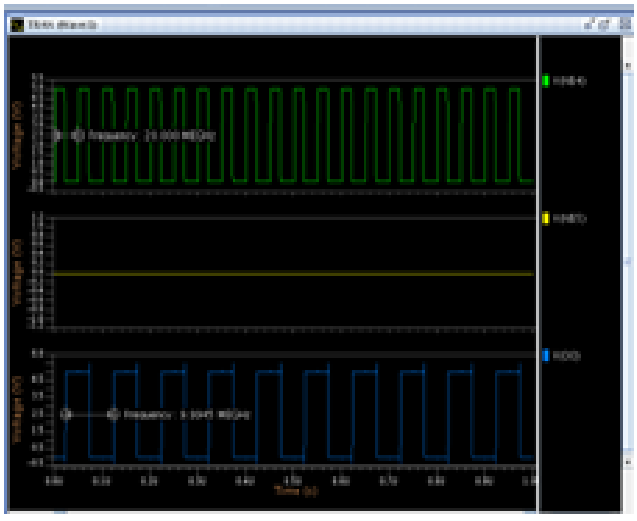

Fig.7. output waveform of divide by 2 operation for a given clock frequency 20MHZ

Since the same type of E-TSPC FF is used in all three designs, any performance discrepancy would come from the logic structure However, Designs in and are excluded as their stacked logic structures significantly degrade their speed performance when working in the territory of low.

Table 1. Performance Comparison

2/3 counter	AND-OR	PUSHED CONTROL	PROPOSED
Transistor count	21	19	16
Max.Frequncy (f/2 & f/3) (MHZ)	470/449	460/455	512/492
Average Power(mW)	2.0762	1.465	0.6332
delay(nS)	33.5	29.35	23.905
Power-Delay product(MJ)	0.6955	0.4299	0.1514
Jitter(pS)	12.1	9.6	7.05

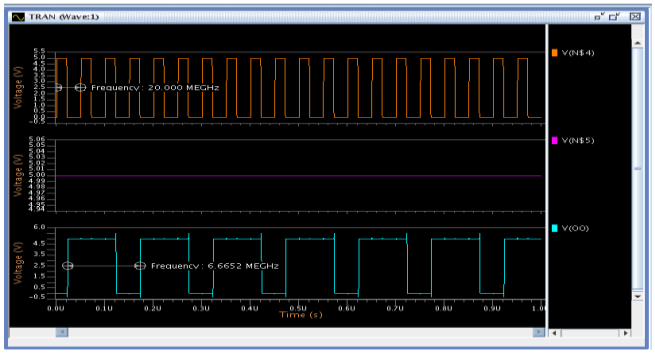

Fig.8. output waveform of divide by 3 operation for a given clock frequency 20MHZ

Table I summarizes the design features of these divide-by-2/3 counter designs at 0.6 V supply voltage. The two numbers separated by a slash in the "transistor count" indicate the number of transistors needed for the entire circuit versus that needed for the extra logic gates.

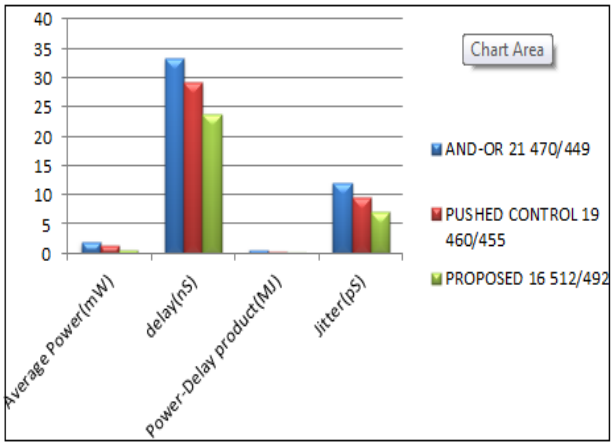

Fig.9. performance comparison chart

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IV. CONCLUSION

A modified divide by 2/3 counter architecture employing E-TSPC D flip-flop is proposed and presented. The D flip-flop requires only a single clock signal and uses a common-gate configuration for the bias transistors in addition to dynamic loading to increase its maximum operation frequency at low supply voltages. The proposed design successfully simplifies the control logic and one pMOS transistor alone serves the purposes of both mode select and counter excitation logic. The circuit simplicity leads to a shorter critical path and reduced power consumption. Post layout simulation results proved its advantages in power, speed, and layout area against previous designs.

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