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Performance Analysis of Different Topologies of 1-Bit Full Adder in UDSM Technology

J Samanta, A Patra, D Mishra, R Rashmi, I Kundu & R Koley

Abstract: ***Adders are key components in digital design, performing not only addition operations, but also many other functions such as subtraction, multiplication and division. Adders of various bit widths are frequently required in Very Large-Scale Integrated circuits (VLSI) from processors to Application Specific Integrated Circuits (ASICs). In this work, we have compared the performance of recently proposed topologies of 1-bit full adders in 150nm technology. We have compared ten different full adder topologies*** *like Standard* ***CMOS, CPL, Leap, LP, Mirror, TGdrivecap, 16Transistor, Conventional, Transmission Gate and 14Transistor full adder. The investigation has been carried out with EDA Tanner SPICE simulation tool. Performance has been also compared for variation of different supply voltage. The analysis has been done on the basis of propagation delay, power consumption and power delay product. The design guidelines have been derived to select the most suitable topology for the design features required.***

Index Terms: CMOS full adder, Propagation delay, PDP, Topology, UDSM

I. INTRODUCTION

UDSM (Ultra Deep Sub-Micron) Technology deals with MOS devices with channel length of the order of 0.25µm to 0.022µm or even less. This technology is also known as Nano Technology [13]. The increasing demand for low-power Very Large Scale Integration (VLSI) can be addressed at different design levels, such as the architectural, circuit, layout, and the process technology level [2]. At the circuit design level, considerable potential for power savings exists by means of proper choice of a logic style for implementing combinational circuits. Depending on the application, the kind of circuit to be implemented, and the design technique used, different performance aspects become important. In the past, the parameters like high speed, small area and low cost were the major areas of concern, whereas power considerations are now gaining the attention of the scientific community associated with VLSI design [1]. Addition is one of the important and commonly used arithmetic operations in many signal processing and other applications. So, an adder is one of the most critical components of a processor which determines its throughput, as it is used in the ALU, the floating-point unit, and for address generation in case of cache or memory access[3]. In this work ten different full adder topologies are compared in terms of propagation delay, power consumption and power delay product. Adder performances are measuring by varying the supply voltage.
The rest of the paper is organized as follows. In section II ten different full adder topologies are discussed. Simulation result is given in section III. In section IV the result analysis is discussed. The paper is concluded in section V.

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II. DESIGN OF DIFFERENT TOPOLOGIES OF FULL ADDER CIRCUITS

In this section 1-bit full adder are implemented using different styles. The inputs are the two bits to be summed and the carry bit, which derives from the calculations of the previous digits. The outputs are the result of the sum operation and the resulting value of the carry bit. The sum and carry output are given $S = A \oplus B \oplus C_i$

$C_o = AB + (A + B)C_i$

Where the and C_i is the input previous carry and C_o is the final carry out.

In this paper there are ten no. of topologies are implemented in Tanner EDA tool. These are explained in the next subsection.

2.1 CMOS full adder

In fig1 the CMOS full adder [7 & 12] is implemented by using standard CMOS logic. Total 28 no of transistor required for this configuration. The sum expression is given below.

S = ABCi +C₀ (A + B + C)

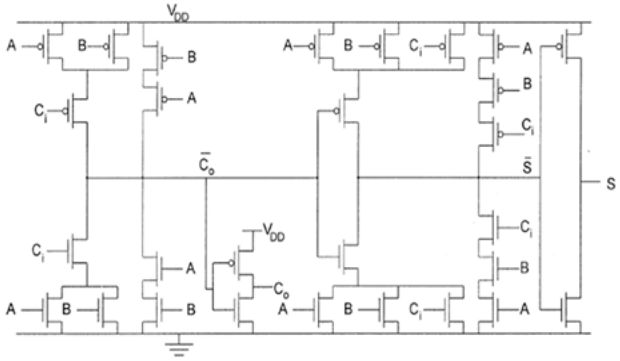

Fig1: Schematic view of the CMOS full adder

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2.2. CPL adder

The CPL full adder [1], shown in Fig.2 is made up of NMOS pass-transistors, and has differential inputs and outputs. Cross-coupled PMOS transistors are introduced to achieve the level restoring thus reducing short-circuit power consumption.

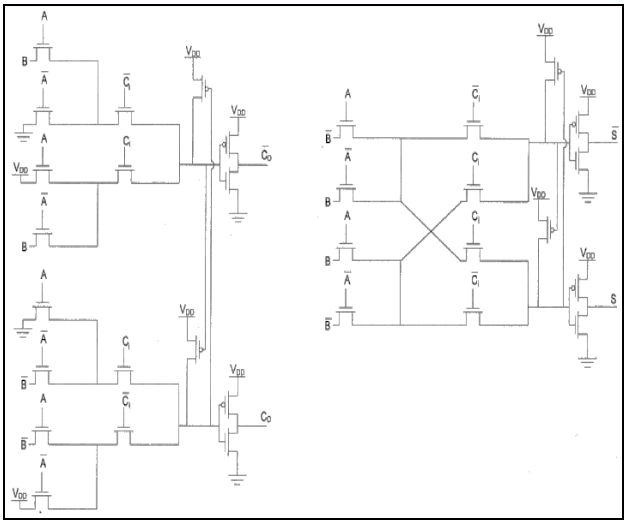

Fig2: Schematic view of the CPL full adder

2.3. LEAP full adder

The LEAP full adder, shown in Fig3, is obtained from the CPL, and has a smaller number of transistors since it uses only one NMOS tree for each output, with the complementary output being obtained by a simple inverter. Due to the swing degradation at the first inverter's input, the minimum supply voltage is equal to 2Vtn.

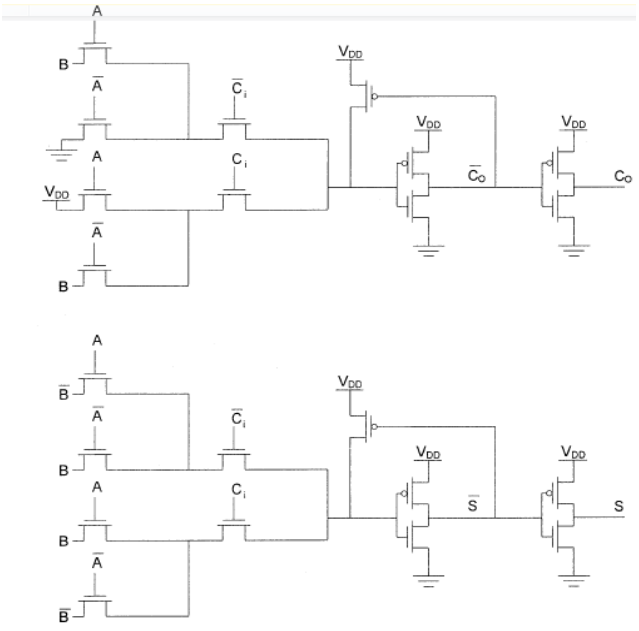

Fig3: Schematic view of the LEAP full adder

2.4. LP full adder

The LP full adder [1], shown in Fig4, has low power consumption because it is based on the low-power XOR and XNOR cells.

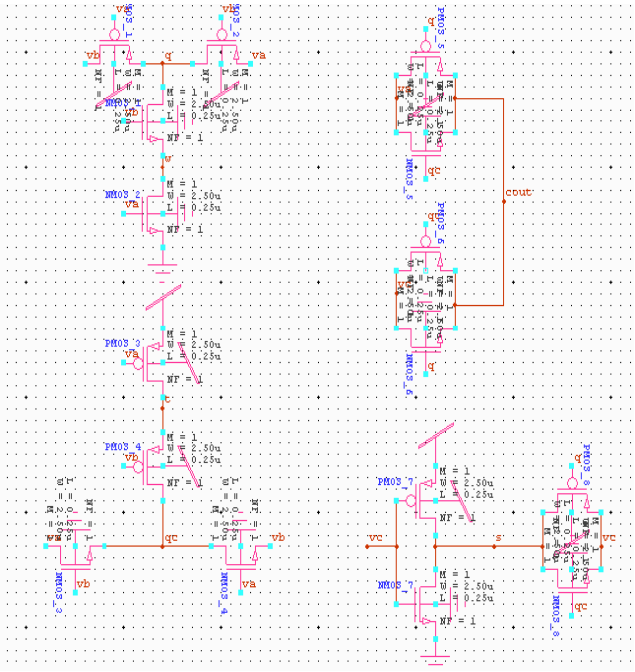

Fig4: Schematic view of the LP full adder

2.5. MIRROR adder

The MIRROR adder, in Fig5, is simply derived from the CMOS adder by directly connecting the series PMOS transistors to the supply, both in the carry and sum circuits, since when **A=B=0**, the series connected PMOS transistors are connected to Vdd.

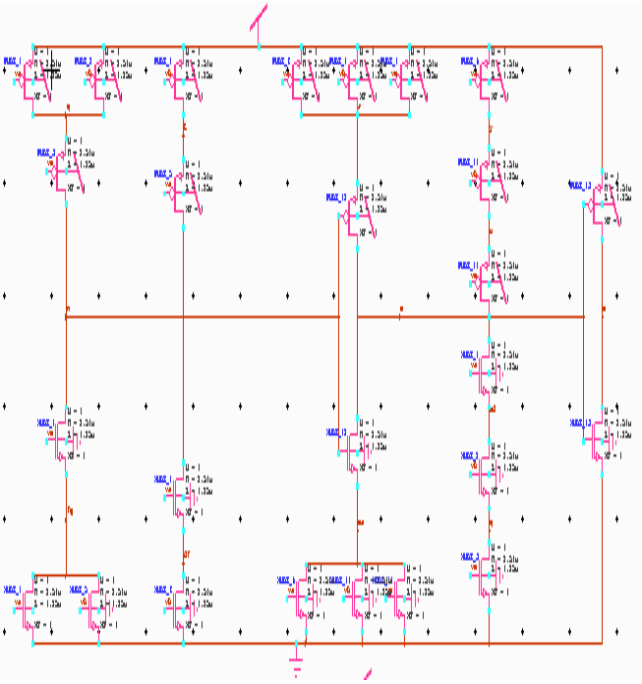

Fig5: Schematic view of the MIRROR adder

2.6. TGdrivecap full adder:

As in the case of the LP adder circuit(in fig4), cascading n full adders leads to an overall propagation delay roughly proportional to n^2, which becomes excessive for long chains of full adders. This drawback is solved in the T Gdrivcap [1], shown in Fig6.

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Output buffers which interrupt the transmission gate chain when cascading full adders are added.

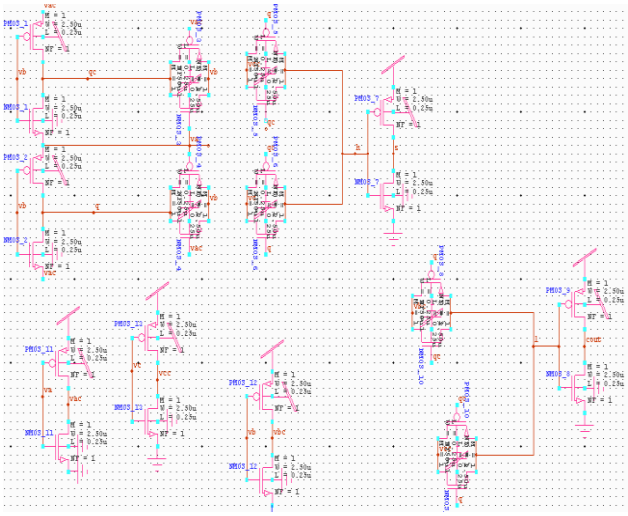

Fig6: Schematic view of the TGdrivecap full adder

2.7. 16-Transistor 1-bit full adder

The 16-transisitor 1-bit full adder, shown in fig7, is based on the 4-transistor implementations of the XOR and XNOR functions. The pass transistor and transmission gates of the cell, which decreases the cell delay. This adder does not use any inverters or standard CMOS style. This eliminates the short-circuit power component within the cell. Finally, the incomplete voltage swing for some input combinations (A = B = 0, A = B = 1) reduces the power consumed in these.

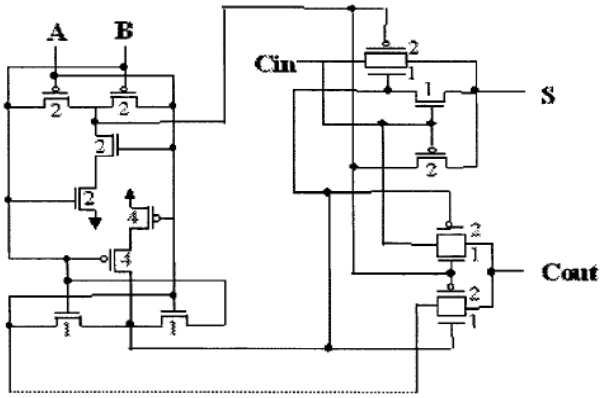

Fig7: Schematic view of 16-Transistor low power full adder

2.8. Conventional CMOS full adder

The Conventional CMOS full adder is based on Transmission gates called the Transmission gates full adder cell (TGA) and it is one of the standard implementations of the 1-bit full-adder cells that is shown in Fig8 and has 20 transistors.

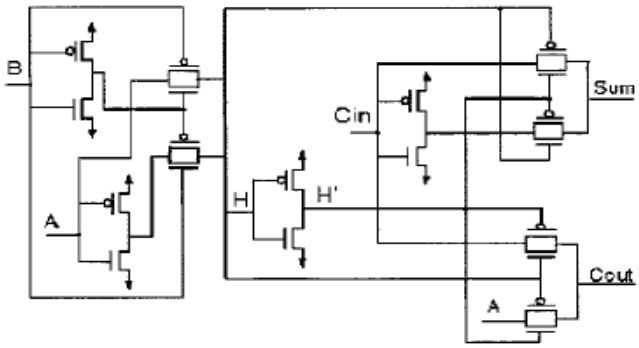

Fig8: Schematic view of Conventional CMOS full adder

2.9. Transmission full adder

The transmission function full-adder cell (TFA), shown in Fig9, is based on the transmission function theory and has 16 transistors. Both XOR and XNOR are used to control the transmission gates generating the Sum and Cout outputs. The inverter introduces unwanted delay between XOR and XNOR leading to a 0–0 or 1–1 overlap. This overlap will cause the transmission gates to act as pass transistors, which may cause glitches (spurious transitions) in the output signals. These glitches will increase the power consumption of these cells. In addition, TGA uses three inverters, while TFA uses two. The presence of inverters will introduce short-circuit power due to the current flowing from the power supply to ground (when both P and N transistors are instantaneously ON).

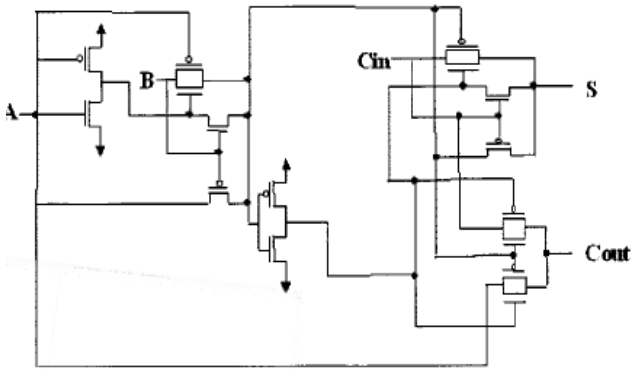

Fig9: Schematic view of Transmission full adder

2.10. 14-Transistor 1-bit full adder

One of the recent enhancements is the 14-transistor adder (14T). Power consumption has been reduced by using the 4-transistor XOR implementation presented in [4], which decreases the overall cell transistor count to 14. 14T uses only one inverter, but it still has the same problem of glitches in the outputs. Also, it has the drawback of introducing a static power component at the inverter output. Due to the incomplete voltage swing of the XOR gate when A = B = 0, both the N and P transistors will be ON (N is weakly ON), which will lead to drawing current from the power supply although the circuit is in steady state. This drawback increases the power consumed by this cell, but still it remains a good candidate for low power applications due to having only 14 transistors.

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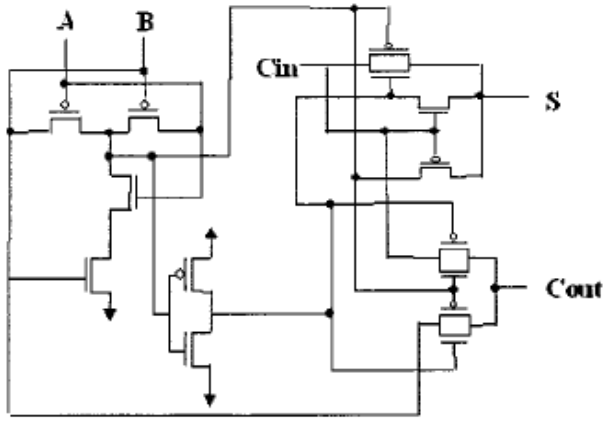

Fig10: Schematic view of 14-transistor low power full adder

III. SIMULATION RESULTS

Here complete simulation results are shown in this section. To compare one-bit full adder performance, we have evaluated delay and power dissipation by performing simulation runs on a Tanner Spice simulation environment using a 150nm CMOS technology. The simulations have been performed for different constant power supply voltages. Each one-bit full adder has been analyzed in terms of propagation delay, minimum, maximum and average power dissipation and power-delay product. The propagation delay has been measured as the time interval between the time the input signal takes to reach 50% of its logic swing and the time the output takes to reach the same value [9]. The power dissipation has been evaluated by averaging the power flowing into the full adder. It is well known that input waveform significantly affects delay and short-circuit power dissipation. Hence, to avoid underestimating delay and power consumption, we have fed realistic waveforms to inputs and by inserting two symmetrical inverters between the ideal voltage sources and the input nodes, while carry input C_i has been obtained by inserting an equal full adder in propagate mode. The sum output and the carry output nodes have been realistically loaded by connecting a minimum-sized inverter and the carry input of an equal full adder, respectively. Results and comments are reported in the subsections that follow: The input and output waveforms of sum and carry bit of CMOS full adder is taken from Tanner simulation tool, which is shown in fig11.

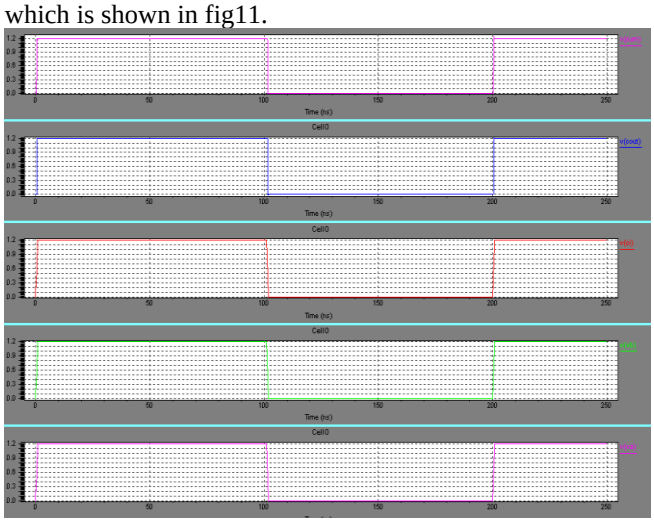

Fig11: Input & Output waveforms of CMOS full adder

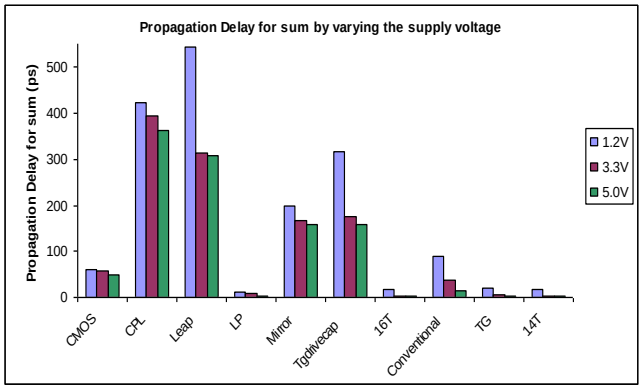

Fig12: Propagation delay of sum for different adder topology by varying supply voltage

In fig12, showing how propagation delay of sum bit for different adder topologies are relating with varying the supply voltages (Vdd=1.2V, 3.3V & 5.0V).

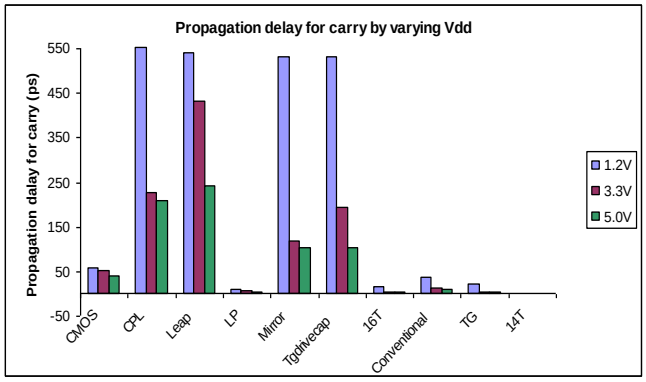

Fig13: Propagation delay of carry for different adder topology by varying supply voltage

In fig13, showing how propagation delay of carry bit for different adder topologies are relating with varying the supply voltages (Vdd=1.2V, 3.3V & 5.0V).

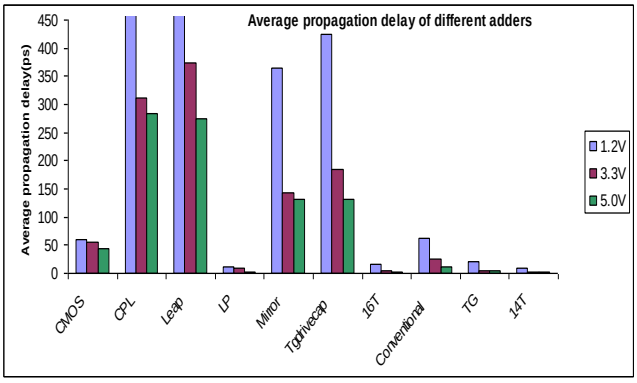

Fig14: Propagation delay of carry for different adder topology by varying supply voltage

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In fig14, Average propagation delay for different adder are changing with different supply voltages (Vdd=1.2V, 3.3V & 5.0V).

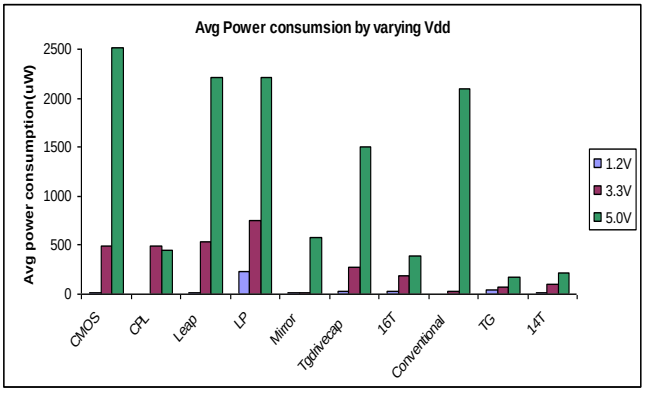

Fig15: Average power consumed by different adder topology by varying supply voltage

In fig15, Average power consumption of different adder are varying with different supply voltages (Vdd=1.2V, 3.3V & 5.0V).

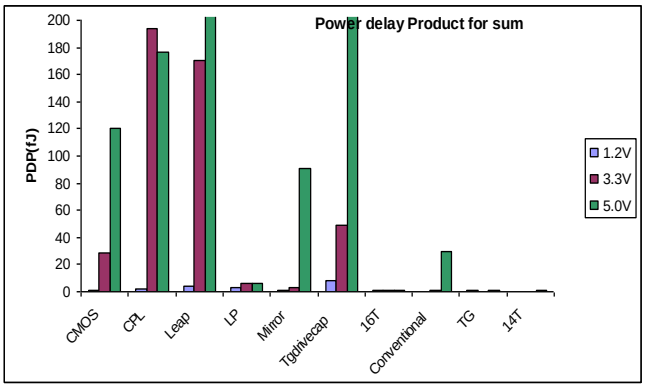

Fig16: Power Delay Product of sum for different adder topology by varying supply voltage

In fig16, Power Delay Product (PDP) of sum bit for different adder is varying with different supply voltages.

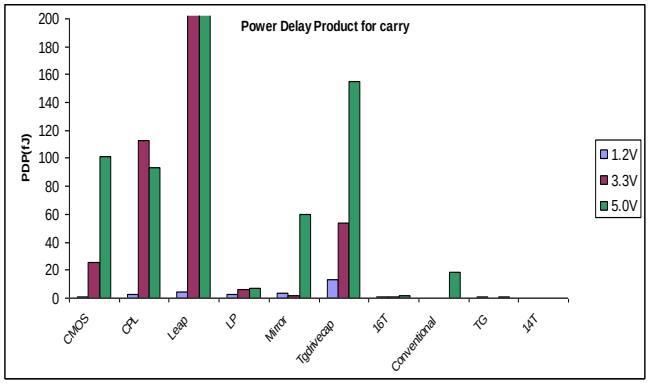

Fig17: Power Delay Product of carry for different adder topology by varying supply voltage

In fig17, Power Delay Product (PDP) of carry bit for different adder is varying with different supply voltages.

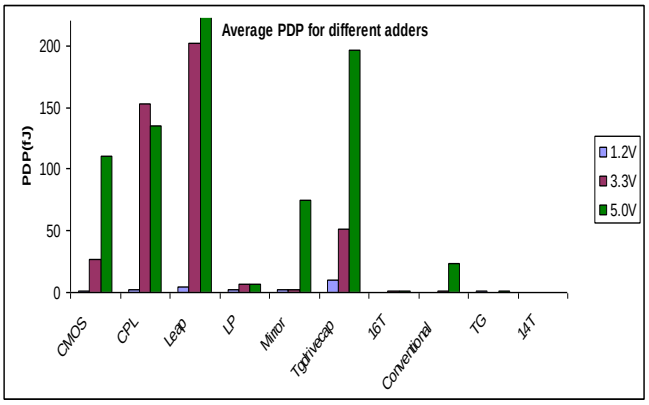

Fig18: Average Power Delay Product of carry for different adder topology by varying supply voltage

Average Power Delay Product (PDP) for different adder is varying with different supply voltages in fig18.

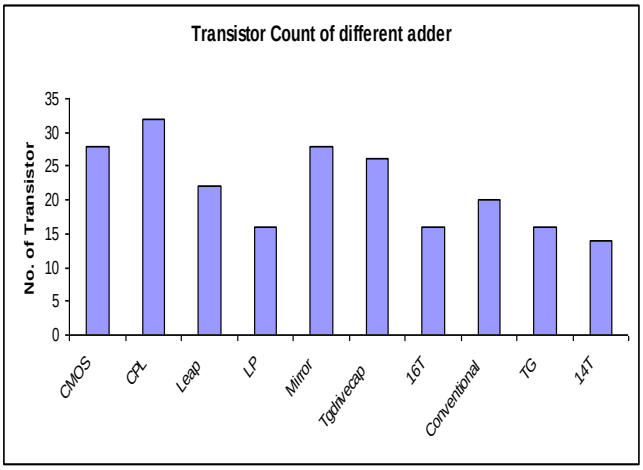

Fig19: No. of transistor required to implement the different adder topology

Fig19 showing no of transistors required to implement the different adder topology. The least no of transistor required in 14T full adder topology and highest no of transistor are required in CPL full adder. In the next section result can be analyzed.

IV. RESULT ANALYSIS & DISCUSSION

The ten full adder topologies like Standard CMOS, CPL, Leap, LP, Mirror, TGdrivecap, 16Transistor, Conventional, Transmission Gate and 14Transistor full adder, are compared in terms of delay, power consumption, Power Delay Product (PDP) and transistor complexity. The details results are shown in table 1. The bold data are showing the minimum value of the different performance parameters. From table2 it is noted that summery of all results are given. The bold value in the table 1, showing the least performance parameter.

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4.1. Comparison with respect to average propagation delay:

From the observation table2, it is shown that the smallest propagation delay is found in 14T full adder for any supply voltage. For medium and low supply voltage delay noted maximum in Leap adder. CPL adder has least speed at higher supply voltage.

4.2. Comparison with respect to average power consumption:

It is also shown that the smallest & highest power consumed in Conventional & LP full adder for lower supply voltage. For medium supply voltage the smallest & highest power consumed in Mirror & LP full adder. CMOS and TG will consume maximum and minimum power in high voltage application.

Table2: Summery of lowest and highest performance of different adder

Measuring Parameter	Vdd=1.2V		Vdd=3.3V		Vdd=5V	
	Max	Min	Max	Min	Max	Min
Average Propagation Delay	Leap	14T	Leap	14T	CPL	14T
Avg. power consumed	LP	Conven -tional	LP	Mirr -or	CMOS	TG
Average PDP	TGdriv -ecap	14T	CPL	14T	TGdriv -ecap	14T

4.3. Comparison with respect to average PDP:

It is also shown that the smallest Power Delay Product in 14T full adder for lower supply voltage. For low & high supply voltage the highest PDP in TGdrivecap full adder. PDP in medium supply voltage will be highest in CPL adder.

V. CONCLUSION

In this paper, ten different full adder topology like Standard CMOS, CPL, Leap, LP, Mirror, TGdrivecap, 16Transistor, Conventional, Transmission Gate and 14Transistor full adder are circuits are implanted using Tanner EDA simulation tool for 150nm technology. They are compared in terms of delay, power consumption, Power Delay Product (PDP). VLSI designer can easily implement the different full adder circuits using this concept.

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Table 1: Complete Observation results of different topologies of CMOS full adder for different Supply Voltages

Sl. No.	Different Topology	Variation of Supply Voltage(V)	Propagation Delay for sum (ps)	Propagation Delay for carry (ps)	Avg. Power Consumed (μW)	PDP for Sum(fJ)	PDP for Carry (fJ)	Transistor Count
1	**CMOS Full Adder**	1.2	60.63	59.59	17.73	1.0750	1.0565	28(2)
		3.3	57.86	51.18	492.51	28.4966	25.2067	
		5.0	47.74	40.18	2520	120.3048	101.2536	
2	**CPL Full Adder**	1.2	423.37	552.90	4.23	1.7909	2.3388	32(2.3)
		3.3	393.64	228.66	492.50	193.8677	112.6151	
		5.0	361.4	208.52	449.60	176.9805	93.7506	
3	**Leap Full Adder**	1.2	545.63	541.73	8.17	4.4578	4.4259	22(1.6)
		3.3	315.05	431.80	541.55	170.6153	233.8413	
		5.0	308.5	241.74	2205.28	742.0289	581.4524	
4	**LP Full Adder**	1.2	**12.54**	11.56	227.20	2.8491	2.6264	16(1.1)
		3.3	8.76	7.76	749.84	6.5686	5.8188	
		5.0	**2.679**	2.85	2215.28	6.4437	6.8550	
5	**Mirror Full Adder**	1.2	197.43	531.34	7.44	1.4689	3.9532	28(2)
		3.3	167.8	117.41	**17.36**	2.9130	2.0382	
		5.0	158.5	103.36	575.52	91.2199	59.4857	
6	**TGdrivecap Full Adder**	1.2	317.78	531.34	24.66	7.8365	13.1028	26(1.9)
		3.3	176.58	194.71	276.54	48.8314	53.8451	
		5.0	158.5	103.36	1502.71	238.1795	155.3201	
7	**16 Transistor Full Adder**	1.2	16.52	17.40	30.96	0.5115	0.5387	16(1.1)
		3.3	4.16	4.42	186.78	0.7770	0.8256	
		5.0	3.29	3.51	384.70	1.2657	1.3503	
8	**Conventional Full Adder**	1.2	89.62	36.70	**4.16**	0.3728	0.1527	20(1.4)
		3.3	36.7	13.34	32.80	1.2038	0.4376	
		5.0	13.89	8.80	2094	29.0857	18.4272	
9	**Transmission Gate Full Adder**	1.2	21.28	22.52	36.41	0.7748	0.8200	16(1.1)
		3.3	5.34	5.77	**66.88**	**0.3571**	0.3859	
		5.0	4.11	4.47	168.16	**0.6911**	0.7517	
10	**14 Transistor Full Adder**	1.2	17.00	**1.90**	19.00	**0.3230**	**0.0361**	**14(1)**
		3.3	**4.04**	**0.81**	108.24	0.4373	**0.0877**	
		5.0	3.24	**0.76**	214.40	0.6947	**0.1629**	

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