Design & Implementation of E1 to STM-1 Frame and Deframe

Konda Vijayasree, Siva S Yellampalli

Abstract*: *This paper describes the design and implementation of E1 frame and generating STM-1 frame multiplexing 64 E1 Frames, as well as degenerating E1 frame from STM-1 frame. The design of Formatter & Analyzer is implemented in Verilog HDL, functionally validated by simulation, carried out by RTL to GDSII tool and synthesized to get resource utilization and implemented on an FPGA for functionality verification, and the power analysis and area calculation of the framer is analyzed using Cadence v6.1.4 and Xilinx 13.2. The designed framer can be used for generation and analysis of E1 frame that has a data rate of 2.048 Mbps and STM-1 frame that has a data rate of 155.52 Mbps

***Index Terms*: PRBS, E1 frame, scrambler, descrambler, clock divider.**

I. INTRODUCTION

E1 is the lowest level of the Plesiochronous Digital Hierarchy (PDH) and is among the most common ways of transmitting voice & data over telephone and data networks. Physically E1 is transmitted as 32 timeslots, but one is used for framing and typically one allocated for signalling call setup and tear down [1]. Unlike Internet data services, E-carrier systems permanently allocate capacity for a voice call for its entire duration.

E1 is one of the fundamental technologies used in telecommunication but there is insufficient provision for network management within the PDH frame format for them to be able to do this & there is no standard for synchronization. In this method inability to identify individual channels in a higher-order bit stream and Copper interfaces defined, even Overhead percentage increases with rate.

STM1 is a synchronous digital hierarchy (SDH) is standardized multiplexing protocols that transfer multiple digital bit streams over optical fiber using lasers or light-emitting diodes (LEDs) [2]. The method was developed to replace the PDH system for transporting larger amounts of telephone calls and data traffic over the same fiber without synchronization problems. This method provides High Transmission Rates, high data rates by multiplexing any size frame, limited only by technology Provide, reduced bit rate errors and high levels of recovery from faults.

Revised Manuscript Received on 30 July 2012
***Correspondence Author(s)**

Konda Vijayasree, Department of VLSI Design and Embedded Systems, Visveswaraya Technological University, UTL Tech. ltd., VTU Extn. Center, UTL Technologies, Bangalore, India.
Dr. Siva S Yellampalli, Department of VLSI Design and Embedded Systems, Visveswaraya Technological University, UTL Tech. ltd., VTU Extn. Center, UTL Technologies, Bangalore, India
.

II. FRAME STRUCTURE

A. E1 Frame Structure

Each channel in a frame has 8 bits and is called a time slot, TS as shown in **Figure 2.1**. Thus, a frame contains a total of 256 bits.

Time slots in a frame are numbered from 0 to 31. Each time slot corresponds to a 64Kbps channel carrying 8 bits of either data or an 8 kHz digitized voice sample. Bits in a time slot are numbered from 1 to 8. Time slots are combined using Timing Division Multiplexing (TDM) at 2,048MHz. Thus, a frame is transmitted each 125µs [3].

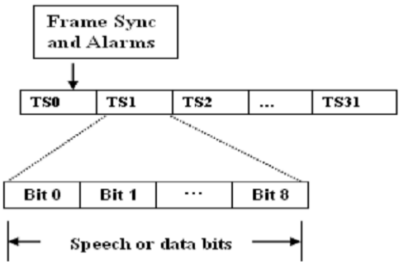


Fig 2.1 E1 frame Structure [1]

B. STM-1 FRAME STRUCTURE

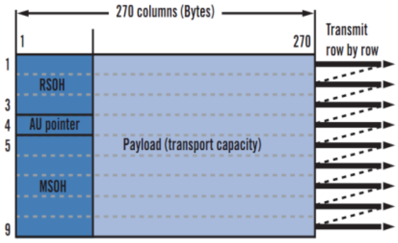


Figure 2. 2. STM-1 Frame Structure [2]

Multiple frames are grouped to transportalignment, error detection and service information. Sixty four consecutive frames constitute an STM-1 Frame structure.

The STM-1 frame is capable of transporting any PDH tributary signal (≤ 140 Mbit/s). The frame comprises of section overhead (SOH), pointer and the payload as shown in **Figure 2.2.**

Published By:
Blue Eyes Intelligence Engineering
and Sciences Publication (BEIESP)
© Copyright: All rights reserved.

C. SDH Mapping of E1 Frame

D. r

The **figure 2.3** represents the mapping of E1 frames into STM-1 Frame. Stuffing bytes are added in the container one at the head and the other at the tail of each frame [2].The lower order POHs are added at the head of each frame in the VC12. Adding of pointers takes place at the head of each frame in the TU12.Three parallel TU12s are multiplexed to form a TUG-2 Seven TUG-2s are multiplexed to form a TUG-3Multiplexing of three TUG3s with stuffing bytes at the header forms the input to VC.

Higher order path over heads are added at this level, which is the input to AU4. The location of the starting byte J1(VC-4) is written in pointer bytes H1 and H2. This process is defined as pointer processing AUG, performs the function of concatenation in case of higher order STMs. In STM-1, virtually there is no difference between AUG and AU-4 AUG is attached with SOH, to form an STM-1 (1st order of Synchronous Transport module)

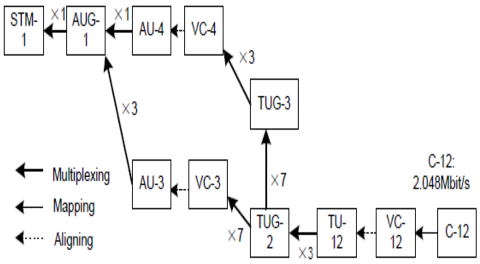


Figure 2.3 : Mapping of E1 frame to STM-1 frame [3]

E. Specifications

According to the ITU-T standard G.707 the specification

Data rate for E1 frame[1]

Frame lengt	: 256 bits
Each slot capacity	: 64 kbps
Frame repetition rate:	8000 frames/s
Transmission time	: 125μs
Data rate	: 2.048Mbps

Data rate for STM1 Frame[2]

Number of rows	: 9 rows
Number of columns	: 270 columns
Number of bytes/frame	: 2,430 bytes
Number of bits/frame	: 19440 bits
Each slot capacity	: 64 kbps
Frame repetition rate	: 8000 frames/s
Transmission time	: 125μs
Data rate	: 155.54 Mbps

III. STM1 FRAME FORMATTER

A. *STM-1 Frame Formatter*

STM1 is a scalable Frame Formatter, allowing 64 E1 carrier channels [frame signal] to mapped/Demapped into/from STM-1 Frame.E1 to STM-1 multiplexing is a several step process of merging 64 E1 lines into a single STM-1 line, the several steps are illustrated in the below figure-3.1.

The first step is the container [3], Input signals are placed into the containers. It adds stuffing bytes for PDH signals, which compensates for the permitted frequency deviation between the SDH system and the PDH signal.The second step is the virtual [3], It adds overheads to a container or groups of tributary units, that provides facilities for supervision and maintenance of the end to end paths.The third step is the tributary unit [3], It adds pointers to the VCs. TU's acts as a bridge between the lower order path layer and higher order path layer.

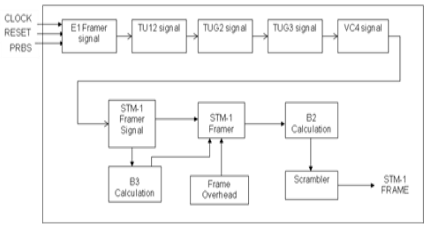


Figure 3.1: E1 to STM-1 Frame Formatter Block Diagram

The Fourth step is Tributary Unit Group [3], It defines a group of tributary units that are multiplexed together. As a result, a TU group could contain one of the following combinations:

1. Three TU-12s (TUG – 2)
2. Seven TUG-2s (TUG – 3)

The fifth step is Administrative Unit [3], It adds pointer to the HO Virtual Containers (similar to the tributary unit).then forming the Administrative Unit Group, It defines a group of administrative units that are multiplexed together to form higher order STM signal.

The last step is generating the Synchronous Transport Module – N [3], It adds section overhead (RSOH & MSOH) to a number of AUG's that adds facilities for supervision & maintenance of the multiplexer & regenerator sections. This is the signal that is transmitted on the SDH line. The digit "N" defines the order of the STM signal.

B. *E1 Frame*

The E1 framing is the first level in the digital hierarchy. The E1 frame carries 30 voice channels in a 256-bit frame. Since 30 channels only require 240 bits, 16 bits are available for framing, signaling, error checking and supervisory communications. These extra 16 bits are divided into two groups of 8 bits each.

C. Buffer Memory

To attain synchronization between the lower rate tributaries [E1], buffer memories are placed between the tributaries and the bit interleave [Multiplexer].

Published By:
Blue Eyes Intelligence Engineering
and Sciences Publication (BEIESP)
© Copyright: All rights reserved.

Synchronization is achieved by reading out bits from the buffer memory with a higher bit rate than when writing bits into it.

D. Digital Multiplex

The main principle for digital multiplexing is the bit interleaving process in which the tributaries are combined bit by bit to a common outgoing bit flow.

At each of the higher transmission levels in the network, four lower rate tributaries are combined by Time Division Multiplexing (TDM) to produce one higher rate signal. This multiplexing process is used to transmit a large number of digital voice channels over the same physical path. Similarly the demultiplexing process is used to transmit a small number of voice channels.

E. Frame Synchronous

Framing synchronous [9] is necessary so that any equipment receiving the STM-1 signal can synchronize, identify, and extract the individual channels.

F. STM-1 Framer Formatter

The frame formatter is made up of sixty four sets. The sixty four sets are transmitted one after another (...Set1/Set2/.../set64/Set1...) to make up the complete STM-1 frame formatter. The section over head is placed in the first 10 bits of every row.

At each stage when the tributaries are combined, the resulting bit rate is slightly higher than the input bit rate that is, 64 x 2048 kb/s = 131072 kb/s, but the actual rate is 15554 kb/s.

These extra bits are overhead, introduced as part of the multiplexing process.

G. Deframer

The **figure 3.2** shows the block diagram of STM-1 Deframer. The STM-1 Frame signal is fed to the Frame Synchronization block which performs frame synchronization as per ITU-T G.707 [1].

The Received signal is descrambled and then fed to the Overhead detector which will detect the overhead**.** It verifies the incoming B1 value and indicates the presence and number of any B1 errors. It also extracts the Regenerator Section Overhead and outputs it from the core. The Overhead block verifies the incoming B2 value and indicates the presence and number of any B2 errors. It also extracts the Multiplex Section Overhead and outputs it from the core. The block extracts Higher Order Path Overhead for all the configured VCs. It also calculates and verifies the B3 value for all VCs and indicates the presence and number of B3 errors.

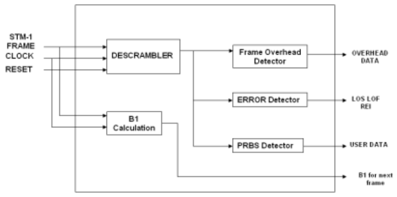


Figure 3.2: STM – 1 De-Framer

The PRBS detector block will compare the received payload data with the original data and will indicate if the data received is correct or not. The Error Detector Block will detect the errors present in the received data and will

generate the errors which have been generated.

IV. DESIGN & IMPLEMENTAION

A. Frame

The **Figure 4.1** shows the block diagram of how an STM-1 frame is generated. The 8 bit PRBS data is used to fill the payload section of the STM-1 frame. At every positive edge of the clock the PRBS data is fed into the Framer block. When the RESET signal is set the frame will be reset to the initial value.

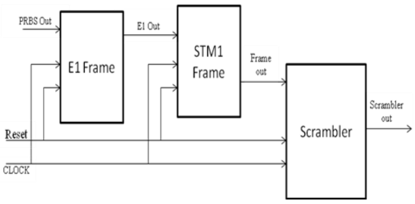


Figure 4.1: E1 to STM-1 Frame Generation

The Regenerator section overhead and Multiplex section overhead values are also sent into the framer at appropriate positions to complete the frame. The B2 calculation block will calculate the parity of all the bytes except for the regenerator section overhead before scrambling and is placed in the following frame. The B3 calculation block will calculate the parity of all the bytes of the payload section before scrambling and is placed in the following frame.

Finally the Scrambler block will scramble the incoming data and will then transmit the scrambled data.

The figure 4.2 shows the PRBS block will give the inputs to the STM-1 payload section.

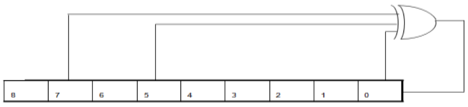


Figure 4.2. PRBS Block Diagram

Figure 4.3 shows the scrambler. Scrambling of the bits in a synchronous transport module (SONET) frame is needed to keep the frequency content of the transmitted signals near the actual line rate [6].

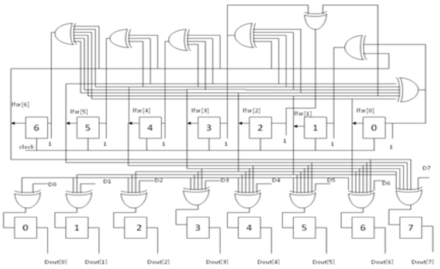


Figure 4.3. Scrambler Diagram

There are two main reasons why scrambling is used

1. To eliminate long sequences of zeros and ones.
2. It eliminates the dependence of a signal's power spectrum upon the actual transmitted data, making it more dispersed to meet maximum power spectral density requirements.

The scrambler used in this implementation is a parallel scrambler shown in figure 5. The scrambler is reset to 1111111 at the start of the frame, by loading all seven flip flops with 1’s

B. Deframe

The **figure 4.4** shows the overall block diagram of how an E1 frame is regenerated from the STM1 frame. The STM-1 Frame signal is fed to the Frame Synchronization block which performs frame synchronization as per ITU-T G.707 [1].

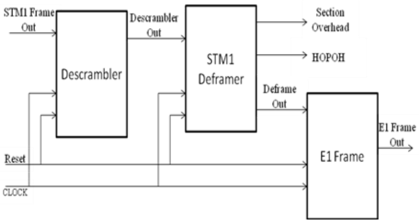


Figure 4.4: Block diagram of Deframer[3]

The received serial STM1 is the input to the Deframer block as shown in Figure. The other inputs to this block are clock and reset. When reset is made high, all the internal registers are set to predefined values. When reset goes low, this block takes the serial data from the receiver on negative edge of the clock.

Frame head detector: The frame head detector block is used at the Receiving end to determine whether the frame has started or not. This is done by comparing the first six bytes with A1 and A2 which is the Frame Alignment Word and is used to recognize the beginning of an STM-N frame. A1 has a default value of F6h and A2 has a default value of 28h. The head detector will wait for these values and whenever it encounters all the six values the head signal will be asserted to indicate the start of the frame. Once the head signal is asserted the STM data will be extracted. The frame head detector has designed based on [2].

FSM shown in figure 4.5 is designed for the implementation of Head Detector. The FSM has 7 states.

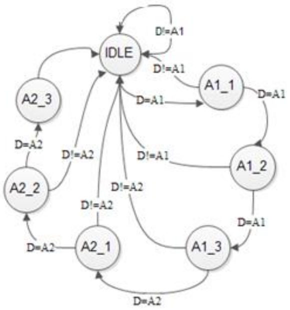


Figure 4.5 FSM for Head Detector

IDLE: When Reset signal is high FSM remains in IDLE state and it makes transition to state A1_1 when Reset goes low and input data is equal to A1.

A1_1: If the input data is equal to A1 the FSM makes transition to state A1_2 else it goes to the IDLE state.

A1_2: If the input data is equal to A1 the FSM makes transition to state A1_3 else it goes to the IDLE state.

A1_3: If the input data is equal to A2 the FSM makes transition to state A2_1 else it goes to the IDLE state.

A2_1: If the input data is equal to A2 the FSM makes transition to state A2_2 else it goes to the IDLE state.

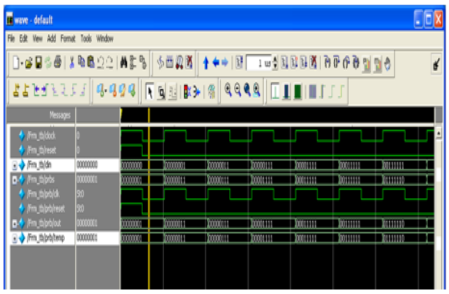
A2_2: If the input data is equal to A2 the FSM makes transition to state A2_3 else it goes to the IDLE state.

A2_3: At this state the first six bytes will be detected indicating the start of the frame and hence the head signal will be asserted and the FSM makes transition to IDLE state to reset the head signal.

V.TESTS AND RESULTS

A. Simulation and Synthesis results of Frame

The design of PRBS has been described in verilog, Figure 5.1 depicts the simulation result of 8 bit PRBS, the output data is generated based on the polynomial.



/Frm_tb/clock 0
/Frm_tb/reset 0
/Frm_tb/din 00000000
/Frm_tb/prbs 00000001
/Frm_tb/prbs/clk St0
/Frm_tb/prbs/reset St0
/Frm_tb/prbs/out 00000001
/Frm_tb/prbs/temp 00000001

Figure 5.1 Simulation result of PRBS

Figure 5.2 depicts the simulation result of the E1 frame generator module. This figure illustrates the functional validation of E1 Frame Formatter.

Published By:
Blue Eyes Intelligence Engineering
and Sciences Publication (BEIESP)

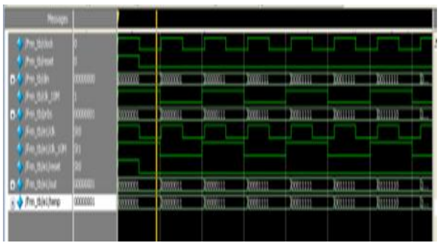


Figure 5.2 Simulation result of E1

Figure 5.3 depicts the simulation result of the STM-1 frame generator module. When the reset signal is high at the positive edge of the clock the count will be initialized to zero and the input will be zero, once the reset signal is made low the input from the PRBS generator will be coming in but since the STM-1 frame consists of overhead bytes, stuffing bytes, and pointers those values are stored at the corresponding count values.

In the below figure since the first three bytes have to the frame synchronization bytes A1 which is equal to F6h has been passed and the next three bytes have to be A2 which is equal to 28h, then the 7th byte is J0 which is the path trace byte and the eight n ninth bytes are reserved for future use so they have been given a constant value of zero.

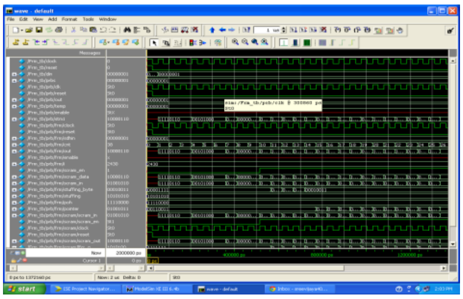


Figure 5.3 Simulation result of E1 to STM-1 Frame

Figure 5.4 depicts the simulation result of 8 bit Scrambler module. In the case of an SDH frame the first 9 bytes of the frame must not scrambled as per the ITU.T standard G.707 [1].

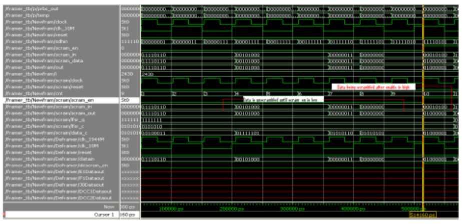


Figure 5.4 Simulation results of the Scrambler

RTL view of the Frame in Cadence : The following Figures 5.5, 5.6, 5.7 shows the representation of the netlist obtained using the DC_SHELL GUI viewer.

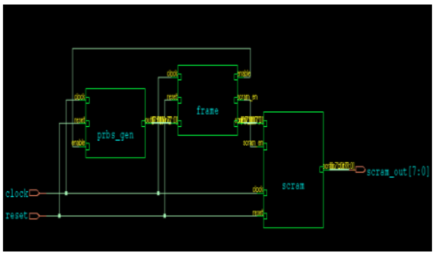


Figure 5.5 E1 to STM-1 Frame

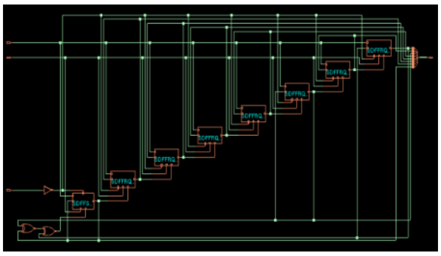


Figure 5.6 PRBS Circuit

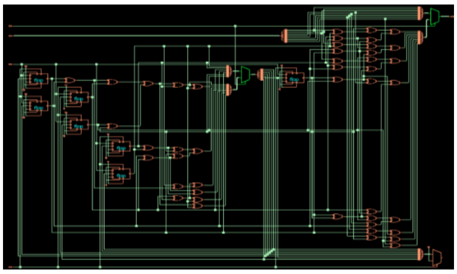


Figure 5.11 Scrambler circuit

Physical Disign Layout: The logic synthesis of the code was Carry the net list through a Physical Design flow which consist of the floor plan, placement, clock tree synthesis, and route, then A GDSII layout is generated for the design, which is programmed to physical design.

The figure 5.12 shows the layout diagram of the frame.

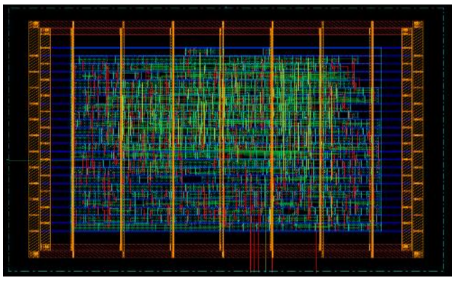


Figure 5.12 Layout view of the Frame

Area Report:

Instance	Cells	Cell Area
STM1_Frame_Gen	634	3604
frame	559	3075
inc_add_69_24_5	61	280
scram	64	360
prbs_gen	11	169

Gate Report:

Type	Instances	Area	Area %
Sequential	89	1433.074	39.8
Inverter	38	80.438	2.2
logic	507	2090.693	58.0
total	634	3604.205	100.0

RTL view of the Frame in Xilinx : The figure 5.13 shows the register transfer logic view of the complete top module on Spartan 6 SP605 evaluation kit.

Published By:
Blue Eyes Intelligence Engineering
and Sciences Publication (BEIESP)

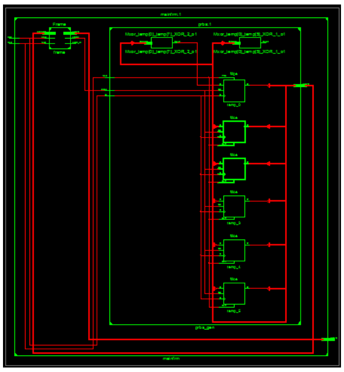


Figure 5.13 RTL view of the complete design of Frame

B. Simulation and Synthesis results of DeFrame

Figure 5.14 depicts the simulation result of the descrambler circuit. While transferring the data in framer side scramble the output data, so to degenerate the original data at the receiver side descrambler operation will perform.

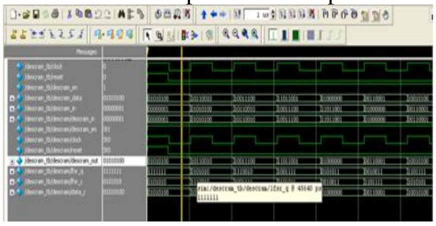


Figure 5.14 Simulation results of descrambler

Figure 5.15 depicts the simulation result for Frame Head Detector block. The frame head detector is used at the receiver end to detect the frame synchronization bytes of the frame which indicates the start of the frame.

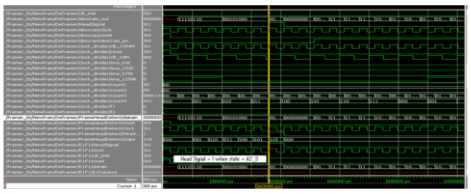


Figure 5.15 Simulation Results of Frame Head detector

Figure 5.16 depicts the simulation result of the E1 frame degenerate from STM-1 module. This results consists the 64 E1 frames with stuffing bytes, pointers, POH and section overhead.

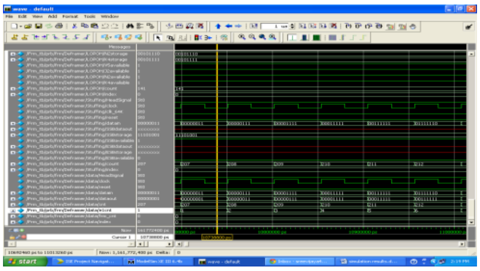


Figure 5.16 Simulation Results of DeFrame

RTL view of the DeFrame in Cadence: The following Figures 5.17, 5.18 shows the representation of the netlist obtained using the DC_SHELL GUI viewer.

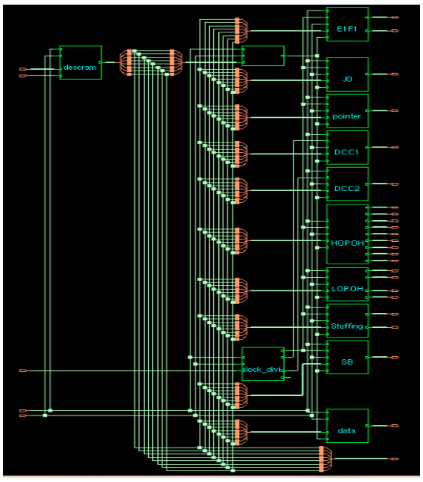


Figure 5.17 GUI of Deframer

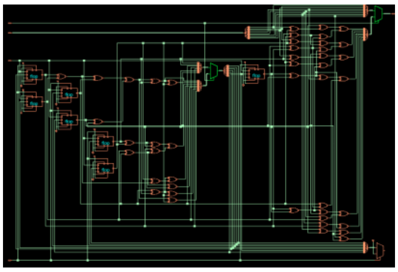


Figure 5.18 GUI of Descrambler

Physical Disign Layout: The logic synthesis of the code was Carry the net list through a Physical Design flow which consist of the floor plan, placement, clock tree synthesis, and route, then A GDSII layout is generated for the design, which is programmed to physical design.The figure 5.19 shows the layout diagram of the frame.

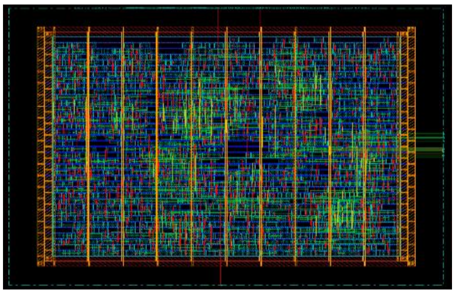


Figure 5.19 Layout View of Deframer

Area Report:

Instance	Cells	Cell
SDHProcess	2552	21020
DCC2	347	3728
HOPOH	340	3400
LOPOH	231	2049
DCC1	243	2010
Stuffing	224	1715
E1F1	217	1705
SB	220	1497
data	244	1438
pointer	187	1355
J0	162	1231
clock_divider	54	411
descram	64	363
HD	19	116

Published By:
Blue Eyes Intelligence Engineering
and Sciences Publication (BEIESP)
© Copyright: All rights reserved.

Gate Report:

Type	Instances	Area	Area %
sequential	874	13584.211	64.6
inverter	52	110.074	0.5
logic	1626	7325.539	34.9
total	2552	21019.824	100.0

RTL view of the Frame in Xilinx : The figure 5.13 shows the register transfer logic view of the complete top module on Spartan 6 SP605 evaluation kit.

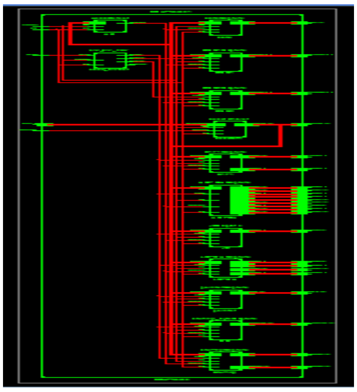


Figure 5.20 RTL view of the complete design of DeFrame

C. CONCLUSIONS

This paper presents the E1 to STM-1 Framer and Deframer, with basic Frame length of 2430 bytes (19440 bits). Each Frame is transmitted at 125usec. The Frame is mapped in a bit interleaved fashion, into a higher rate signal and damped into a small rate signal. This soft core offers high data rate and also provides a faster and lower cost solution.

ACKNOWLEDGEMENT

I acknowledge Dr. V. Venkateswarlu, Principal, UTL Technologies for his guidance and suggestion and UTL Technologies for providing lab facility during the design and implementation.

REFERENCES

1. Data communication & Networking: E and T carrier, Available: http://datacombasic.blogspot.in/2011/03/e-and-t-carrier.html.
2. Khamer Fathima U B, Nandini, Vijay Ramprasad "Design and Implementation of E1 submultiframe (SMF) Formatter and Analyzer'' 2011.
3. ITU-T Recommendation G.702, "Digital Hierarchy bit rates",1988.
4. TEKTRONIX, INC. "SDH Telecommunications Standard Primer" http://www.tektronics.com/optical.
5. E2-E3: Enterprise & Wholesale, "SDH Overview, CPE, Protection schemes" april-2011.
6. SDH.PG.OPT.TM.AE, Available: http://www.jdsu.com/ProductLiterature/sdh_pg_opt_tm_ae.pdf.
7. "Microwave Radio Transmission Design Guide", Second Edition,Trevor Manning-2009.
8. ITU-T Recommendation G.704 "Synchronous frame structures used at 1544, 6312, 2048, 8448 and 44736 kbit/s hierarchical levels",1998.
9. ITU-T, Recommendation G.706, "General Aspects of Digital Transmission Systems", 1991.
10. ITU-T, Recommendation G.707, "Network Node Interface for Synchronous Digital Hierarchy", 2003.