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Dynamic Power Suppression Technique in Booth Multipliers

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Abstract: ***The SPST has been applied on both the modified Booth decoder and the compression tree of multipliers to enlarge the power reduction. This paper provides the experience of applying an advanced version of our former spurious power suppression technique (SPST) on multipliers for high-speed and low-power purposes. To filter out the use-less switching power, there are two approaches, i.e., using registers and using AND gates, to assert the data signals of multipliers after the data transition. The simulation results show that the SPST implementation with AND gates owns an extremely high flexibility on adjusting the data asserting time which not only facilitates the robustness of SPST but also leads to a 40% speed improvement. Adopting a Xilinx Spartan 3 Xc3s200 board the proposed SPST-equipped multiplier dissipates only 0.0121 mW per MHz in H.264 texture coding applications, and obtains a 40% power reduction and the overall utilization of the resources reduced to 26%.***

Index Term: low-power multiplier, spurious power suppression technique (SPST)

I. NTRODUCTION

With the recent rapid advances in multimedia and communication systems, real-time signal processing's like audio signal processing, video/image processing, or large-capacity data processing are increasingly being demanded. Most digital signal processing methods use nonlinear functions such as discrete cosine transform (DCT) or discrete wavelet transform (DWT). Because they are basically accomplished by repetitive application of multiplication and addition, the speed of the multiplication and addition arithmetic's determines the execution speed and performance of the entire calculation. Because the multiplier requires the longest delay among the basic operational blocks in digital system, the critical path is determined by the multiplier, in general. For high-speed multiplication, the modifiedradix-4 Booth's algorithm (MBA) is commonly used. The most effective way to increase the speed of a multiplier is to reduce the number of the partial products because multiplication proceeds a series of additions for the partial products. To reduce the number of calculation steps for the partial products, MBA algorithm has been applied mostly where Wallace tree has taken the role of increasing the speed to add the partial products. To increase the speed of the MBA algorithm, many parallel multiplication architectures have been researched.

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The design [1] proposes a concept called partially guarded computation (PGC), which divides the arithmetic units, e.g., adders, and multipliers, into two parts, and turns off the unused part to minimize the power Consumption. The reported results show that the partially guarded computation can reduce power consumption by 10% to 44% in an array multiplier with 30% to 36% area overheads in speech related applications. Design [2] proposes a 32-bit 2's complement adder equipping a master-stage flip-flop and a slave-stage flip-flop for both operands of the adder, a dynamic-range determination (DRD) unit, and a sign-extension unit. This design tends to reduce the power dissipation of conventional adders for multimedia applications. Additionally, design [3] presents a multiplier using the DRD unit to select the input operand with a smaller effective dynamic range to yield the Booth codes. The direct report of [3] shows that the multiplier can save over 30% power dissipation than conventional ones. Design [4] incorporates a technique for glitching power minimization by replacing some existing gates with functionally equivalent ones that can be "frozen" by asserting a control signal. This technique can be applied to replace layout-level descriptions and guarantees predictable results. However, it can only achieve savings of 6.3% in total power dissipation since it operates in the layout-level environment which is tightly restricted. The design [5] proposes a double-switch circuit-block switch scheme capable of reducing power dissipation during down time by shortening the settling time after reactivation. The drawbacks of the scheme are the necessity for two independent virtual power rails and the necessity for two additional transistors for switching each cell. Design [6] and design [7], respectively, study signal gating schemes for adders and multipliers. Design [6] presents the arithmetic details about the signal gating schemes and illustrates 10% to 45% power reduction for adders.

II. PROPOSED SPURIOUS POWER SUPPRESSION TECHNIQUE (SPST)

The main contribution of this paper is exploring two implementing approaches for the SPST and comparing their efficiency, which provide diverse reference materials for applying the SPST. For completeness of this paper and easy understanding for the readers, we simply review the former SPST first. In Fig. 1, the SPST is illustrated through a low-power adder/subtract or design example. The adder/subtract or is divided into two parts, i.e., the most significant part (MSP) and the least significant part (LSP).The MSP of the original adder/subtract or is modified to include detection logic circuits, data controlling circuits, denoted as latch-A and latch-B in Fig. 1, sign extension circuits, and some glue logics for calculating the carry in and carry out signals.

The most important part of this study is the design of the control signal asserting circuits, denoted as asserting circuits in Fig. 1, following the detection logic circuits.

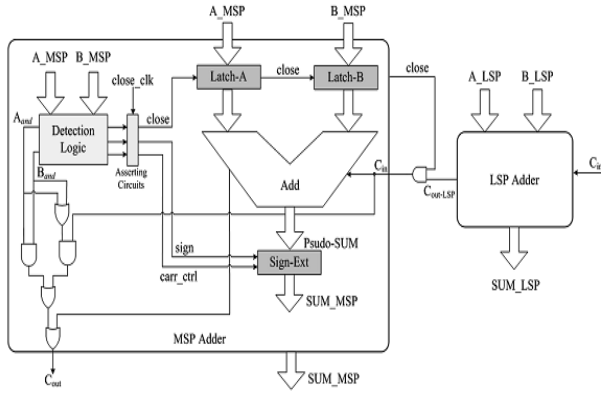

Fig.1 Low-power adder/subtractor design example adopting the SPST.

The control signal assertion circuits is using registers, which is illustrated in the shadow area in Fig. 2.

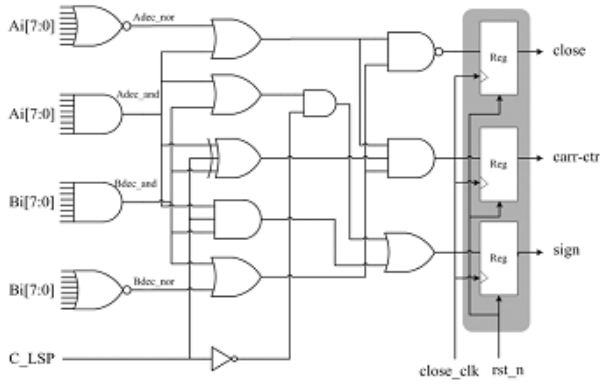

Fig. 2. Detection logic circuits using registers to assert the control signals.

III. LOW POWER MULTIPLIER DESIGN

The proposed low-power multiplier is designed by equipping the SPST on a tree multiplier. There are two distinguishing design considerations in designing the proposed multiplier, as listed in the following by applying the SPST on the Modified Booth Encoder Fig. 3 shows a computing example of Booth multiplying two numbers "2AC9" and "006A," where the shadow denotes that the numbers n this part of Booth multiplication are all zero so that this part of the computations can be neglected. Saving those computations can significantly reduce the power consumption caused by the transient signals.

According to the analysis of the multiplication shown in Fig. 3, we propose the SPST-equipped modified-Booth encoder, which is controlled by a detection unit. The detection unit has one of the two operands as its input to decide whether the Booth encoder calculates redundant computations.

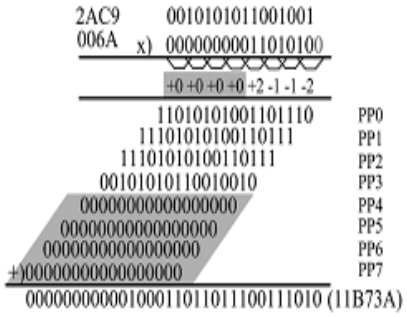

Fig. 5. Illustration of multiplication using modified Booth encoding, where PP0 to PP7 denote the partial products.

The second design considerations in designing the proposed multiplier is by applying the SPST on the Compression Tree.

The proposed SPST-equipped multiplier is illustrated in Fig. 4.The PP generator generates five candidates of the partial products ,i.e., f 2A; A; 0 ; A; 2Ag , which are then selected according to the Booth encoding results of the operand B. Moreover, when the operand besides the Booth encoded one has a small absolute value, there are opportunities to reduce the spurious power dissipated in the compression tree. According to the redundancy analysis of the additions, we replace some of the adders in compression tree of the multiplier with the SPST-equipped adders, which are marked with oblique lines in Fig. 4. The bit-widths of the MSP and LSP of each SPST-equipped adder are also indicated in fraction values nearing the corresponding adder in Fig. 4.

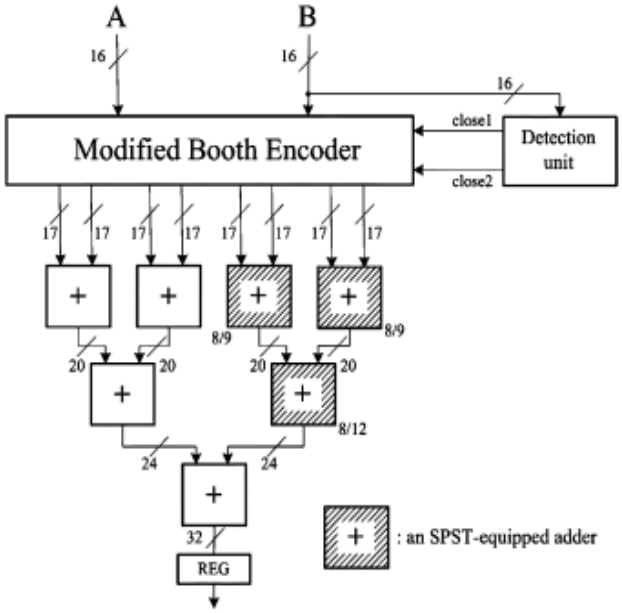

Fig. 7. Proposed low-power SPST-equipped multiplier, where the fraction values denote the bit-widths of the MSP and LSP of the SPST-equipped adders.

IV. MODIFIED BOOTH ALGORITHM

Multipliers play an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried and are trying to design multipliers which offer either of the following design targets – high speed,

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low power consumption regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for various high speed, low power and compact VLSI

The common multiplication method is “add and shift” algorithm. In parallel multipliers number of partial products to be added is the main parameter that determines the performance of the multiplier. To reduce the number of partial products to be added, Modified Booth algorithm is one of the most popular algorithms.

It is a powerful algorithm for signed-number multiplication, which treats both positive and negative numbers uniformly. For the standard add-shift operation, each multiplier bit generates one multiple of the multiplicand to be added to the partial product. If the multiplier is very large, then a large number of multiplicands have to be added. In this case the delay of multiplier is determined mainly by the number of additions to be performed. If there is a way to reduce the number of the additions, the performance will get better. Booth algorithm is a method that will reduce the number of multiplicand multiples. For a given range of numbers to be represented, a higher representation radix leads to fewer digits. Since a k-bit binary number can be interpreted as K/2-digit radix-4 number, a K/3-digit radix-8 number, and so on, it can deal with more than one bit of the multiplier in each cycle by using high radix multiplication.

Multiplicand, A = ● ● ● ●

Multiplier, B = (●●)(●●)

Partial product bits	● ● ● ●	(B1B0)2 $A4^0$
	● ● ● ●	(B3B2)2 $A4^1$
Product, P	= ● ● ● ● ● ● ● ●	

V. PERFORMANCE EVALUATION

The SPST-equipped multiplier design has been realized by following the standard cell-based design flow. The efficiency of applying the SPST on modified Booth encoder is described above. The proposed SPST, 65.67% power dissipation and 28.02% area cost are saved. The simulation results of the original tree multiplier and the two SPST-equipped multipliers with different implementing approaches are listed in Table I.

TABLE- 1

Device Utilization Summary (estimated values)			[-1]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	43	1920	2%
Number of Slice Flip Flops	35	3840	0%
Number of 4 input LUTs	77	3840	2%
Number of bonded IOBs	32	173	18%
Number of GCLKs	1	8	12%

HDL Synthesis Report
Macro Statistics
Counters : 1
4-bit up counter : 1
Registers : 3
1-bit register : 1
16-bit register : 2
Xors : 17
#1-bit xor3 : 17

From Table I, we can know that both the SPST-equipped multipliers using registers and that using AND gates save about 40% power dissipation of the original tree multiplier. However, the maximum operating frequency of the SPST-equipped multipliers using AND gates is 40% higher (200=142 □ 1) than that using registers. Besides, Table also shows that the proposed SPST-equipped multiplier dissipates only 0.0121 mW per MHz when computing the multiplication of texture coding in H.264. The precision analysis of the test pattern “Stefan” sequence is shown in the figure.

VI. CONCLUSION

In this paper, we propose a multiplier adopting the new SPST implementing approach, i.e., using AND gates in the detection logic unit. The simulation results show that the power reduction of the new approach, i.e., a 40% saving, is very close to that of the former approach. Besides, the new approach leads to a 40% speed improvement when compared with the former one. When implemented in a 0.18-_m CMOS technology, the proposed SPST-equipped multiplier dissipates only 0.0121 mW per MHz in H.264 texture coding. In addition, this paper explores the performance of the proposed design under the conditions of different bit-width input data. The results also show that the new SPST approach not only owns equivalent low-power performance but also leads to a higher maximum speed when compared with the former SPST approach. Moreover, the proposed SPST-equipped multiplier also has better power efficiency when compared with the existing modern multipliers.

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