Image Compression Technique using Two Dimensional Discrete Cosine Transform

S. Rajeswari, P. Deepthi, K. V. Ramana Rao

Abstract —This paper presents an architecture for the fast computation of the 8×8 two dimensional (2D) Inverse Discrete Cosine Transform. The proposed method is the permanent storage of the Basis Matrices of the 8×8 2D Discrete Cosine Transform (DCT). The sparseness property of the 2D DCT coefficient matrix, the computational time decreases as the number of nonzero coefficients decreases.

The proposed structure computes all 64 pixel luminance values of an 8×8 block simultaneously. The design was implemented in Xilinx Xc3s500 board and the design used 23% LUT's and 33% of the total slices. The total power consumed by the device was 0.081W.

Index Terms — 2D IDCT, image processing, sparse matrices

I. INTRODUCTION

The Discrete Cosine Transform (DCT) is regarded as one of the best tools in digital signal processing. The standards H.261, and H.263, which are the most widely used in image and video compression, perform two dimensional (2D) DCT on the image dataset and keep only a few of the coefficients calculated, in order to reduce the memory or the bandwidth required. The image under processing is split into 8×8 blocks, and 2D DCT is performed on each block. To obtain the initial picture, the 2D Inverse Discrete Cosine Transform (IDCT) is performed. A variety of algorithms has been proposed, focusing on the speed of computation, the minimization of the required chip area. The research work done until now on 2D DCT/IDCT is based on the separability property of the transform, employing a row-column decomposition method.

This paper employs only the nonzero DCT coefficients, by the implementation of a forward-mapping algorithm [1], resulting in a variable number of operations and computational time per block. The power consumption and the throughput rate can be significantly improved at a high compression rate. The tradeoff between the visual quality and the given power or time constraints by using different numbers of the nonzero DCT coefficients. The proposed architecture improves the work presented in by fully utilizing the symmetry properties of the DCT basis kernel.

II. PROPOSED ARCHITECTURE

The three main domains of the proposed architecture are the superimposition principle, the sparseness property of 2D DCT coefficient matrices and the symmetry of the entries of the Basis Matrices (BM).

A. The Superimposition Principle

The proposed architecture implements 2D IDCT by an algorithm that uses the superimposition principle. For a nonzero coefficient the 2D IDCT matrix that corresponds to this particular coefficient is computed; in other words, this coefficient is multiplied with the corresponding BM of Fig. 1.

Thus, the fraction of the luminance of the block that is associated with this coefficient is obtained. The aforementioned procedure is repeated for every nonzero coefficient, and, the image block is reconstructed by adding the intermediate results

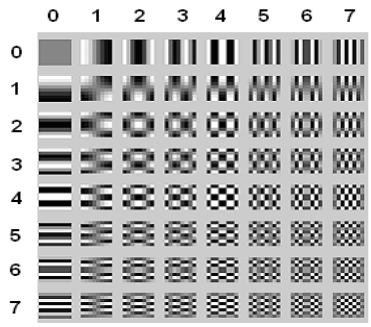

Fig. 1. The Basis Images of the 8×8 2D DCT.

B. Distribution of 2D DCT Coefficients

The decorrelation property of DCT, combined with quantization and compression techniques applied in image processing, result in the sparseness of the 2D DCT coefficient matrix. Typically, DCT blocks of MPEG-compressed video sequences have only five to six nonzero coefficients, mainly located in the low spatial frequency positions.Fig. 2 plots the normalized probability of occurrence of a nonzero spatial frequency foreach block position, based on tests performed on the following, QCIF (Quarter Common Intermediate Format) encoded, video sequences: "Foreman," "Akiyo," "container," "news," "highway," and "bridge-far."

The proposed architecture skips arithmetic operations associated with zero coefficients, since only the nonzero coefficients are multiplied with the corresponding BMs.

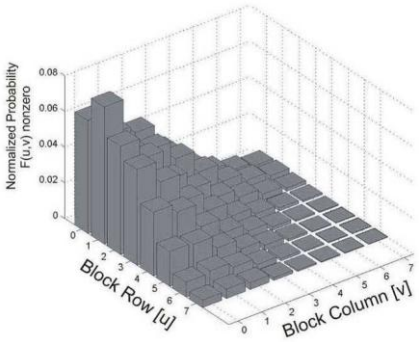

Fig. 2. Probability of occurrence of nonzero DCT coefficients for 8×8 2D DCT image transform

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C. Symmetry of the Entries of the Basis Matrices

The computation of BM10 will be presented as an example of the symmetries in the entries of the BMs. The following substitutions must be done in (2):

$$F(u,v) = \begin{cases} 1, & u=1, v=0 \\ 0, & u\neq 1 \text{ or } v\neq 0 \end{cases}$$

$$\text{SetBM}_{10} = \{\sqrt{2}\cos(\pi/16)/8,\ \sqrt{2}\cos(3\pi/16)/8,\ \sqrt{2}\cos(5\pi/16)/8,\ \sqrt{2}\cos(7\pi/16)/8\}$$

D. Implementation Details

The schematic diagram of the introduced architecture is shown in Fig. 3. It consists of 4 discrete modules: the ROM Bank, the Multipliers Unit, the Interconnections and Sign Network, and the Registers-Adders Unit. The architecture has two inputs: the value, and the order of the coefficient. Both inputs can be provided directly by the run-length decoder (RLD) block, therefore, the sparseness property of the coefficient matrix is exploited without any additional cost. The reconstruction process is accomplished *one clock cycle* after the last nonzero coefficient of the block enters thearchitecture. At that time, the image data of all 64 pixels of an 8×8 block are available simultaneously at the output of the architecture.

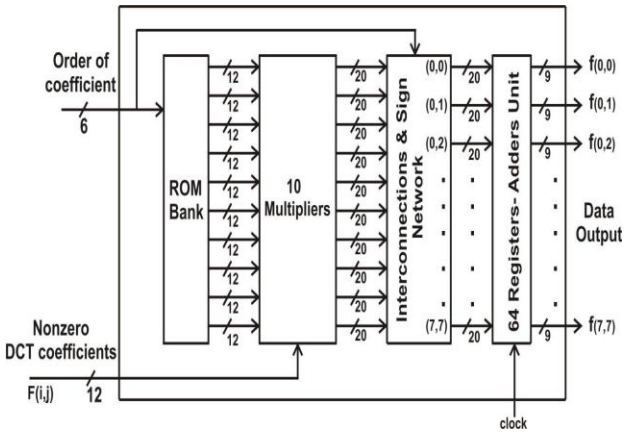

Fig. 3. 8×8 2D IDCT architecture

III. THE ROM BANK AND THE MULTIPLIER UNIT

Fig. 4 illustrates the ROM Bank and the 10 Multipliers Unit, pointed by dashed lines. The ROM Bank consists of 10 ROM cells, with a common address bus, each of which comprises 64 word lines. The number of the ROM cells equals the maximum number of the DAVs of a BM (i.e. it is 10). The ROM cells contain the absolute values of the elements of the BMs. Applying the zigzag scan order of the nonzero coefficient in the address bus, will drive at the outputs of the ROMs the DAVs of the elements of the corresponding BM (in ascending order). In case the entries of a BM have $\delta < 10$ DAVs, the 10-δ last ROMs (i.e. ROM(δ+1)….ROM10) will output zero. For example, in case of the DC coefficient (corresponding to BM00) address 000000 is applied; then, ROM1 outputs 1024 and all nine other ROMs produce 0 at their outputs. The Multipliers Unit consists of 10 multipliers. The destination of this module is to multiply the coefficient with the DAVs of the BMs. It is clear that, for 48 out of the 64 coefficients, not all ten multipliers need to be enabled, since most BMs have less than 10 DAVs. Thus, an extra bit is attached to the words of the ROMs; this extra bit provides the information whether the word is zero or not, in order to activate or deactivate the succeeding multiplier, as shown in Fig. 4.

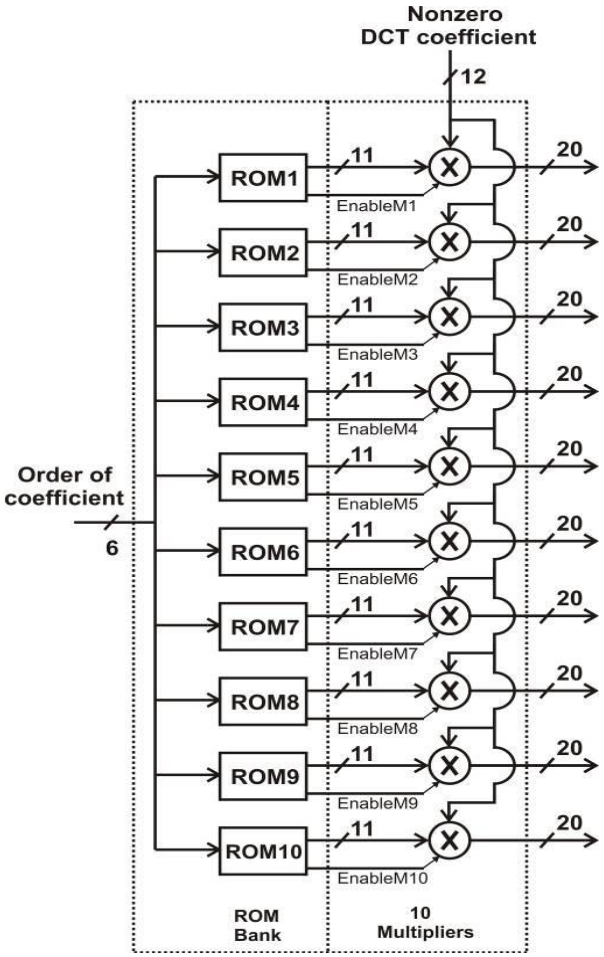

Figure:4 ROM BANK

IV. REGISTERS-ADDERS UNIT

The structure of the 64 Registers-Adders Unit is depicted in Fig. 5. Actually, this unit consists of 64 modules, identical to the one illustrated in Fig. 5, operating in parallel.

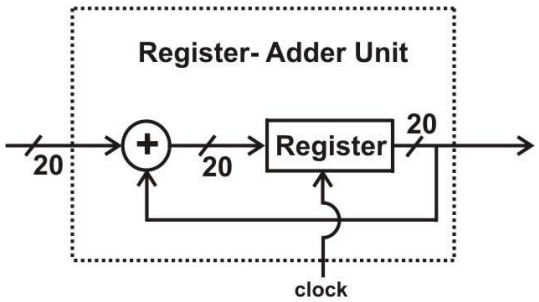

Fig. 5. Registers-Adders Unit

V. PERFORMANCE EVALUATION

The functional blocks of the proposed architecture (i.e. the multipliers, the adders, the registers, the ROM Bank, and the Interconnections and Sign Network), were described in VHDL (Very-high-speed integrated circuits Hardware Description Language) and the architecture was targeted to a XC3s500E

field-programmable gate array (FPGA). For a video sequence with 1920×1080 resolution and 4:2:2 chroma subsampling, the rate of frames (with the aforementioned characteristics) that the proposed architecture can reconstruct per second, depending on the average number of nonzero coefficients per block, is shown in Table I.

FRAME RATE THAT CAN BE RECONSTRUCTED DEPENDENT ON THE NUMBER OF NONZERO COEFFICIENTS

Number of nonzero coefficients	1	2	3	6	12	32	64
Frames per second	970	646	485	277	149	58	30

TABLE 1

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	1548	4656	33%
Number of Slice Flip Flops	1749	9312	18%
Number of 4 input LUTs	2156	9312	23%
Number of bonded IOBs	37	232	15%
Number of BRAMs	10	20	50%
Number of GCLKs	1	24	4%

Power Utilization Summary:

On-Chip	Power (W)	Used	Available	Utilization (%)
Clocks	0.000	1	---	---
Logic	0.000	2150	9312	23.1
Signals	0.000	3189	---	---
IOs	0.000	37	232	15.9
BRAMs	0.000	10	20	50.0
Leakage	0.081			
Total	0.081			

Thermal Properties	Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)
	26.1	82.9	27.1

Device	
Family	Spartan3e
Part	xc3s500e
Package	fg320
Grade	Commercial
Process	Typical
Speed Grade	-4
Environment	
Ambient Temp (C)	25.0
Use custom TJA?	No
Custom TJA (C/W)	NA
Airflow (LFM)	0
Characterization	
PRODUCTION	v1.2,06-23-09

Supply Summary Source	Voltage	Total Current (A)	Dynamic Current (A)	Quiescent Current (A)
Vccint	1.200	0.026	0.000	0.026
Vccaux	2.500	0.018	0.000	0.018
Vcco25	2.500	0.002	0.000	0.002

	Total	Dynamic	Quiescent
Supply Power (W)	0.081	0.000	0.081

VI. CONCLUSION

This paper presents a novel architecture for the computation of 8×8 2D IDCT. Based on the distribution properties of the coefficient matrix, the symmetry properties of the DCT basis matrices, and the superimposition principle, an architecture that offers high computational speed with minimum number of required multiplications is established. The computational time required is variable and proportional to the number of nonzero coefficients, thus, the proposed architecture can be very attractive for low quality image/video decoding applications.

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