Carbon Nanotube Field Effect Transistor: Fabrication of Thin Film of SiO_2-Based Micro Cantilevers Dielectric Layer between the Channel and Substrate by Anisotropic Chemical Etching of (100) Single Crystal Si

Kuldeep Niranjan, Sanjay Srivastava, Jaikaran Singh, Mukesh Tiwari

Abstract*— the performance of the CNT-FET with variable channel length was modified by using the micro-cantilever/micro-bridge of SiO_2. The etching technique was used to prepare the micro cantilever of SiO_2 from the Si-substrate. We focus the idea about for the fabrication of the nano-device, in order to reduce the dielectric layer thickness. The channel length of the FET was altered along with the dimension of the substrate. One of the possibilities to reduce the thickness of the dielectric layer is either by etching processes or growing the oxide layer from the substrate through etching process. In this case Laser leaching process was used to reduce the thickness of the substrate. Various electrical properties like gate voltage, drain current, mobility, and device performance have been investigated. A better I-V characteristic was obtained with higher mobility in between the channel and used dielectric layer.

Index terms- Anisotropy, CNT-FET, Lateral growth, Micro-cantilever

I. INTRODUCTION

The dimensions of individual devices in an integrated circuit have been decreased by a factor of approximately two every two years, which was designed by Moore's law [1]. Silicon based MOSFET (Metal Oxide Transistor Field effect transistor) gives the better performance if sizes less than 60nm are common in the world wide research. Scaling down has faced serious limits related to fabrication technology and device performances as the critical dimension shrunk down to sub-22 nm range [2]. The limits involve electron tunneling through short channels and thin insulator films, the associated leakage currents, passive power dissipation, short channel effects, and variations in device structure and doping.. These limits can be overcome to some extent and facilitate further scaling down of device dimensions by modifying the channel material in the traditional bulk.

Device or developing a new structure which has/have minimum thickness must be considered to solve the problem [3]. For developing the better performance of the nanoelectronic device, either the shrinkage of the dimension of the existing

Revised Manuscript Received on September, 2012.

Kuldeep Niranjan, M.Tech Scholar (VLSI), SSSIST, Sehore (M.P.), India.

Prof. Jaikaran Singh, Professor & Head, Depatment of Electronics and Communication, SSSIST, Sehore (M.P.), Inida.

Dr. Sanjay Srivastava, Professor, Department of MSME, MANIT, Bhopal (M.P.), India.

Prof. Mukesh Tiwari, Dean Academic, SSSIST, Sehore (M.P.), Inida.

In this research work, we focus the idea about for the fabrication of the nano-device, in order to reduce the dielectric layer thickness. The channel length of the FET was altered along with the dimension of the substrate. One of the possibilities to reduce the thickness of the dielectric layer is either by etching processes or growing the oxide layer from the substrate through etching process. In this case Laser leaching process was used o reduce the thickness of the substrate. Various electrical properties like gate voltage, drain current, mobility, and device performance have been investigated.

II. THEORY AND MODELING

The voltage between the gate and the substrate (back gate) is V_{gb}, the potential drop across the oxides ψ_{ox1} and ψ_{ox2}, the surface potential in the substrate with respect to the back gate is ψ_{subs}, the potential across the CNT is ψ_{cnt}, and the work function difference between the gate and the substrate materials is ϕ_{ms}. The work function, ϕ_{ms} can be divided in two parts and is expressed as follows [4],

$$\phi_{ms} = \phi_{mc} + \phi_{cs'} \quad \text{..... (1)}$$

Where ϕ_{mc} and ϕ_{cs} are the work function differences between the metal gate and carbon nanotube materials and the carbon nanotube and substrate materials, respectively. If the electrodes are sufficiently separated (long-channel hypothesis), this latter region is flat band type, its energetic level being essentially determined by the nanotube capacitance, which is assumed to dominate over the insulator capacitance. Accordingly, the gate capacitance is dominated by the nanotube capacitance, yielding a surface potential $\phi_S = qV_{gs}$, where V_{GS} is the gate-source applied voltage and q the electron charge. Then the capacitance of the system is given by the following expression [5].

$$C_{ox} = \frac{2\pi\varepsilon_{ox}L}{\ln\left(\frac{t_{ox} + R_t + \sqrt{t_{ox}^2 + 2t_{ox}R_t}}{R_t}\right)} \quad \text{..... (2)}$$

To show how well the transistor turns on and off, trans-conductance 'g_m' and carrier mobility μ are calculated. The g_m is determined by [5]

$$g_m = \frac{dI_{ds}}{dV_g} \quad \text{.....(3)}$$

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication

With d*I*ds and d*V*g from the measured *I*ds-*V*g curve, a high trans-conductance *g*m=1.6 μS at low voltages for original FET is obtained. The value turns to 3.3 μS after applying BOE. Carrier mobility μ is often used to compare device properties, which can be calculated by [5]

$$\mu = \frac{g_m L^2}{C V_{ds}} \qquad \text{…….. (4)}$$

III. EXPERIMENT

Wet chemical etching is employed in various processing steps. For many discrete devices and integrated circuits of relatively large dimensions (> 3 μ), chemical etching is used to delineate patterns and to open windows in insulating materials. The dielectric layer of the SiO_2 beneath the channel is grown by the chemical etching process of Si in (100) direction. Due to chemical etching process, SiO_2 is grown on the surface of the silicon as microcantilevers or microbridges, anisotropic wet etching of Si substrate beneath the SiO_2 film creates free standing structures between the channel and the substrate. The SiO_2 micro cantilevers used for these experiments had been fabricated on n-type (boron-doped) Si wafers with the (100) orientation. Approximately 1 μm thermal oxide was grown on the Si substrate in oxygen ambient saturated with H_2O vapor. The temperature for the silicon oxide growth was 1115 °C. The cantilevers patterns were aligned to the prime wafer flat on the (100) Si substrate, *i.e.*, along the ⟨110⟩ direction. Two types of cantilevers and microbridges orientations were investigated: one parallel to the prime flat or aligned to the ⟨110⟩ direction and the other was oriented to the ⟨100⟩ direction, which is 45° from the prime wafer flat as shown in Fig.1. This micro cantilevers or microbridges are used as the dielectric layer in between the CNT and the substrate. The dimensions of the designed cantilevers and microbridges were 25, 50 or 100 μm in width and 1000, 500, 300, 200,100 or 50 μm in length used as a dielectric layer in CNTFET. Fig.2 shows the schematic diagram of the CNT-FET with strained channel length. The channel length of the CNT is strained due to use of the micro-cantilever of the minimum thickness as shown in Fig.2.The etching process was carried out using two alkaline solutions namely: a 25 wt. % aqueous TMAH solution or a 30 wt. % aqueous KOH solution. Long, aligned CNTs are directly grown by chemical vapor deposition (CVD) system on a silicon substrate by suing different types of the SiO_2 micro cantilevers in between the channel and the substrate. The original channel length of CNT-FET was 5μ (but not fixed), used with a fixed width. Different channel length was used to study the performance of the device. Due to use of different types of SiO_2 micro cantilevers, the CNT bears the strain and change the length of the length as shown in Fig.2. The etching solutions were put in a thermostat Pyrex glass vessel at the etching temperature of 80 °C (temperature stabilization ±0.5°C) for both solutions. The vessel was tightly sealed with a screw on lid which included a tap water cooled condenser, to minimize evaporation during the etching. During the etching, the wafer of Silicon was held in a Teflon holder in the horizontal position above a magnetic stirrer bar.

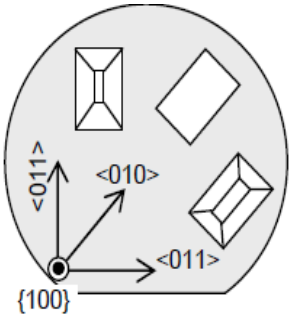

Fig.1. Different structure types which can be produced by anisotropic etching on a (100) Si substrate. Gray field represents the masking material (SiO2) [6]

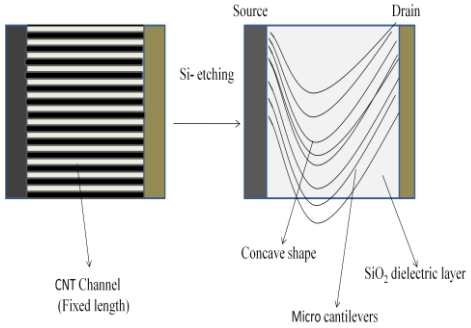

Fig.2 Schematic diagram of the strained CNT channel with dielectric layer as micro cantilever

IV. RESULT DISCUSSION

Multiple sheets of graphene may assemble in stacks, where by two adjacent sheets are held together weakly by dispersion forces and have an inter-layer spacing of about 3.35°A. The chiral vector begins and ends at equivalent lattice points, so that the particular (n_1; n_2) tube is formed by rolling up the vector so that its head and tail join, forming a ring around the tube. The length of C_h is thus the circumference of the tube, and the radius is given by the following formula and their variation is shown in Fig.3 along with band gap. With increase the chiral number, tube radius increases but band gap decreases [6].

$$R_t = \frac{|C_h|}{2\pi} = \frac{acc}{2\pi}\sqrt{3\left(n_1^2 + n_2^2 + n_1 n_2\right)} \qquad \text{…….(5)}$$

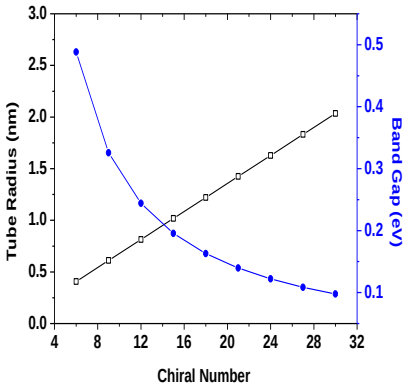

Fig.3 Variation of Tube radius and Eg with chiral Number ($n_1 = n_2$ and $\zeta = 30^o$))

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication

It is well known that Si exhibits a diamond cubic structure and its anisotropic etching behavior strongly depends on the crystal orientation [**7**].The family of {100} planes in silicon posses fourfold symmetry and their anisotropic etching can produce either vertical {100} walls or sloping {110} or {111} walls, inclined at 45° or 54.7°, respectively.[**8**]. Plane formation of a sidewall during anisotropic wet chemical etching is the one with the slowest etch rate aligned to the mask edge. When the pattern edge is aligned along the ⟨100⟩ direction, *i.e.*, 45° from the prime flat, the selection of walls bounded pattern depends on relative etch rates of the {110} and {100} planes. There is small difference between these two etch rates and they are very sensitive toward the employed solution, etching conditions, temperature, additives, impurities in solution, *etc*. The etched depths (*d*) on Si (100) substrate were measured using a micrometer gauge and the lateral distances were measured under an optical microscope as well as SEM. The method of evaluation of the etching rates of some crystallographic plane is illustrated in Fig. 4. By measuring the etching depth (*d*) in the ⟨100⟩ direction and knowing the etching time (τ), the etch rate of the (100) plane, $R\langle 100\rangle$, is calculated from the Equation:

$$R_{<100>} = d\tau^{-1} \quad (6)$$

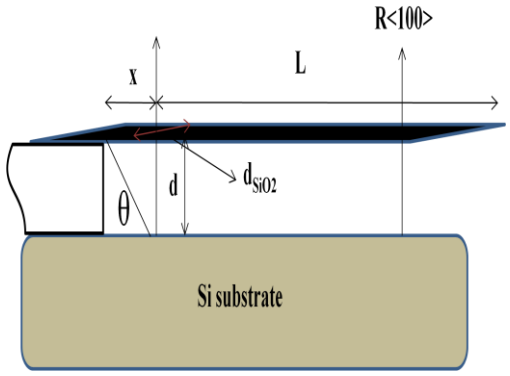

Fig.4. The method for estimating the etch rate of Si crystallographic planes. A SiO_2 micro cantilever is released by undercutting of the Si substrate

By measuring the distance *a*, which is the side wall projection on the (100) surface, the angle of inclination, θ, of the developed plane toward the (100) substrate surface can be estimated as

$$\theta = arctg\frac{d}{a} \quad (7)$$

This angle determines unambiguously which crystallographic plane has developed in the considered crystal direction. The etch rate of a developed sloped plane with {*hkl*} orientation can be estimated from the formula:

$$R_{<hkl>} = \frac{x\sin\theta}{\tau} \quad (8)$$

where *x* is the undercutting of the oxide mask. It is important to notice that *x* denotes not only the undercutting of the oxide mask, but also the distance which defines how ideally the micro cantilever is clamped. For ideally clamped micro cantilevers, *x* = 0. From the evolution of Si undercutting during the release of ⟨110⟩ oriented micro cantilevers, it can be seen that {111} crystallographic planes stop the undercut from the edge of the micro cantilevers. Hence, for ⟨110⟩ oriented micro cantilevers the undercutting results from the convex corner effect, this spreads along the cantilever length. This idea was used to develop the CNT FET with different channel length. Oxide thickness is the important parameter for judging the transport of electron through the channel. From this idea developed between the channel length and considered dielectric layer in the form of the micro cantilever, the I-V characteristics was plotted with different gate to source voltage show in Fig.5,and The variation of the oxide capacitance with thickness of the oxide layer is shown in Fig.6. The capacitance of the oxide layer decreases with increase the oxide thickness. That is, due to reduction in oxide thickness by the leaching process, the capacitance of the interface layer between the CNT channel and the dielectric layer approaches towards the higher values.

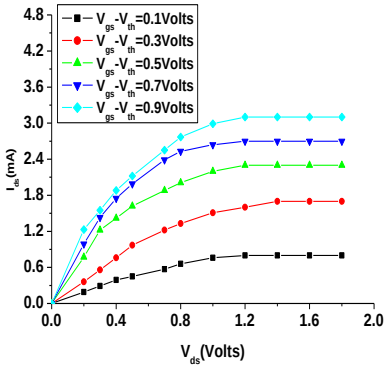

Fig.5. I-V characteristics was plotted with different gate to source voltage (for (10, 10) chiral number.

In Fig.7 Chiral number is the important parameter to affect the capacitance of the oxide layer. At 50 nm oxide thickness for long channel length CNTFET show the variation of the oxide capacitance with chiral number. The lower chiral number shows the higher capacitance between the oxide layer and the CNT channel. The alternation of the channel length is supposed to be brought by the removal of dielectric layer. This is due to channel length in between the source and drain. Due to removal of the layer, the CNT are stretched along the concave shape. The main part of the CNT remains contact with the substrate surface instead of hanging across the electrode gap, because there is no filed effect in the transistor with suspending channel. The etching of the oxide layer from the substrate shows the dramatic effect Fig2. Long channel shows the higher values of the capacitance as shown in Fig.8.

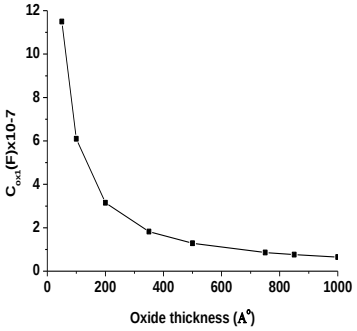

Fig.6. variation of the oxide capacitance with the chiral Number of the CNT

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication

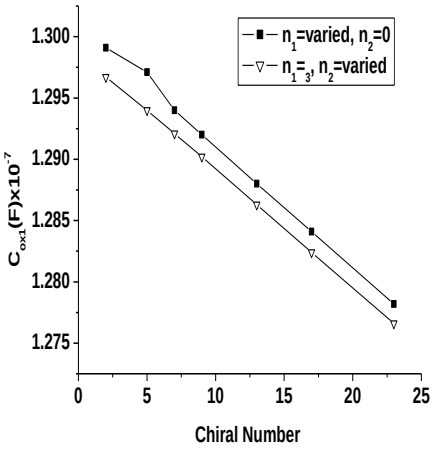

Fig.7. variation of the oxide capacitance with the chiral Number of the CNT

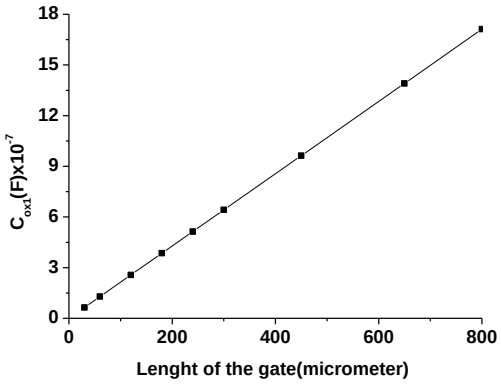

Fig.8. Variation of the oxide capacitance with the length of the gate (for (10, 10) chiral number.

Thin films of high-κ materials, such as ZrO_2 and HfO_2 (κ ~ 15–25), are highly desirable for gate dielectric integration in field effect transistors as they enable high ON-state current densities (speed) and low operating power consumptions. The lack of dangling bonds at the nanotube/high-κ interface and the weak noncovalent bonding interactions between the two materials, prevent any large perturbation of electron transport in carbon nanotubes. The integration of high-κ dielectrics, however, has been a challenging problem towards many researchers in planar MOSFETs because of the inherent mobility degradation of the Si channels

In CMOS FETs, the gate capacitance is actually the series combination of three terms, the oxide capacitance, the depletion capacitance of the gate electrode, and the capacitance to the carriers in the Si channel [9], as shown in Fig 10. These three capacitances add as

$$1/C = 1/C_{ox} + 1/C_{gate} + 1/C_{si} \quad (9)$$

As C varies as $1/t$, capacitances in series can be represented by a sum of effective distances. Thus we can define an effective capacitance thickness (of SiO_2) as

$$ECT = EOT + t_{gate} + t_{si} \quad (10)$$

The channel capacitance arises because quantum delocalization of the two-dimensional electron gas of electrons means that these electrons cannot lie infinitely close to the channel surface, but must delocalize a few Angstroms into the channel. On the other hand, the gate electrode is presently made out of degenerately doped polycrystalline silicon, for engineering convenience. Thus, its low carrier density gives a depletion depth which is a few ˚A, whereas a good metal has a higher carrier density and has a depletion depth of only 0.5 ˚A. This depletion effect can be removed by replacing the poly-Si with a normal metal. Typical metals for this use could be TiN, TaSiN and Ru. The metal is chosen primarily for its work function. One of the utmost significant developments in devices fabrication is that the gate dielectric have moved from silicon dioxide (SiO_2) to high-κ dielectrics such as ZrO_2, HfO_2, and Al_2O_3, which delivers high-performance transistors with low voltage and possibly hysteresis-free operation [10,11]. SiO_2 possesses network type of structure is bound with other units form cross linked polymer. This cross linking provides the better path to mobilize the electron from the channel, But these cross linking are not found in other type of the dielectric materials. One problem with high *K* oxides is that they contain much higher defect concentrations than SiO_2. The SiO_2 possessed such a low concentration of defects for three reasons, It's high heat of formation means that off stoichiometry defects such as O vacancies are costly and so are rare, The second is that SiO_2 has covalent bonding with a low coordination and third is The covalent bonding means that the main defects are dangling bonds, and the low coordination allows the SiO_2 network to relax to remove any dangling bonds by rebonding the network.

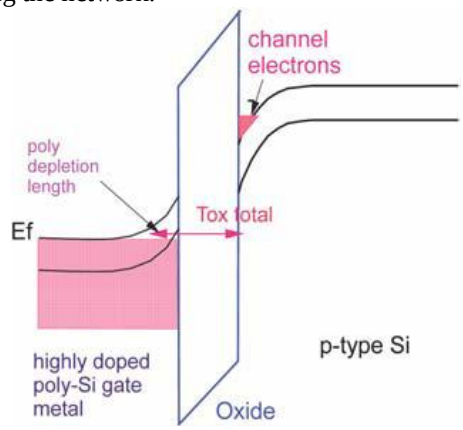

Fig.9. The three contributions to the capacitance of the gate/electrode stack; channel, dielectric and gate depletion.

This occurs in particular for defects at the Si: SiO_2 interface. The high *K* oxides differ in that their bonding is ionic rather than covalent, and they have higher coordination number. However, the non-equilibrium concentration of defects in acidic layer is high, because the oxide network is less able to relax, to rebond and remove defects [10] [11] [12].

At 100mV, Fig.10 shows the behavior of mobility of electron between the CNT channel (5μm, of (10, 10)) and dielectric interface of the different materials. The mobility of the electron get reduces with increase the dielectric constant of the materials. SiO_2 provides the better path for the electronic transport between the electronic channel and dielectric layer as compared to other high-κ dielectrics.

This effect can be seen in channel length modification of the CNT with chemical etching, which enhance the mobility of the electron between channels. Higher mobility is obtained at long channel length of the CNT between the source and drain which shows the linear relationship as shown in Fig.10.

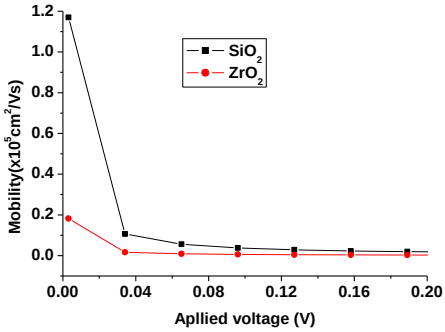

Fig: 10 Variation of the mobility with channel length (micrometer) of the CNT.

V. CONCLUSION

Behind this idea, the performance of the CNT-FET with variable channel length was modified by using the micro-cantilever/micro-bridge of SiO_2. The etching technique was used to prepare the micro cantilever of SiO_2 from the Si-substrate. CNT was used as channel in between the source and drain because of high mobility. This cantilever strains the channel of the CNT which is used in FET. A better I-V characteristic was obtained with higher mobility in between the channel and used dielectric layer. Length of the channel modifies the mobility as well as the oxide capacitance of the CNT channel. Substrate etching can make the device thinner and lighter without losing the performance. Higher channel length provides the better mobility at the thinner cantilever of the SiO_2 dielectric layer.

REFRENCES

[1] G. Moore 1975,"Progress in Digital Electronics," IEDM Tech Digest, 1975, pp 11-13.
[2] "International Technology Roadmap for Semiconductors" 2009 Edition.
[3] S.J.Wind, J.Appenzeller, and Ph. Avouris,"Lateral scaling in carbon-nanotube field-effect transistors," Phys. Rev. Lett., 91(5), pp .1058301-1058304, (2003).
[4] Chun-Wei Chen and Ming-Hsien Leede,"pendency of work function on the geometries of single-walled carbonnanotubes," 2004 Nanotechnology 15 480 doi:10.1088/0957-4484/15/5/013.
[5] J. Wildoer, L.Venema, A. Rinzler, R. Smalley, and C. Dekker, "Electronic structure of atomically resolved carbon nanotubes," Nature, vol. 391, pp. 59-62, January 1998.
[6] R. Bacon, "Growth, structure, and properties of graphite whiskers," Journal of Applied Physics, vol. 31, pp. 283-290, February 1960.
[7] M. Madou, "Fundamentals of micro fabrication," CRC Press, Boca Raton, 1997, p. 145.
[8] O. Powell, H. B. Harrison, J. Micromech. Microen., "Fabrication of SiO2-based micro cantilevers by anisotropic chemical etching of (100) single crystal Si," 11 (2001) 217.
[9] G. Wilk, R.M. Wallace, J.M. Anthony, "High-κ gate dielectrics: Current status and materials properties considerations," J. Appl. Phys. 89, 5243 (2001).
[10] J.D. Plummer, P.B. Griffin, "Material and process limits in silicon VLSI technology," Proc. IEEE 89, 240 (2001).
[11] M. Copel, M. Gribelyuk, E. Gusev, "Reaction of SiO2 with hafnium oxide in low oxygen pressure," Appl. Phys. Lett. 76, 436 (2000).
[12] M. Gutowski, J.E. Jaffe, C.L. Liu, M. Stoker, R.I. Hegde, R.S. Rai, P.J. Tobin, "Structure and stability of ultrathin zirconium oxide layers on Si(001)," Appl. Phys. Lett. 80, 1897 (2002).

Published By:
Blue Eyes Intelligence Engineering
& Sciences Publication