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Optimised Architecture Implementation of Bidirectional Scanning in FPGA for Television

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Abstract- In the past, Field Programmable Gate Array (FPGA) circuits only contained a limited amount of logic and operated at a low frequency, but during last decade there has been a tremendous advancement in the fields of FPGAs circuits. Today FPGA are very fast, high density, and low power, suitable for implementing any kind of application. Bidirectional scanning is one of the novel techniques used in television to avoid the retrace or fly back period of the electron beam. This saves power consumed by the beam during retrace period. RTL using Very High Speed Integrated Hardware Description Language (VHDL) is used to implement bidirectional scanning in FPGA. The functional and timing simulations of design are verified using Modelsim Simulator. Integrated software environment (ISE) from Xilinx is used to generate net-list from RTL code. The power consumption of the design is calculated using Xilinx power calculator.

Index Terms- Bidirectional scanning, FPGA.

I. INTRODUCTION

There has been a rapid growth in the field of television during the last decade. Today we have different kind of television in market. Some of them are liquid crystal display (LCD), Plasma display (PDP), light emitting display (LED) televisions. All these displays have merits and demerits over each other in terms of brightness, contrast ratio, view angle, power and cost. The *cathode ray tube* (CRT) is still used in many applications because of low cost and contrast ratio it provides. Most of the applications still use CRT based displays.

There has been a stringent requirement to have low power in CRT circuits to keep the cost low. The CRT is based on raster scanning where each line is scanned from left to right and again beam fly-back left to scan next line. This fly-back of the beam to left consumes power. This power is reduced by using bidirectional scanning.

II. DESIGN

This paper describes the work carried out to implement an optimized architecture of bidirectional scanning for television in field programmable gate array (FPGA) for saving power. A standard video source which generates composite PAL-B interlaced video signal having 625 scanning lines and a vertical scanning frequency of 50 Hz signal was chosen as input source to validate the bidirectional scanning. PAL-B is 625 lines (575 active lines) x 720 (active pixel per line) standards at 50 Hz field frequency. FPGA being high density, low cost, low power, high speed and programmable is selected for implementation. The Bidirectional line scanning is achieved by scanning each odd numbered scan line from left to right and each even numbered scan line from right to left, thereby avoiding the necessity for retrace, or fly back. In order to avoid loss of intelligibility in displaying the video information received from a conventional source providing video information written only from left to right, the received video information is stored in memory by scan lines with each odd numbered line being read out in the same order as stored in memory and each even numbered line being read out in reverse order as stored in memory [3]. Timed control is provided for processing of the video information and display thereof with bidirectional scanning to the CRT, and geometric error correction is provided for both the horizontal and vertical scan generators.

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III. SYSTEM DESCRIPTION

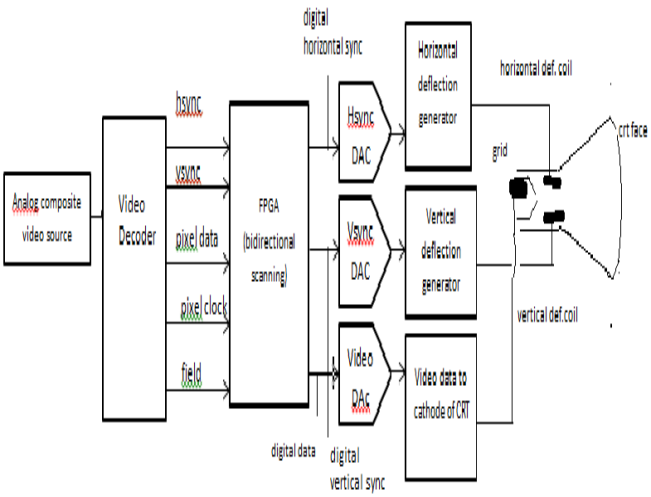

Fig. 1. System Block Diagram for CRT Driving

The system setup to check the bidirectional scanning consists of the following block:

A. Analog composite video source

This block Generate analog composite interlaced PAL-B signal at 50 Hz field frequency. A standard source that can generate various patterns like colour bars, stair, step, ramp pattern is selected for carrying out testing.

B. Video decoder

Converts analog composite signal to digital data, synchronized with timing information like pixel clock, h-sync, v-sync and field information suitable for interface to the Spartan3S1400an676 -4fgg device. This data is processed in FPGA using bidirectional scanning.

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C. DAC

The main function of DAC [7] is to condition the digital signal to analog form suitable for deflection circuits.

D. Deflection generator

The bidirectional analog hsync is applied to horizontal deflection generator to move the beam horizontally to scan the lines and unidirectional analog vsync is applied to vertical deflection generator to move the beam vertically to scan the frame .The processed pixel data is applied to high speed video DAC for converting to analog form.

This analog pixel data is amplified to suitable level before applying to the grid of the CRT to control the intensity of the beam.

IV. SIGNAL DESCRIPTION

Fig.2 below shows composite signal [6] with embedded hsync, vsync, field (pre-equalising pulses, serration pulses, post equalising pulses) and the blanking pulses. The 625 line frame is divided into two fields each of 312.5 lines, out of which 25 lines are blank in each field. These fields are called as odd and even field.

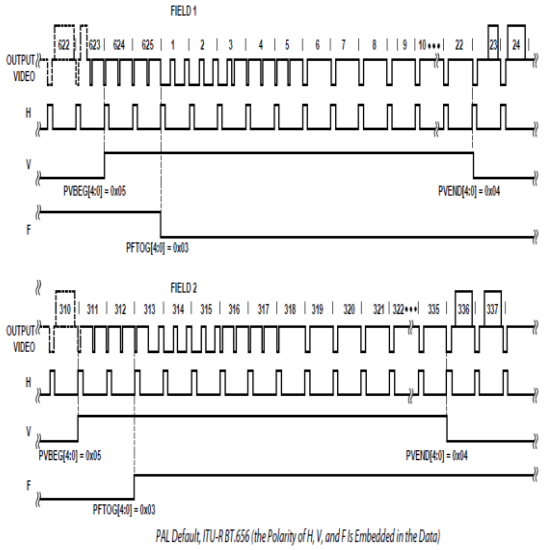

Fig. 2. PAL Default, ITU-RBT.656

The fig.3 shows the relation of pixel clock, data and hsync. As per table the output of video decoder [6] consists of 1728 pixels out of which 284 pixel are blanked in each hsync period. Each hsync period consists of 1440 pixel, 720 pixels each for Chroma and luma. SAV (start of active period) indicate the start of active pixel and EAV (end of active period) indicates the end of active pixel data.
The data is transferred at the rate of 27 MHz.

HS Timing Parameters

Standard	Characteristic: HS Begin Adjust HSB[10:0] (Default)	HS End Adjust HSE[10:0] (Default)	HS to Active Video LLC Clock Cycles, C in Figure 35 (Default)	Active Video Samples/ Line, D in Figure 35	Total LLC Clock Cycles, E in Figure 35
NTSC	0000000010b	00000000000b	272	720Y + 720C = 1440	1716
PAL	0000000010b	00000000000b	284	720Y + 720C = 1440	1728

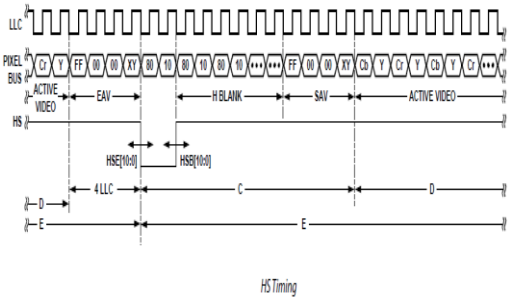

Fig. 3. HS Timing

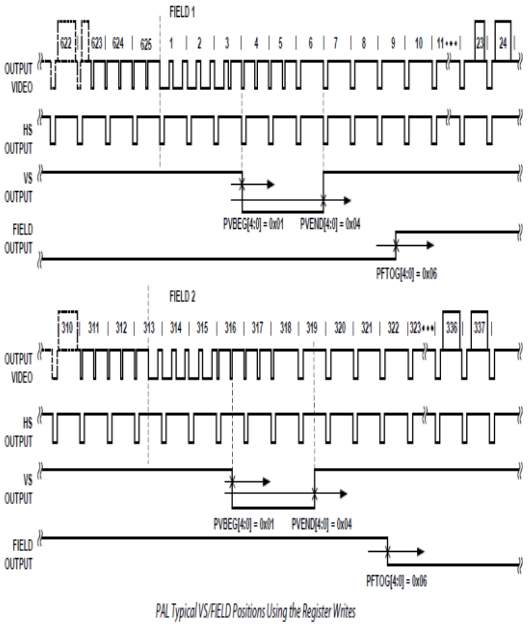

Fig.4. PAL Typical VS/Field Positions

The analog composite signal is digitized using a decoder that generates digital data, hsync, vsync, field, pixel data and pixel clock. The architecture uses two internal block rams of FPGA for storage of 720 pixel information of two consecutive lines. Two counters are used to generate the address of these block rams and for the generation of bidirectional ramps for scanning. The horizontal- ramp is implemented to be bi-directional. This is accomplished as following: the digitized video information corresponding to two consecutive (even and odd) lines is stored into a buffer. The buffered lines are then read in such a way that odd line data is outputted from left to right and the even line data is outputted in the reverse manner .Whenever video information from the odd line is outputted, an up-counter is triggered by the H-sync. However when an even line is outputted, a down-counter is triggered. The output of up and down counter gives rise to up and down counting for horizontal-ramp on every H-sync.

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The video and horizontal-ramp being triggered by same H-sync and same clock, the information is synchronized to the pixel level. The bi-direction horizontal ramp is applied to a Digital to Analog conversion before feeding to horizontal deflection generator. The deflection generator produces proportional current to deflect the beam in horizontal direction. When the odd lines are displayed the beam traverse in forward direction and when even lines are displayed it traverse in reverse direction. This scanning process is depicted below [1]

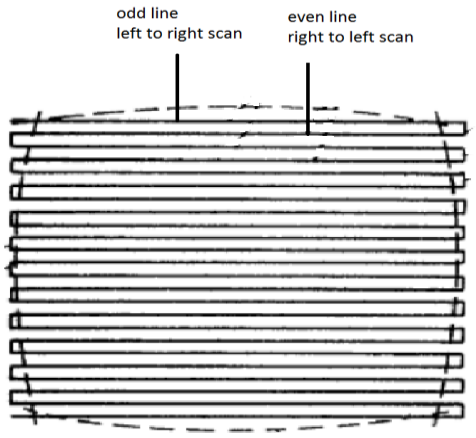

Fig.5. Pictorial representation of bi-directional scanning.

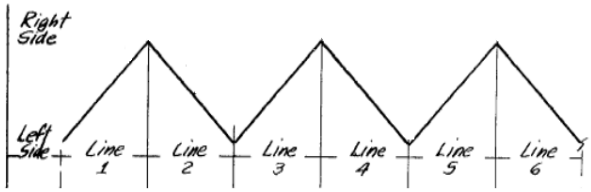

Fig. 6. Bidirectional Horizontal Ramp

The vertical- ramp is generated by simply implementing an up counter which is reset on every V-sync pulse received from decoder .The vertical-ramp is applied to a vertical generator which produces a proportional current to move the beam from top to bottom.

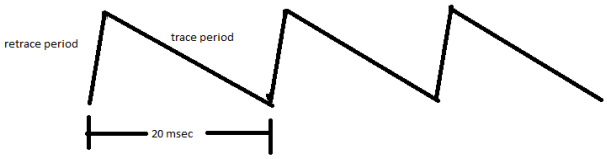

Fig.7. Vertical Ramp

V.ARCHITECTURE BLOCK DIAGRAM

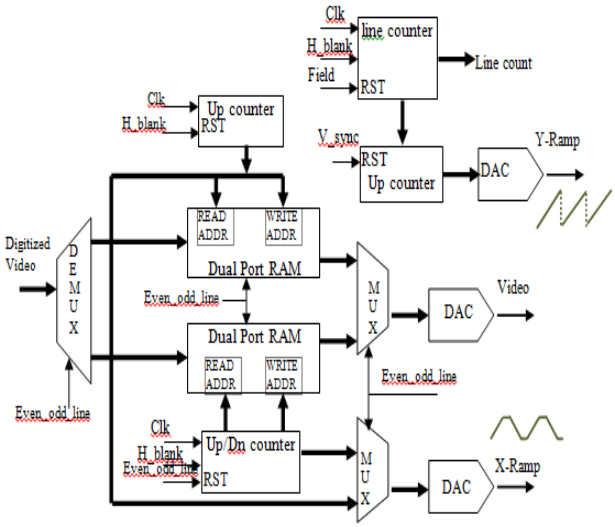

Fig. 8. Architecture Block Diagram

The architecture consists of De-mux block that selects even and odd memory as per the status of even and odd selection line. Dual port memory having separate read and write port is used for reading and writing of data .An up counter that counts from 0 to 719 is used to store the 720 pixel data in the two dual port memory. The two memories are used in ping pong fashion. When data is written in one memory, data is read from the other memory. The data is written from 0 to 719 pixels using an up counter in both the memory and read using up counter in odd memory and down counter that counts from 719 to 0 in case of even memory. The ramp is generated as per the reading of data to accomplish bidirectional scanning.

The design is synthesised using ISE (integrated software environment) from Xilinx and targeted to low cost Spartan3an FPGA. The synthesis report is attached below.

The design has been validated on a Spartan3an development kit and the results are shown in table1. The results show that the resources of FPGA utilized are, number of slices of flip flop is 1%, number of 4 input look up table is 1%, number of block ram 2 i.e. 6%.

Table. 1. Synthesis Report

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	185	22,528	1%	
Number of 4 input LUTs	135	22,528	1%	
Number of occupied Slices	120	11,264	1%	
Number of Slices containing only related logic	120	120	100%	
Number of Slices containing unrelated logic	0	120	0%	
Total Number of 4 input LUTs	177	22,528	1%	
Number used as logic	117			
Number used as a route-thru	42			
Number used as Shift registers	18			
Number of bonded IOBs	61	502	12%	
Number of BUFGMUXs	1	24	4%	
Number of RAMB16BWEs	2	32	6%	
Average Fanout of Non-Clock Nets	2.27			

Table. 2. Power Consumption Table

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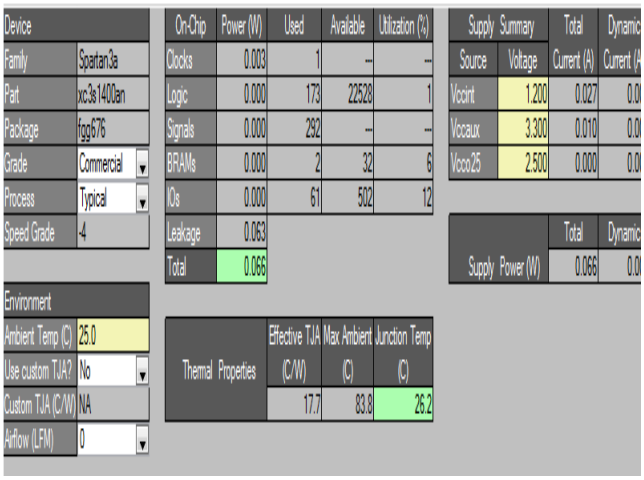

A deflection circuit for a television picture tube comprises a horizontal generator producing a first, symmetrical output current. A corrective current is generated from the first output current. The corrective current and the first output current change in value oppositely to one another at times. A vertical generator produces a second output current. The second output current and the corrective current are summed to form a composite current having a stair step configuration. An amplitude control circuit for the composite current adjusts horizontal segments of the stair step. A composite control signal for the amplitude control circuit is developed from the horizontal and vertical generators. A vertical sweeping coil is coupled to the amplitude control circuit and controlled by the composite current

VI. TEST RESULTS

The Fig. 9 below shows the wave form of 100 % vertical bar pattern generated through a standard pattern generator.

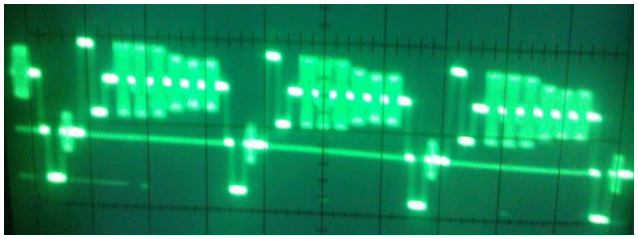

Fig. 9. Composite Analog PAL- B Signal

The Fig.10 below shows that the data is read in the same fashion as it is stored in odd memory and read in the reverse order in even memory.

Fig. 10. Bi-directional Processed Data

The Fig.11 below shows the composite analog step signal generated through standard pattern generator.

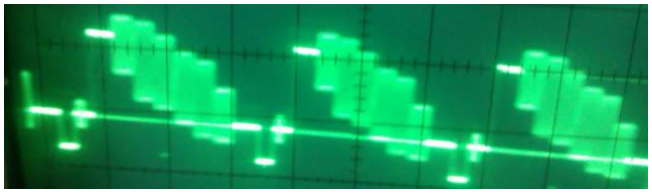

Fig.11. Composite PAL-B Signal

The Fig.12 below shows that the data is read in the same fashion as it is stored in odd memory and read in the reverse order in even memory.

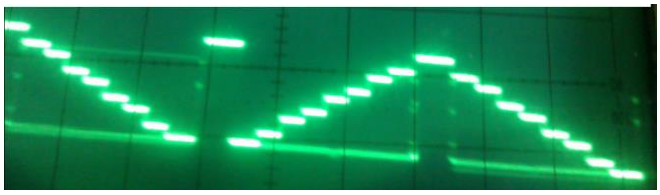

Fig.12. Bidirectional processed data

V11. CONCLUSION

A low latency and power efficient approach was presented for processing the digital video data in reconfigurable hardware (FPGA). The synthesis report suggests that the design only utilizes 1% of the logic of FPGA and consumes only 66mW of power. It is proposed that the above hardware can be implemented on the platform like ASIC (application specific integrated circuits) that can further reduce the power consumption of the bidirectional scanning implementation.

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