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An Area Efficient, High Speed Novel VHDL Implementation of Linear Convolution of Two Finite Length Sequences Using Vedic Mathematics

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Abstract - This paper presents a novel method of implementing linear convolution of two finite length sequences (N×N) in hardware using hardware description language (VHDL). The proposed method uses modified design approach by replacing the conventional multiplier by Vedic multiplier internally in the implementations. The proposed method is efficient in terms of computational speed, hardware resources and area significantly. The efficiency of the proposed algorithm is tested by simulations and comparisons with different design approaches using XILLINX software. The presented circuit consumes less power and has a delay of 17ns from input to output. The proposed circuit is also modular, expandable and regular which provides flexibility to form different number of bits.

Keywords- N×N, VHDL, XILLINX.

I. INTRODUCTION

Many digital signal processing applications require convolution operations for filtering of signals. The existing methods of hardware implementation of linear convolution sum affects the performance of DSP system because of higher delay, area and power requirements. In this paper, a novel method of computing discrete linear convolution is using Vedic multiplication technique is presented. The increased speed convolution algorithm in VHDL also improves level of abstraction. The mathematical formula to find linear convolution is fundamentally similar to *URDHWA TIRYAGBHYAM* sutra in Vedic mathematics.

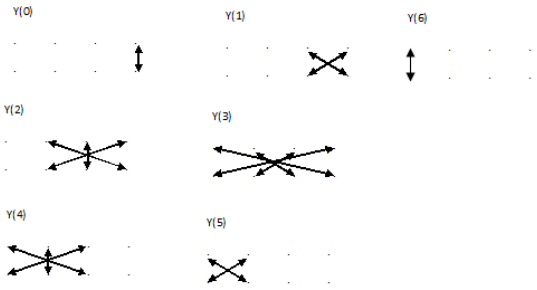
The organization of paper is as follows: Section II introduces the method and properties of linear convolution. Section III investigates Vedic mathematics and URDHWA TIRYAGBHYAM sutra in detail. In section IV the circuit implementations of proposed design are presented. Section V presents the verification and results achieved. Finally the conclusion is obtained.

II. INTRODUCTION TO DISCRETE LINEAR CONVOLUTION

The linear convolution is a basic operation in DSP which relates input signal and impulse response to obtain desired output. Consider two finite length sequences x(n) and h(n) on which the convolution operation is to be performed with lengths l and m respectively. the output of convolution operation y(n) contains l+m-1 number of samples.the formula for calculating discrete linear convolution is

$$y(n) = \sum_{k=-\infty}^{\infty} x(k)h(n-k)$$

e.g.consider x(n)={1,2,3,4} and h(n)={2,1,2,1}here,l=4, m=4
thus, length of output=4+4-1=7
output y(n) will have 7 samples calculated as:
y(0)=x(0)h(0)=4*1=4
y(1)= x(0)h(1) +x(1)h(0)=3*1+2*4=11
y(2)=x(0)h(2)+x(1)h(1)+x(2)h(0)=2*1+2*3+4*1=12
y(3)=x(3)h(0)+x(2)h(1)+x(1)h(2)+x(0)h(3)
=4*2+3*1+2*2+1*1=16
y(4)=x(1)h(3)+x(2)h(2)+x(3)h(1)=1*2+2*1+3*2=10
y(5)= x(2)h(3)+ x(3)h(2)=1*1+2*2=5
y(6)= x(3)h(3)=1*2=2
the final output of convolution is
y(n)= ={2,5, 10, 16 , 12, 11, 4,}



Thus, the partial output can be found out by vertical and crosswise multiplication.[1]

III. VEDIC MATHEMATICS

Vedic Mathematics is useful in many engineering application areas especially in signal processing. It describes 16 sutras and sub-sutras which cover all the branches of mathematics such as arithmetic, algebra, geometry, trigonometry, statistics etc.

Implementation of these algorithms in processors has found out to be advantageous in terms of reduction in power and area along with considerable increase in speed requirements.[2]

These Sutras are given in Vedas centuries ago. To be specific, these sutras are described in ATHARVA-VEDA. The sutras and sub-sutras were reintroduced to the world by Swami Bharati Krishna Tirthaji Maharaja in the form of book Vedic Mathematics.
16 Sutras in Vedic mathematics

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Pronunciation	Ancient Sanskrit	Meaning
Ekadhikena Purvena	एकाधिकेन पूर्वेण	By one more than one before
Nikhilam Navatshcharam am Dashata	निखिलं नवतश्चरमम दशतः	All form 9 and the last from 10
Urdhwam Tiryagbhyam	उर्ध्वम् तिर्यग्भ्यां	Vertically and cross-wise
Paravartya Yojayet	परावर्त्य योजयेत्	Transpose and apply
Shunyam Samyasamuchchaye	शून्यं सांम्यंसमुच्चये	If the samuchchaya is same it is zero.
Anurupye Shunyam Anyat	अनुरुप्ये शून्यं अन्यत	If one is zero,the other is ratio
Sankalana Vyavakalanabhyam	संकलन व्यवकलनाभ्यां	By addition and by subtraction
Poornapoornabhyam	पूर्णापूर्णाभ्यां	By the completion or non completion
Chalanakalanabhyam	चलनकलनाभ्यां	Differential calculus
Yavadoonam	यावदुनं	By the deficiency
Vyashtisamashtihi	व्यष्टिसमष्टिहि	Specific and general
Sheshani Ankena Charamena	शेषाणि अङ्केन चरमेन	The remainders by the last digit
Sopantyadayam Antyam	सोपान्त्यदयं अन्त्यं	The ultimate and twice the penultimate
Ekanyunen Purvena	*एकन्युनेन पुर्वेन*	By one less than one
Gunita Samuchchayaha	गुणित समुच्चयः	Product of the sum
Gunaka Samuchchayaha	गुणक समुच्चयः	All the multipliers

URDHVA TIRYAGBHYAM SUTRA –

The sutra means vertically and crosswise. Consider 2 bit binary numbers which needs to be multiplied. (a1 a0)× (b1 b0)

a1 a0
× b1 b0

a1*b1:a1b0*a0b1:a0*b0

Thus we get result as P3P2P1P0 where
P0=a0*b0
P1=a0*b1+a1*b0
P2=a1*b1
P3=carry

The sutra states that find vertical and crosswise partial products and add them to get the product term at proper place. This can be explained further by an example.

1 0
× 1 1

1 1 0

Thus the sutra can be formulated as

$$P_j = \sum_{i=0}^{N-1} a_i * b_{j-i}$$

4*4 Vedic Multiplier

The 4*4 Vedic multiplier will multiply two 4-bit binary numbers. The product will have 8 bits which can be calculated as follows:

Step1 Find P0

A3 A2 A1 A0

B3 B2 B1 B0

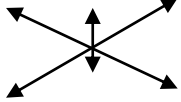
Step2 Find P1

A3 A2 A1 A0

B3 B2 B1 B0

Step3 Find P2

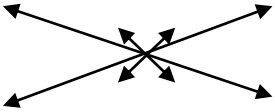
A3 A2 A1 A0



B3 B2 B1 B0

Step4 Find P3

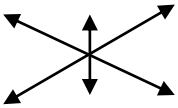
A3 A2 A1 A0



B3 B2 B1 B0

Step5 Find P4

A3 A2 A1 A0



B3 B2 B1 B0

Step6 Find P5

A3 A2 A1 A0

B3 B2 B1 B0

Step4 Find P6

A3 A2 A1 A0

B3 B2 B1 B0

Thus, the product terms can be calculated as
P0=a0*b0
P1=a0*b1+a1*b0+prevcarry
P2=a0*b2+a1*b1+a2*b0+prevcarry
P3=a0*b3+a1*b2+a2*b1+a3*b0+prevcarry
P4=a1*b3+a2*b2+a3*b1+prevcarry
P5=a2*b3+a3*b2
P6=a3*b3

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IV. CIRCUIT IMPLEMENTATION AND PROPOSED DESIGN

For hardware implementation of linear convolution of two sequences (N×N) N=4 is taken for testing . thus, each sequence has 4 samples and every sample is represented by 4 bits. The multiplication of intermediate products will be done using Vedic Multiplier.The output of a 4*4 bit multiplier will be 8 bits. Thus, each sample in convolution output will have 8 bits. Hence convolution output is stored in an array of where each element is represented by 8 bits. The algorithm is coded in VHDL and tested by performing simulations using XILLINX 13.1software.

Algorithm for linear convolution

Where, l=length of x(n)

m=length of h(n)

N=l+m-1=length of output

1. Start
2. Initialize sum=0,result array={0,0,0,0,0,0,0}
3. For i in 0 to N-1 do
4. Sum=0
5. For j in 0 to l-1 do
6. For k in m-1 to 0 do
7. If (i=j+k) then product=x(k)*h(k-j)----------this product will be calculated using Vedic multiplier.
8. Sum=sum+product
9. End loop k;
10. End loop j
11. Result(i)=sum
12. End loop i;
13. End

V. DESIGN VERIFICATION

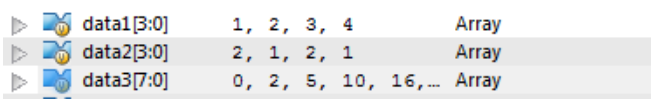
Design verification and testing is done using XILLINX 13.1 software and ISIM simulator.The inputs to the convolution design are stored in two arrays x and h which contains 4 samples each. Every sample in an array is represented by 4 bits for the simplicity of design verification. The number of bits can be increased for increasing resolution and accuracy of the circuit. The design has been tested for the same example i.e. x={1,2,3,4} and h={2,1,2,1}

Thus for vhdl coding

x=0001 0010 0011 0100

h=0010 000100100001

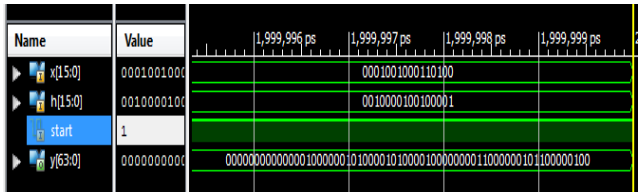
The convolution operation is performed on x and h using 4*4 vedic multiplier for finding samples in the output sequence.the result of 4*4 bit multiplication is stored in variable with 8 bits. The output of the convolution operation is stored in an array of 8 elements each contacting 8 bit sample value. the output of convolution is y={2,5, 10, 16 , 12, 11, 4,}

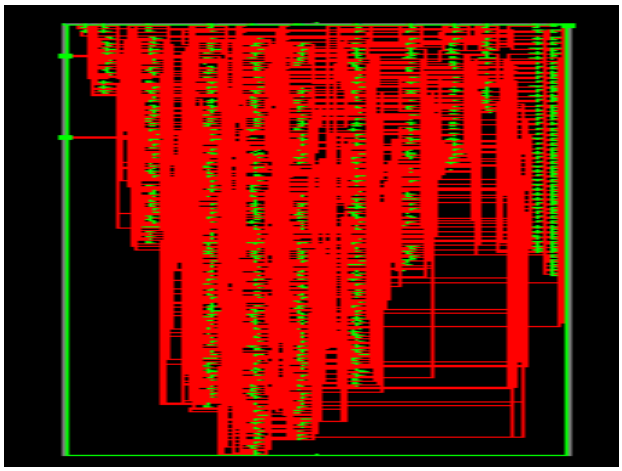


VI. RESULTS

	Array multiplier	Vedic Multiplier	% improvement
Number of Slices:	382 out of 4656 8%	191 out of 4656 4%	50
Number of 4 input LUTs:	677 out of 9312 7%	343 out of 9312 3%	49.33
Number of bonded IOBs	97 out of 232 41%	97 out of 232 41%	0
Offset	19.510ns	16.690ns	14.45
Levels of Logic	18	16	11.11
Total memory usage	1193408 kilobytes	194112 kilobytes	83.73

The results are obtained by synthesizing the design arameters using XILLINX 13.1 software.Table 2 shows the performance analysis of 4*4 Vedic convolution algorithm using array multiplier and Vedic multiplier. The implementation using Vedic multiplier reduces total area, memory usage and delay compared to existing methods.[3]





VII. CONCLUSION

In this paper, an optimized design for linear convolution is presented. This design model has advavantage of fine tuning depending on the requirement for enhancing the signal processing model.This implementation also improves the efficiency of the model design in terms of area and speed requirements.The proposed system design is coded using VHDL language and synthesized for FPGA products with XILLINX 13.1 software. The proposed design is tested for 4×4 discrete convolution using ISIM simulator. The proposed system saves 50% area and it takes 17 ns to complete.The presented concept can be extended on N×N discrete convolution. The modularity and reconfigurability of FPGA makes the design compatible for future improvements.

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