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A Novel 1-Bit Full Adder Design Using DCVSL XOR/XNOR Gate and Pass Transistor Multiplexers

P. Divakara Varma, R.Ramana Reddy

Abstract*— *Adders are the basic building blocks in digital computer systems. Arithmetic operations are widely used in most digital computer systems. Addition is a fundamental arithmetic operation and is the base for arithmetic operations such as multiplication and the basic adder cell can be modified to function as subtractor by adding another xor gate and can be used for division. Therefore, 1-bit Full Adder cell is the most important and basic block of an arithmetic unit of a system. Hence in order to improve the performance of the digital computer system one must improve the basic 1-bit full adder cell. There is always a trade-off between speed and power dissipation in VLSI Design. To achieve high speeds, high drivability hybrid-DCVSL design methodologies are used to build adder cell in this work. Static CMOS, DCVSL adders are compared with hybrid XOR and XNOR based hybrid adder cell for delay, power dissipation and number of transistors utilized. The hybrid adder is designed using DCVSL gates because these can produce both complementary and true outputs using single gate architecture. The multiplexers in the design are based on the pass transistor logic (PTL) because these are simple to construct and occupies less chip area per component.

***Index Terms*—DCVSL, Multiplexer, PTL, XOR/XNOR**

I. INTRODUCTION

Low power and High speed are the design trade-offs in VLSI industry. Until recently performance has been synonymous with speed. Emergence of portable computing devices are enhancing the importance of low power design methodologies. In pass transistor logic, the transistors are used as voltage controlled switches to implement the logic. The PTL logic is bidirectional. There is no static power dissipation in PTL gates. The pass transistor logic suffers logic degradation at the output by an amount of Threshold Voltage (Vth). The advantage of Differential Cascode Voltage Switch Logic (DCVSL) is that it produces both true and complementary outputs when provided with true and complementary inputs. In DCVSL logic gates there is no static power dissipation (unlike static CMOS Ciruits). The hybrid Adder cell utilizes DCVSL logic for generation of XOR and XNOR outputs and PTL logic is used for the design of 2:1 multiplexer unit.

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II. EXISTING ADDER DESIGNS

Basic full adder design

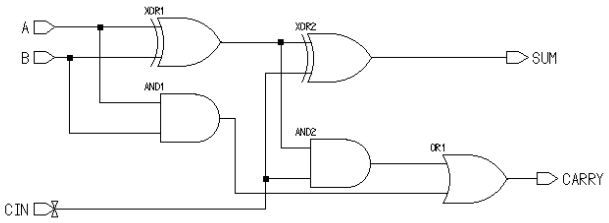

Fig. 1. Basic full adder

General expression for full adder is

$$\text{Sum} = A \oplus B \oplus C_{IN} \quad (1)$$
$$\text{Carry} = A{\cdot}B + A{\cdot}C_{IN} + B{\cdot}C_{IN} \quad (2)$$

From the basic full adder design shown in Fig. 1. sum is obtained by performing the Exclusive-OR function on all the inputs and Carry output is equal to same logic state when any two inputs are assigned with same state.

A. *Static CMOS full adder*

The Schematic Diagram of a 1-bit Static CMOS full adder cell is shown in Fig.2.

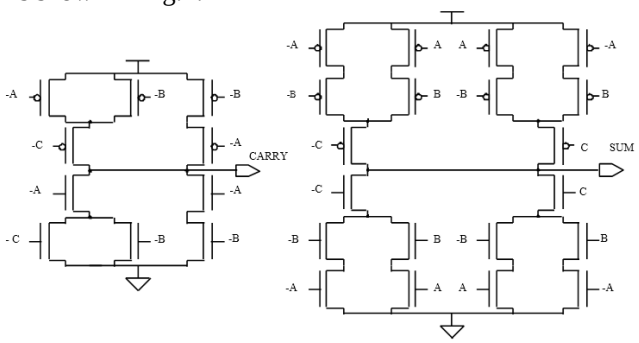

Fig. 2. Static CMOS 1- Bit full adder

The static CMOS consists of Pull-Up and Pull-Down networks. The PMOS transistors in Pull-Up network is the dual network of the NMOS Transistors in Pull-Down network.

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The "-" sign on input terminals indicates the complementary signals. The advantage of CMOS logic is that it dissipates less dynamic power. The disadvantage of static CMOS logic is the higher propagation delays and require 2n transistors where n is the number of inputs and larger chip area and also suffers with low fan-out capability.

B. DCVSL full adder

Static DCVSL is a differential method which requires both true and complementary signals to be routed to gates. Two complementary nMOSFET switching trees are constructed to a pair of cross-coupled pMOSFET transistors. Depending on the differential inputs one of the outputs is pulled down by the corresponding nMOSFET network. The differential output is then latched by the cross-coupled pMOSFET transistors. Since the inputs drive only the nMOSFET transistors of the switching trees, the input capacitance is typically two or three times smaller than that of the conventional static CMOS logic. The advantage of DCVSL is in its logic density that is achieved by elimination of large pMOSFETs from each logic function. Both pull down networks in the Fig. 3 will never conduct at the same time.

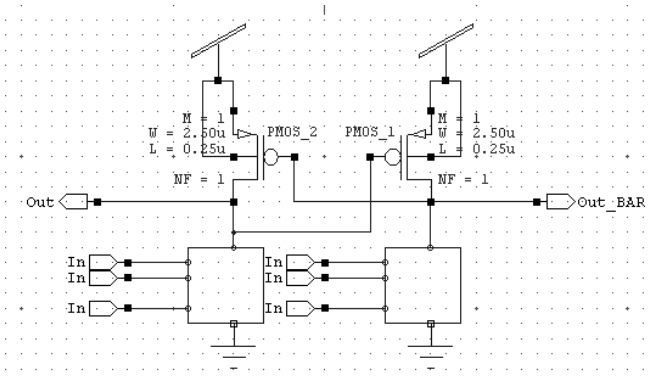

Fig. 3. Basic architecture of DCVSL Logic

Fig. 4 shows the circuit diagram of the static DCVSL full adder.

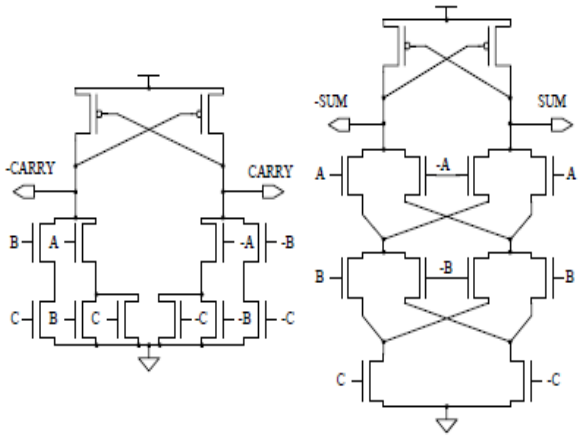

Fig 4. Full adder implementation using DCVSL Logic

III. 1-BIT FULL ADDER IMPLEMENTATION METHODOLOGIES

1-bit full adder can be implemented using

1. Two XOR gates and one 2:1 Multiplexer
2. Two XNOR gates and one 2:1 Multiplexer
3. One XOR gate, XNOR gate and two 2:1 Multiplexers.

Method -1

1-bit full adder using Two XOR gates and one 2:1 Mux

Expressions for Sum and Carry are given by equations (1) & (2). These can be rewritten as

$$Sum = X \oplus C_{IN} \quad (3)$$

where $X = A \oplus B$

$$Carry = A \cdot X' + C_{IN} \cdot X \quad (4)$$

where X' is complement of X

Hence Sum can be implemented using two XOR gates. Carry can be implemented using a 2:1 multiplexer with A and C_{IN} as input lines and X as selection line. The implementation is as shown in Fig.5.

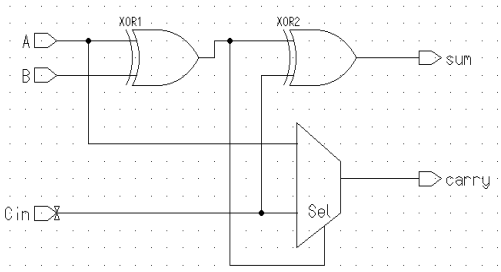

Fig. 5. 1-bit Full adder with XOR and 2:1 Multiplexers

Method -2

1-bit full adder using Two XNOR gates and one 2:1 Mux

Expressions for Sum given in equations (3) can be rewritten as

$$Sum = (X' \oplus C_{IN})' \quad (5)$$

Hence Sum can be implemented using two XNOR gates. Carry can be implemented using a 2:1 multiplexer with A and C_{IN} as input lines and X' as selection line. The implementation is as shown in Fig.6.

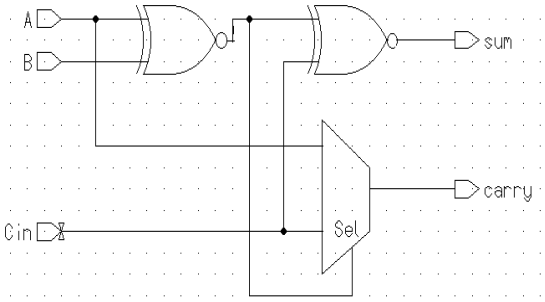

FIG. 6. 1-BIT FULL ADDER WITH XNOR AND 2:1 MULTIPLEXERS

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Method -3

1-bit full adder using one XOR gate, one XNOR gates and two 2:1 Mux

In this method the expressions for Sum is obtained from expanding the equation (3) and carry is obtained from expression

$$Sum = X' C_{IN} + X C_{IN}' \quad (6)$$

and

$$Carry = A \cdot X' + C_{IN} \cdot X$$

The implementation is as shown in Fig.7.

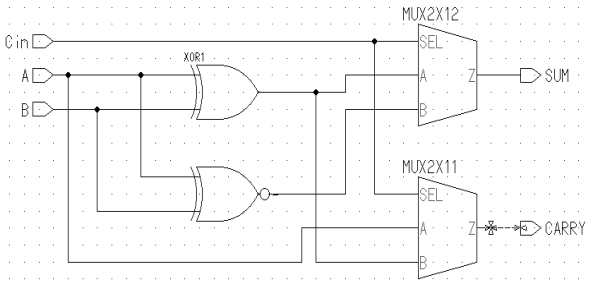

Fig. 7. 1-bit Full adder with XOR, XNOR Gates and 2:1 Multiplexers

1-bit full adder in this paper is implemented using method 3 and designed using a DCVL XOR/XNOR gate. The advantage of DCVSL gates is that these gates can produce both true and complementary outputs i.e., both X and X', provided that true and complimentary inputs are available.

The 2:1 multiplexer is designed using pass transistor logic. The advantage of pass transistor logic is that it can be implemented using very less number of transistors, hence very less power dissipation. Lower noise margin is the disadvantage of Pass Transistor logic.

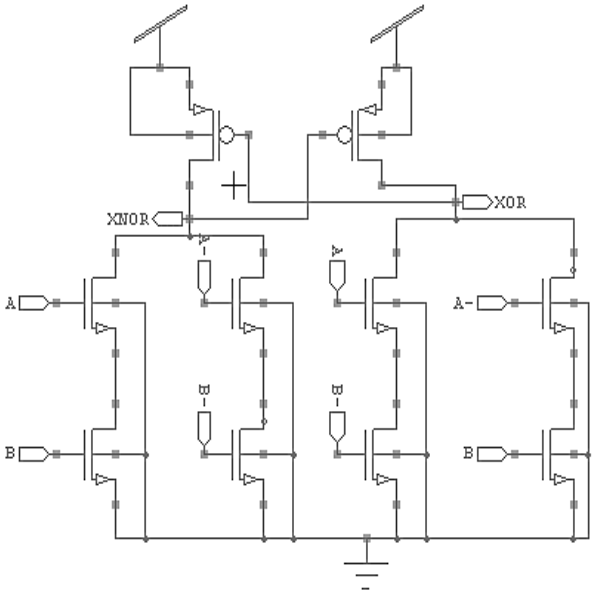

Fig. 8. XOR/XNOR implementation using DCVSL

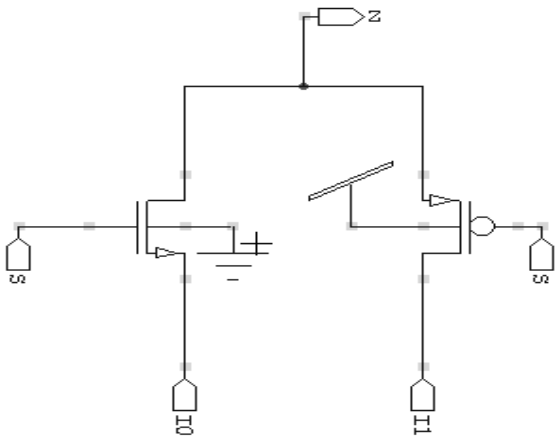

Fig. 9. Multiplexer implementation using Pass Transistor Logic

Final circuit of 1-bit full adder using DCVSL gates and 2:1 Multiplexer is given below.

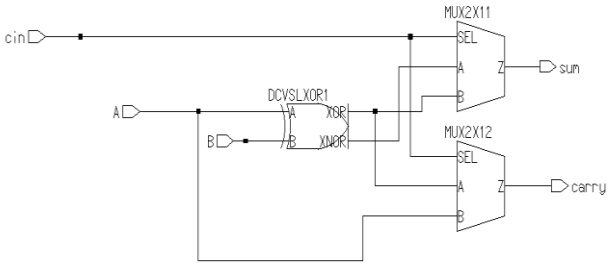

Fig. 10. 1-bit full adder implementation

IV. EXPERIMENTAL RESULTS

Extensive Simulations are carried out on Static CMOS adder as base case and performances of DCVSL and hybrid Full adder circuits are compared with that of base case. The simulations are carried out to calculate average power dissipation and delay using a set of input vectors for equal time periods. Tanner EDA tools are used to extract netlist and HSPICE software is used to carry out simulations.

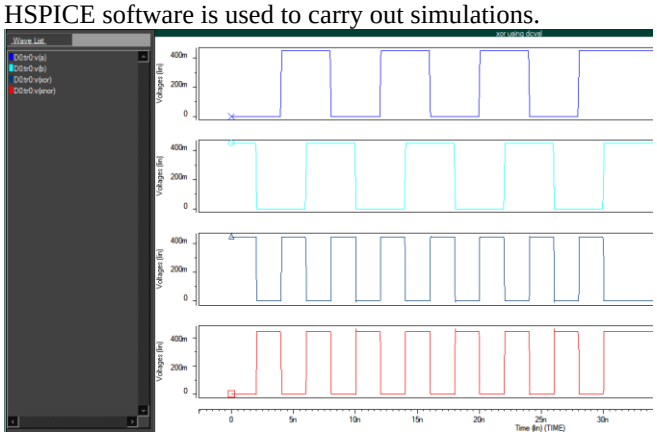

Fig 11. Waveforms of DCVSL XOR/XNOR gate

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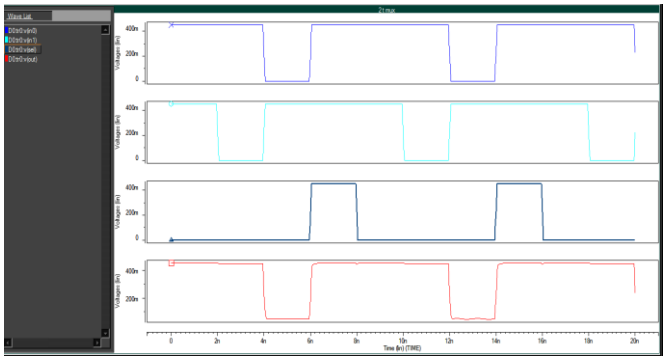

Fig 12. Waveforms of 2:1 Mux using Pass Transistor Logic

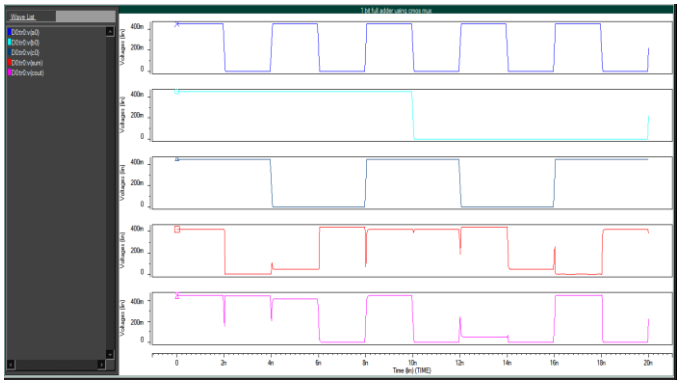

Fig 13. Waveforms of 1- bit fulladder using DCVSL XOR/XNOR gate and PTL 2:1 multiplexers

Table I. Experimental results

	Delay (sec)	Power dissipation (Watts)	No. of Transistors
Static CMOS	2.29E-11	3.05E-06	36
DCVSL	1.36E-11	8.38E-06	30
XOR/XNOR and Mux Based	1.98E-12	2.96E-06	12

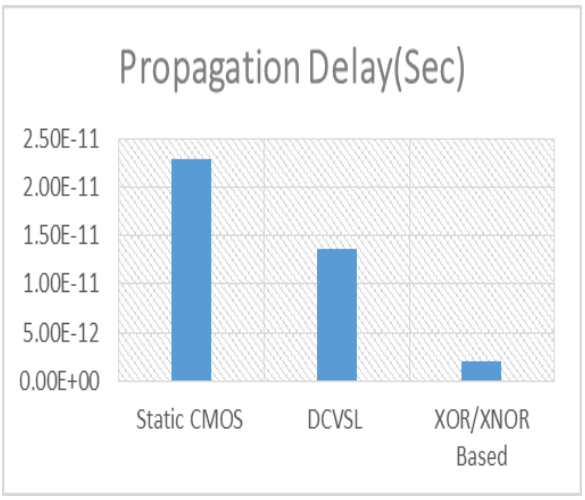

Fig. 14. Implementation technique Vs Propagation Delay

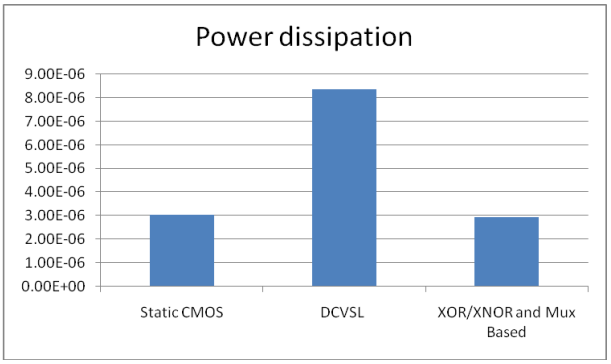

Fig. 15. Implementation technique Vs Dynamic Power dissipation

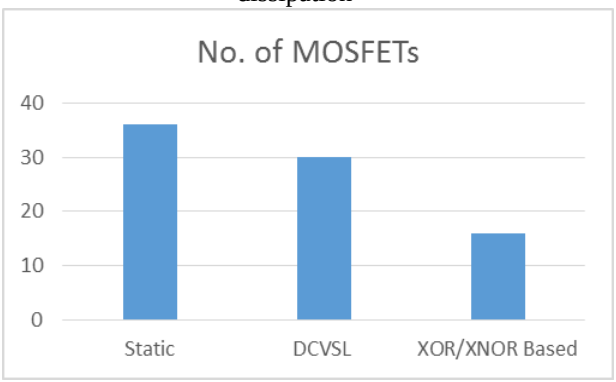

Fig. 16. Implementation technique Vs No. of MOSFETs required

V. CONCLUSIONS

From the results it can be observed that the propagation delay and number of transistors required is reduced in 1-bit full adder implementation using DCVSL technique compared to static CMOS technique. But dynamic power dissipation is increased. This drawback can be overcome by implementing adder cells using XOR/ XNOR and multiplexer in DCVSL methodology. It can be observed that Propagation delay, dynamic power dissipation and requirement of no. of transistors had been reduced remarkably. The problem with pass transistor based multiplexer is that there is logic degradation in the output. When implemented with NMOS pass transistor, the output is decreased by Vth when transmitting logic '1' to the output. This can be eliminated by utilizing the Transmission gate technology or using additional inverters at output stages. In both cases there is need for additional transistors and hence increase in power dissipation and effective chip area.

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