International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-2 Issue-5, April 2013

Comparison of Phase Frequency Detectors by Different Logic Gates

Raj Nandini, Himadri Singh Raghav, B.P.Singh

Abstract*—The Phase Detectors determines the relative phase difference between the two incoming signals and outputs a signal that is proportional to this phase difference. Some phase detectors also detect the frequency error, they are called Phase Frequency Detectors (PFD). It is very important block for the Delay Locked Loop. This paper presents the different design schemes of the PFD and compares them with their output results. The circuits that have been considered are the PFD using AND Gate, PFD using NOR Gate and PFD using NAND Gate. The different PFD circuits are designed and layouts are also simulated on Tanner EDA Tool using 0.18µm CMOS process technology with supply voltage 1.8V.

***Index Terms*— Dead Zone, Layouts, Maximum Operating Frequency, Phase Frequency Detector, Tanner Tool**

I. INTRODUCTION

The rapid growth in wireless applications in last decade has motivated to design fully integrated, low power, low cost and high performance transceivers. Most of the wireless implements frequency using Delay Locked Loops. DLL finds wide application in areas such as communication, clock generation circuits [1], wireless systems, digital circuits. The basic building block of DLL consist of phase detector (PD), loop filters, charge pump, voltage control delay line (VCDL).

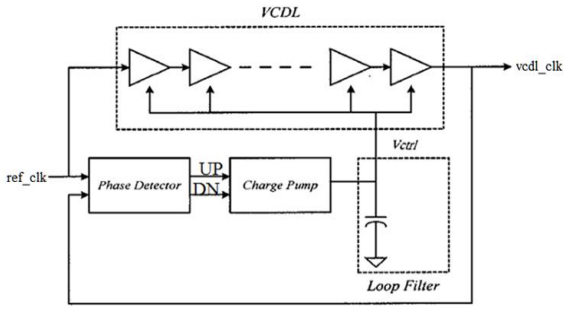

Fig.1 Block diagram of DLL

PFD in DLL is used to detect the phase as well as frequency difference between the two signals that is reference signal and the output from VCDL as compare to the phase detectors which are capable of detecting the phase difference only. The characteristics of PFD have huge impact on performance of DLL. The lock time and timing jitter of a DLL are largely affected by the characteristics of phase frequency detector.

Manuscript published on 30 April 2013.
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II. DESIGN ISSUES

The main two design issues which should be taken into account are dead zone and blind zone. If the phase difference between the clocks at the input of the phase detector is smaller than a certain value, then the control voltage is not a function of the phase difference. This is basic definition of dead zone. Dead zone is due to the delay time of the logic components of digital circuit and the reset time that requires by the reset path to reset the flip flops of the PFD [2].

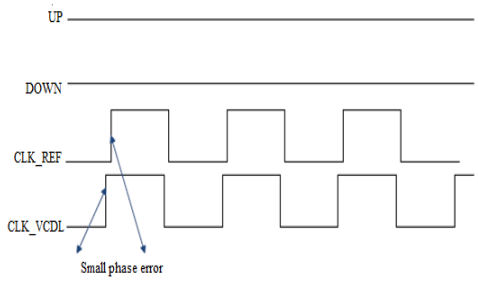

Fig. 2 Dead Zone

A delay cell is inserted in the reset path to reduce the dead zone. Due to dead zone the performance of DLL decreases as noise is added at VCDL output. The blind-zone is the region where the phase difference approaches plus or minus 360°, in which the edges of every next cycle occurs during the resetting pulse will not be seen by PFD. Blind zone [3] reduces the phase detection range. It becomes obvious that the blind zone of a PFD is detrimental to the DLL settling behaviors, and will slow down the lock time. The maximum operating frequency is defined as the shortest period with correct UP and DN signals together with the inputs have the same frequency and 90 degree phase difference [4].

III. CIRCUIT ARCHITECTURE

A. PFD using NAND Gate

The circuit consists of two resettable, edge triggered D flip flops with their D inputs tied to logic 1 and a NAND Gate in the reset path [5]. The explanation of the general operation of the PFD begins by describing the initial state of the device. First, the UP and DN signals are reset to low or zero and assume both the REF frequency signal and the VCDL signal are high or one. Additionally, the REF frequency waveform is slightly leading the VCDL waveform. When a falling edge occurs on the REF input, the high or one on the D input is transmitted to the Q output or UP. A short time later, the VCDL waveform experiences a falling edge and the Q output or DN of the other flip flop is set. Once both UP and DN are high or ONE, the NAND gate experiences a transition to force the Reset signal to zero. The flip flops are designed so that zero on the Reset signal resets the Q outputs to zero.

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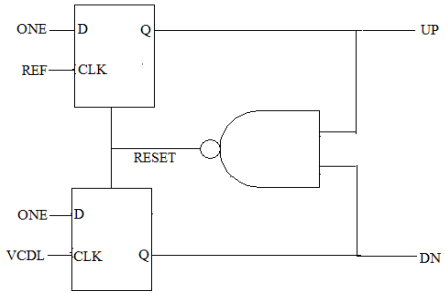

Fig.3 NAND Gate based PFD

The PFD is implemented with True Single Phase Clocked logic. The design strategy is to minimize the number of transistors and the amount of power consumed. However, not all of the transistors can be implemented with minimum width such as those involved in the reset operation. The schematic of NAND Gate based PFD is shown in Fig.4 and layout is shown in Fig.5

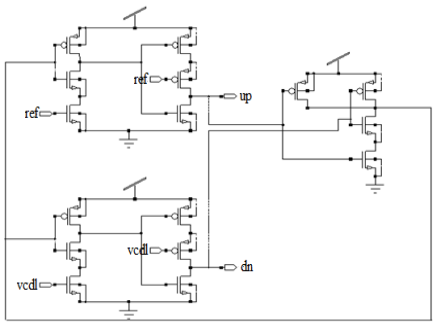

Fig.4 Schematic of NAND Gate based PFD

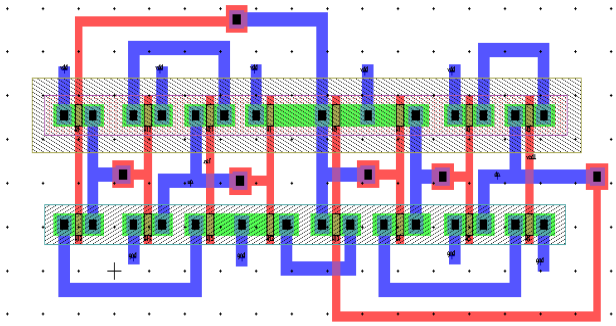

Fig.5 Layout of NAND Gate based PFD

B. PFD using NOR Gate

Fig.6 shows the PFD using NOR gate. The circuit consists of two resettable, edge triggered D flip flops with their D inputs tied to logic 1 and a NOR Gate in the reset path [6]. The REF and VCDL serve as clocks of the flip flops. The UPb and DNb signals are given as input to the NOR gate. Suppose the rising edge of REF leads that of VCDL, then UPb goes to logic low i.e. UP keeps high until the rising edge of VCDL makes DNb on low level. Because UPb and DNb are NORed, so RESET goes to logic high and resets the PFD into the initial state.

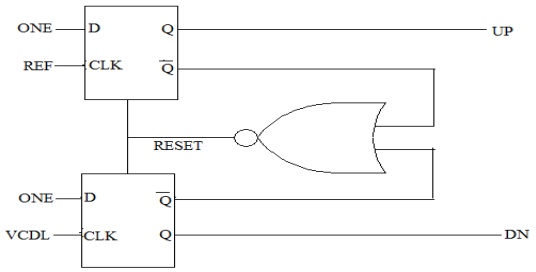

Fig.6 NOR Gate based PFD

The schematic of NOR Gate based PFD consisting of only 20 transistors is shown in Fig.7 and layout is shown in Fig.8

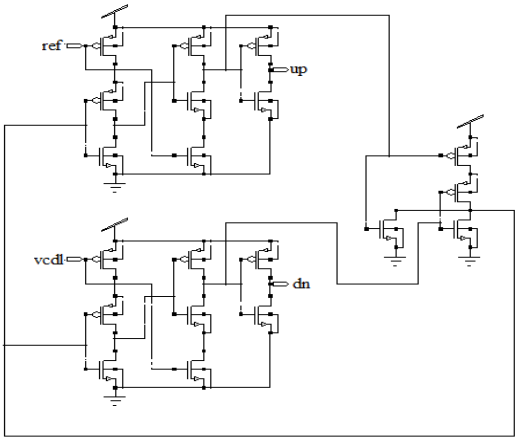

Fig.7 Schematic of NOR Gate based PFD

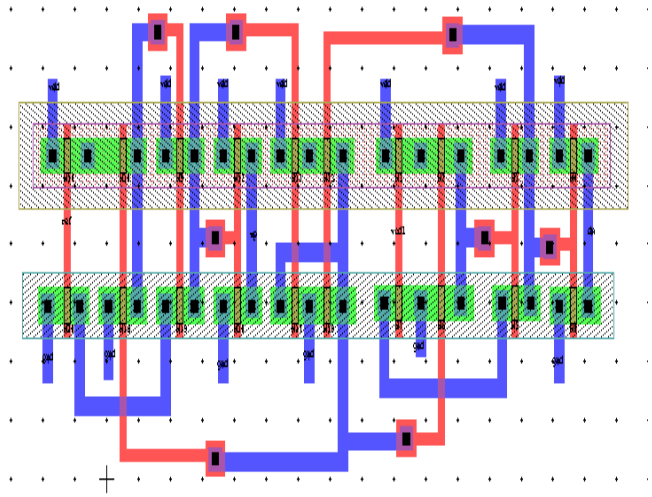

Fig.8 Layout of NOR Gate based PFD

C. PFD using AND Gate

The circuit consists of two resettable, edge triggered D flip flops with their D inputs tied to logic 1 and a AND Gate in the reset path [7]. The REF and VCDL serve as clocks of the flip flops. Suppose the rising edge of REF leads that of VCDL, then UP goes to logic high. UP keeps high until a low to high transition occurs on VCDL. Because UP and DN, are AND, so RESET goes to logic high and resets the PFD into the initial state.

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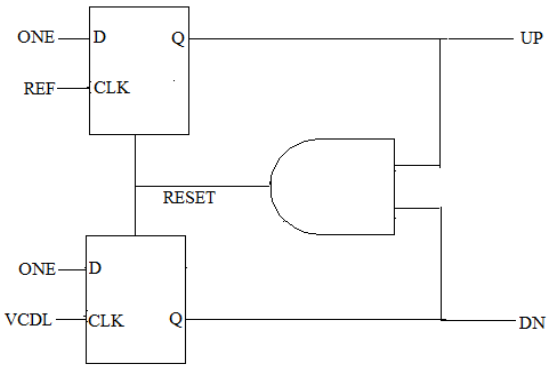

Fig.9 AND Gate based PFD

The schematic of AND gate based PFD circuit consisting of only 22 transistors is shown in Fig.10 and layout in Fig.11

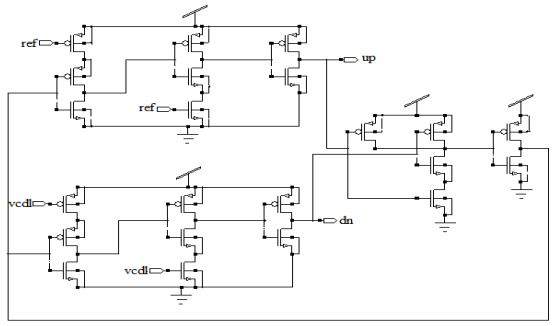

Fig.10 Schematic of AND Gate based PFD

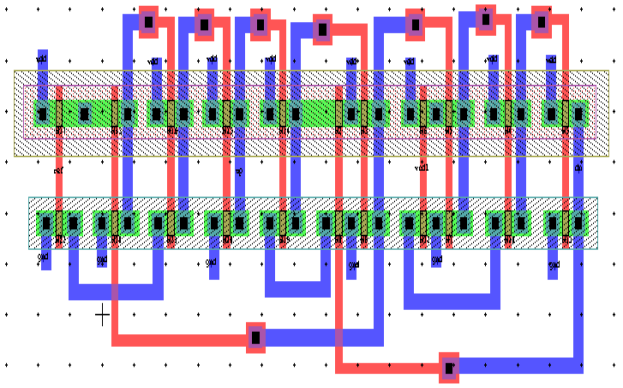

Fig.11 Layout of AND Gate based PFD

IV. SIMULATION RESULTS

The PFD is a state machine with three states. When ref leads vcdl, the up output is asserted on the rising edge of ref. The up signal remains in this state until a low to high transition occurs on vcdl. At that time, the dn output is asserted causing both the flip flops to reset through the asynchronous reset signal. There is a small pulse on the dn output, whose duration is equal to the delay through the logic gates and the reset delay. The pulse width of the up pulse is equal to the phase error between the two signals.

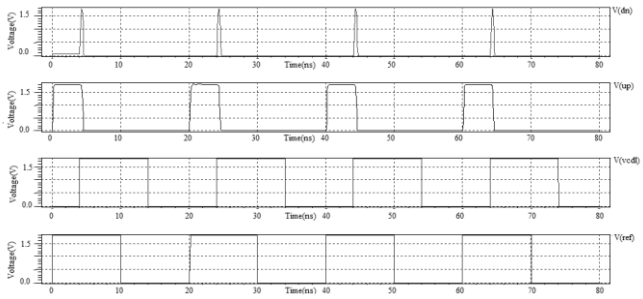

Fig.9 AND Gate PFD simulation I (ref signal leads vcdl signal)

In the second case, ref signal is lagging vcdl signal. In this dn pulse represents the difference between the phases of two clock signals.

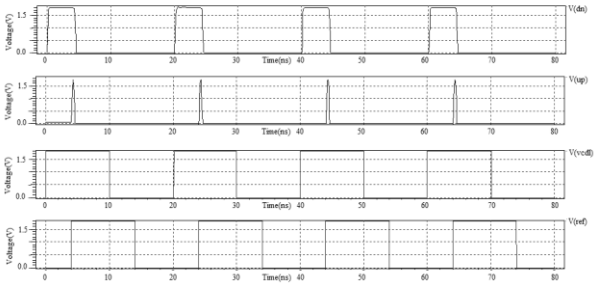

Fig. 10 NOR Gate PFD simulation II (ref signal lags vcdl signal)

In the third case, ref signal is in phase with vcdl signal, which is shown in Fig. 11. In this case, the loop is in locked state and short pulses will be generated on the up and dn outputs.

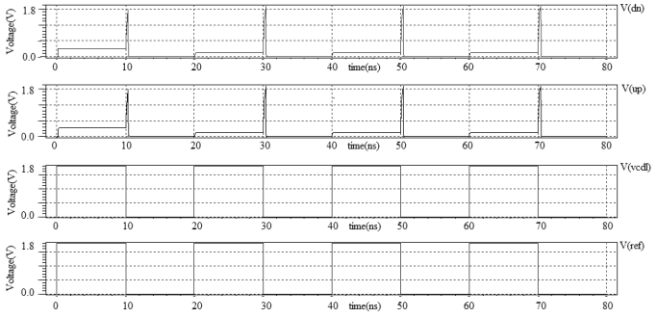

Fig.11 NAND Gate PFD simulation III (ref signal is in phase with vcdl signal)

V. PERFORMANCE COMPARISON

Table I depicts various parameters for the different PFDs when they are designed on Tanner13.0v. It is seen that NAND based PFD has the minimum power consumption and occupy less area compared to the other two. They all have the same range of operating frequency. Dead Zone problem is also negligible for the NAND Based PFD.

Table I: Comparison among different PFDs

Parameters	NAND Based PFD	NOR Based PFD	AND Based PFD
Max.Operating Frequency	1 GHz	1 GHz	1 GHz
Power Consumption	2.157780 e-005W	2.57199 e-005W	2.912547 e-005W
Glitch Period	5.15ns to 5.53ns	5.12ns to 5.66ns	5.19ns to 5.85ns
Glitch Time	380ps	540ps	660ps
Transistor Counts	16	20	22
Dead Zone	25ps	40ps	50ps
Delay	2.4425e-009 sec	4.6267e-009 sec	5.6597e-009 sec

VI. CONCLUSION

Minimization of power consumption is essential for high performance VLSI systems. This paper compares the performance of Phase Frequency Detectors by different Logic Gates .As can be seen from the simulation results AND based PFD consumes maximum amount of power among all the PFDs and has highest delay.

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NOR based PFD consumes more area and power compared to the NAND based PFD. Therefore, in order to have low power consumption and smaller area we use NAND based PFD which is also having approximately zero Dead Zone problem.

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