Tunneling Field Effect Transistors for Low Power Digital Systems

L.Megala, B.Devanathan, R.Venkatraman, A.Vishnukumar

Abstract*— MOSFET transistors are commonly used in high speed integrated circuits, yield smaller and faster more functions at lower cost. Various problems exist with scaling of MOSFET devices i.e., short channel effects, drain induced barrier lowering, velocity saturation which limits the performance of MOSFETs. Scaling limitations of MOSFET devices leads to lower ON to OFF current ratio limited by 60mV/dec sub threshold slope. A new type of device called "Tunnel FET" is used to overcome these difficulties. TFET can beat 60mV/dec sub-threshold swing of MOSFETs. In tunnel FET carriers are generated by band-to-band tunneling and OFF current are low. This makes ideal for ultra low power digital systems. Tunnel FET have energy barrier in OFF state, which avoids power-consuming leakages. In this paper sub-threshold swing and low OFF current is simulated and its power is analyzed.

***Index Items*—Tunnel FET, Sub threshold swing, PIN Tunnel FET, PNPN Tunnel FET**

I. INTRODUCTION

The Tunnel Field Effect Transistor (TFET) had been chosen before as the most promising device to respond to the demanding requirements of future technology nodes. The benefits of the TFET are especially linked to its potential for sub-60mV/decade sub-threshold swings, a pre-requisite for scaling the supply voltage well below 1V. Furthermore, the TFET has reduced short-channel effects compared to the MOSFET.

Tunneling is a quantum mechanical phenomenon with no analog in classical physics. It occurs when an electron passes to a potential barrier without having energy to do. Tunneling is so great i.e., lower sub-threshold swing can allow lower operating voltages to be used. It leads to chips that consume less power.

Electrons tunnel from valence band to conduction band to conduction band where they readily transport to drain terminal. Holes on drain side will tunnel into valence band and transport into floating body. In scaling, TFET do not suffer from short channel effects. Power dissipation of TFETs can beat 60mV/dec sub-threshold swing of MOSFETs.

In most of the literature published so far, the experimentally shown ON-currents are unacceptably low for a technology that would like to replace the MOSFET. While OFF-currents are in the range of femtoamperes or microamperes, ON-currents for applied drain and gate voltages of 2 V are still limited to the nanoamperes range. Furthermore, in order to have a CMOS-compatible technology, voltages should be limited even more, to about 1.2 V.

II. DEVICE ARCHITECTURES

A. PIN Tunnel Structure

Conventional TFETs has smaller ON currents than MOSFETs such that switching speed is smaller than MOSFET switching. TFETs are ambipolar. It demonstrated that it may be possible to shorten the gate without affecting its direct current (fig (a)). Short gate TFET offers both performance advantages such as reduced ambipolar behavior increased switching speed.

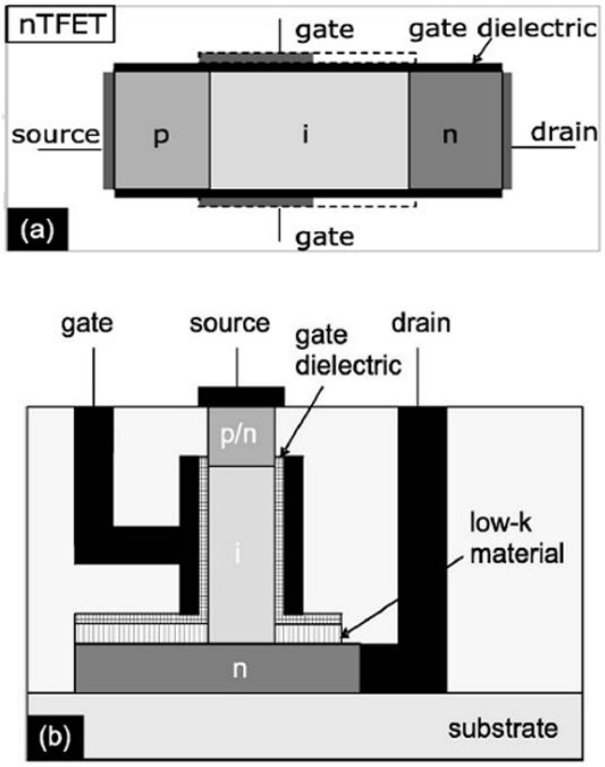

Figure 1: (a) Conventional nTFET (highly-doped p-type source region, intrinsic channel region, highly-doped n-type drain region) with flexible gate structure: the dashed line shows the conventional gate structure, the filled box represents a shortened gate. (b) Cross-section of the most straightforward implementation of a vertical TFET depending on the source doping type).

B. PNPN Tunnel Structure

A thin lightly doped packet is inserted at the source tunneling junction to reduce tunneling distance in fig2. PNPN device concept based on band-band tunneling gate controlled tunneling junction is a source of electrons tunneling width is reduced by fully depleted n^+ layer.

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PNPN tunnel FET has reduced potential drop at tunnel junction and it has improved drive current. Ambipolar conduction is reduced at PNPN tunnel FET. Compared with PIN tunnel FET PNPN is best.

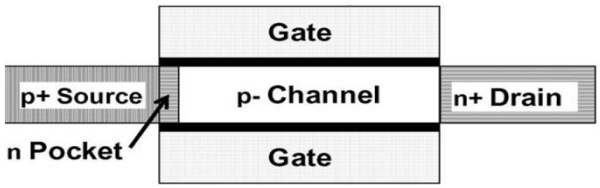

Figure 2: PNPN Tunnel Structure

III. DEVICE OPERATION

In the device structure of Tunnel FET, the drain is connected to n^+ terminal whereas source is connected to p^+ terminal. SiO_2 or High-K is used as an insulator. Metal Gates also take place in the operation of Tunnel FET in fig3.

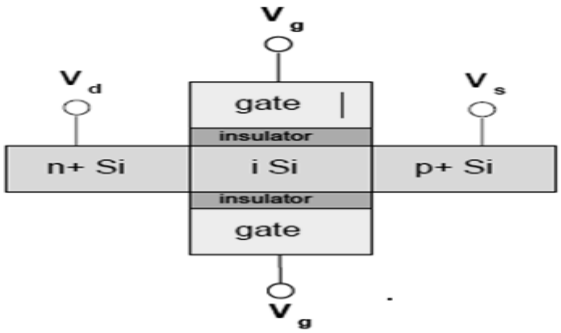

Figure 3: Device Structure of Tunnel FET

In the OFF state, when the drain voltage is positive and gate voltage is zero, no current flows through the terminal and shown in fig 4.

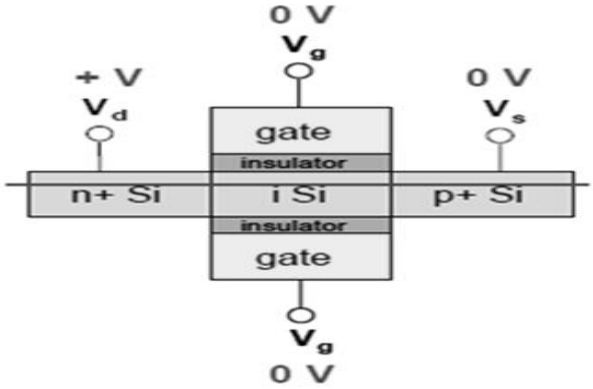

Figure 4: Device Operation in OFF state

In the fig 5 shows ON state, when the gate voltage and drain voltage is positive, the barrier becomes thin and hence the current flows through the terminals.

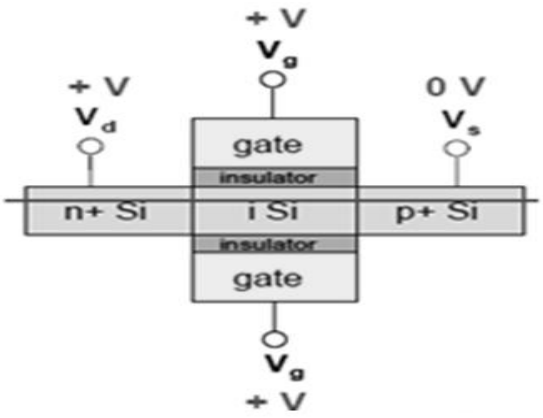

Figure 5: Device operation in ON state

Continuous downscaling of CMOS technology has led to immense improvements in its performance. However, the switching characteristics of the present day MOSFET switch are far from the ideal one. For the ideal switch, the sub-threshold swing is zero and this leads to zero off-state current. This off-state current is the most crucial parameter for the low standby power applications (e.g. cellular phone) as it determines the battery life of the device. The minimum value of the sub-threshold swing of today's MOSFET is physically limited to 60mV/decade at room temperature due to the drift-diffusion mode of carrier transport. In fact, in ultra-short channel MOSFET the sub-threshold swing is further deteriorated due to several parasitic effects (e.g., punch through, short channel effects etc). Therefore for future low standby power application one requires alternative MOSFET architecture which uses different type of carrier transport mechanism. The aim of this paper is to explore the various available options and to come up with a technology which is CMOS compatible and solves the problem of increased leakage for low standby power applications. The Tunnel Field Effect Transistor (TFET) with perfect saturation in the output characteristics, sub-60mV/decade sub threshold swing and extremely high I_{ON}/I_{OFF} ratio has attracted a lot of attention for such applications. However, due to extremely low I_{OFF}, even though it has a very good I_{ON}/I_{OFF} ratio, it fails to meet the technology requirements of I_{ON}. The simulation process is obtained by means of TCAD software.

IV. SIMULATION

To model band-to-band tunneling generation rate, the Kane's model is used in TCAD. Technology Computer Aided Design (TCAD) simulates and predicts characteristics of a transistor or semiconductor circuit and thereby increases the efficiency in designing and development of VLSI. An important benefit of using TCAD is that it can help in understanding how semiconductor devices work. TFET structure shown in fig 6.

$$I_{DS} = A_{kane} D^2 W_g^{-1/2} V_{GS}^2 e^{-(B_{kane} W_g^{\frac{3}{2}})/(V_{GS} D)}$$

Where,

$$A_{kane} = (e^2 m_0^{1/2})/(18\pi h^2)$$

$$B_{kane} = (\pi m_0^{1/2})/(2eh)$$

Sub- threshold swing: Sub-threshold swing of a device is defined as the change in gate voltage which must be applied in order to create a one decade increase in the output current.

$$S = \frac{dV_g}{d(\log I_d)}[\text{mV/dec}]$$

Sub-threshold swing of a MOSFET is limited by its physics (formation of inversion channel). Sub threshold swing is about 60mV/dec.

$$S_{MOSFET} = \ln(10)\frac{kT}{q}[\text{mV/dec}]$$

Sub-threshold swings of Tunnel FETs use different physics and can have swing less than 60mV/dec.

$$S_{TFET} = \left(\frac{l(\log I_d)}{dV_{gs}}\right)^{-1}$$

Sub-threshold slope of the Tunnel FET is expressed as

$$S_{TFET} = \frac{V_{gs}^2}{5.75(V_{gs}+Const)}[\text{mV/dec}]$$

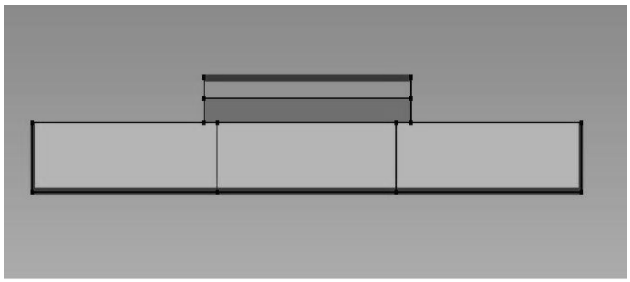

Fig.6 Structure of Tunnel FET in TCAD

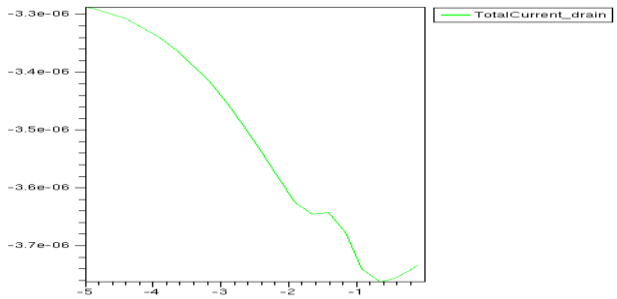

Fig: 7 Graph showing the plot of Gate voltage Vs drain current

V.ANALYSIS

In this paper, the power is analyzed by means of equation given by,

$$P = CV^2f$$

Where, C – Capacitance
V – Applied voltage
f – Frequency

This analysis is very much useful for ultra low power systems.

Static power and dynamic power

Static power analysis uses average current to calculate IR drop while dynamic power analysis uses peak value of current at any time to calculate the same. Static power analysis considers Power to ground network as resistive while dynamic power analysis considers it as R and C.

$$V_{Static} = I * R$$
$$V_{Dynamic} = I(t)*R+L\ di/dt$$

Where, t – time taken
R – Resistance
L - Inductance

Static power analysis include power consumption in steady state, it also includes leakage current. Static power is small compared to dynamic power because it does not include power consumption during switching. Dynamic power analysis includes power consumption due to switching only, and it's a high value than static power analysis.

Off-state leakage is static power, current that leaks through transistors even when they are turned off. The other source of power dissipation in today's microprocessors is dynamic power arises from the repeated capacitance charge and discharge on the output of the hundreds of millions of gates in today's chips.

Active and Standby power

The active and standby power is analyzed by means of equation,

$$P_{active} = F.C.V^2_{dd}$$
$$P_{standby} = I_{off}.V_{dd}$$

VI. CONCLUSION

Until recently, only dynamic power has been a significant source of power consumption and Moore's law helped to control it. However power consumption has now become a primary microprocessor design constraint in which the researchers in both industry and academia will struggle to overcome in the next few years.

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