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Three-Stage 18 level Hybrid Cascaded Multilevel Inverter Using a Hybrid Method

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Abstract*— This paper proposes a new hybrid algorithm for three stage 18 level cascaded multilevel inverter. The inverter consists of main high-voltage, medium-voltage and low-voltage stages connected in series from the output The high-voltage stage is made of a three-phase conventional inverter to reduce dc source cost and losses. The medium- and low voltage stages are made of three-level inverters constructed using cascaded H-bridge units. The aim of the proposed algorithm is to avoid the undesirable high switching frequency for high and medium-voltage stages despite the fact that the inverter's dc sources are selected to maximize the inverter levels by eliminating redundant voltage states. Switching algorithms of the high- and medium-voltage stages have been developed to assure fundamental switching frequency operation of the high-voltage stages and not more than few times this frequency for the medium-voltage stage. The low-voltage stage is controlled using SVM to achieve the reference voltage vector exactly and to set the order of dominant harmonics as desired. The realization of this control approach has been enabled by considering the vector space plane in the state selection rather than individual phase levels.

The simulation results shows the effectiveness of the proposed strategy in terms of computational efficiency as well as the capability of the inverter to produce very low distorted voltage with low switching losses.

Index Terms*—Inverters, harmonics, pulse width modulation (PWM), space vector modulation (SVM).

I. INTRODUCTION

The multilevel voltage source inverters unique structure allows them to reach high voltages and power levels without the use of transformers. They are specially suited to high voltage vehicle drives where low output voltage total harmonic distortion (THD) and electromagnetic interference (EMI) are needed. The general function of the multilevel inverter is to synthesize a desired voltage from several levels of dc voltages. As the number of levels increases, the synthesized output waveform has more steps, which produces a staircase wave that approaches the desired waveform. Also, as more steps are added to the waveform, the harmonic distortion of the output wave decreases, approaching zero as the number of levels increases.

As the number of levels increases, the voltage that can be spanned by connecting devices in series also increases. The most attractive features of MLIs are as follows. 1. Staircase waveform quality: Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced.

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2. Common-mode (CM) voltage: Multilevel converters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Furthermore, CM voltage can be eliminated by using advanced modulation strategies 3. Input current: Multilevel converters can draw input current with low distortion. 4. Switching frequency: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency. Many studies have addressed some issues on MLI control strategies. Most of the proposed control methods have been extended from the conventional inverter control methods for example the multicarrier PWM strategy and multilevel space vector modulation control [1,2,3,4].The low switching frequency strategies have advantage when applied to MLI inverters where the harmonics distortion is considerably less than the conventional inverters case. Selected harmonics elimination [6] and voltage approximation [6] are examples of the low frequency strategies. On the other hand, some researchers have started developing control strategies which are fundamentally developed for MLI for example the one dimension [5] modulation and the hybrid modulation [7].Many studies have reported on the control of the MLI.Both high- and low-frequency switching approaches have been considered. Examples of high-frequency switching include the carrier-comparison PWM strategies, the space vector modulation (SVM) and the carrier-based SVM. High-switching frequency approach has been used generally with symmetrical topologies, where effective amplitude control and harmonics reduction method is crucial due to the small number of levels [11,12,13]. Among the low-frequency control strategies are voltage vector approximation which has been applied for asymmetrical MLI [14], selected harmonics elimination which has been implemented using switching angle lookup tables [8], and real-time-selected harmonic elimination [15], [16]. A new method based on unidimensional geometric representation of one phase of MLI voltage levels has been proposed (1-DM) [17]. This method identifies the two nearest inverter voltage levels to the reference voltage and determines the duty ratios corresponding to the two levels by simplified calculations. This concept has been applied to the symmetrical and asymmetrical CHBs and with various voltage ratios. In another paper "submitted for publication" [18], the authors have shown that 1-DM, when applied to three-phase inverter, is equivalent to the conventional SVM control method with simplified switching signal calculations. However, although not explicitly mentioned but can be shown from the concept and results, the control based on.

1-DM subjects the high-voltage stage to high switching frequency when the number of levels is maximized. The high-frequency operation period of the high voltage stage will be very considerable when the amplitude of the reference voltage vector is just below the total minus the highest stage dc voltages. The proposed control strategy is distinctive in enabling the hybrid inverter which has been designed with maximum number of levels by ratio-3 dc sourcing to be PWM controlled without subjecting the high-voltage stage to high switching frequency. This has been enabled by involving the 2-D space vector in the proposed hybrid strategy. In this algorithm, high voltage stage will be operated in square wave mode. The medium-voltage stage will be operated in low-frequency mode, while the low-voltage stage will be controlled by SVM at the intended switching frequency. An approach based on voltage vector decomposition has been developed to ensure the frequency conditions for high and medium stages and, at the same time, to set the low-voltage stage in a valid SVM-controlled region.

II. 18-LEVEL INVERTER TOPOLOGY AND SWITCHING STATES

The inverter circuit shown in Fig. 1 consists of the main high voltage six-switch inverter with each output line in series with two single-phase full-bridge inverters. The main and H-bridge cells are fed by isolated dc sources of 9*V s*, 3*V s*, and *V s*. This voltage ratio provides 18-level inverter. In this design, the high voltage stage has only one dc source that operates with reduced Current ripple compared to the three dc sources of CHB design [9, 10]. Therefore, considerable reduction in the number of dc sources and losses can be achieved.

To explain the noncompliance to the modulation condition by this design, consider the reference point 0 V in Fig. 1. Assume that the output point A voltage is required to be changed between 4Vs and 5Vs. The sole option to produce 4Vs and 5Vs is to add up (0 + 3*V s* + *V s*) and (+9*V s* − 3*V s* − *V s*) from the three stages, respectively. If the reference voltage amplitude is located between these two levels, there will be a carrier frequency switching between the two states. This switching involves all the three stages, including the high-voltage stage, and this is undesirable. The algorithm presented in the next section prevents the need for this kind of switching.

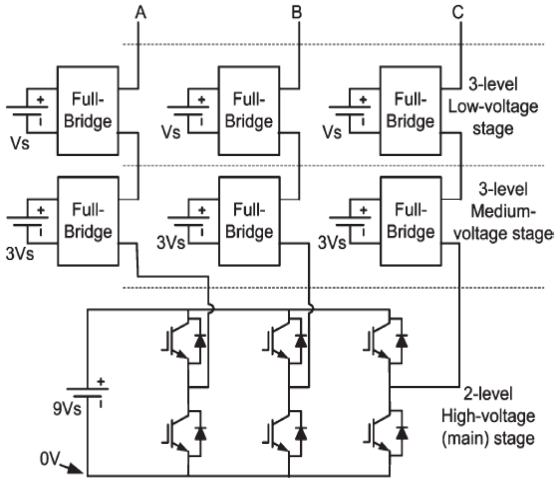

Fig 1.18-level hybrid inverter

A. Voltage Vectors and Inverter States

The switching variables of the inverter are denoted by {(*xabc*), (*yabc*), (*zabc*)}, where *x* is a binary digit ($x \in \{0, 1\}$) while *y* and *z* are trinary digits ($y, z \in \{0, 1, 2\}$). The states of the high-, medium-, and low-voltage stages are determined by *xabc*, *yabc*, and *zabc*, respectively. The output voltage vector can be represented in terms of switching state, as shown in the following derivation. Line voltages are represented in terms of the switching variables in

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = 9V_S \begin{bmatrix} x_a - x_b \\ x_b - x_c \\ x_c - x_a \end{bmatrix} + 3V_S \begin{bmatrix} y_a - y_b \\ y_b - y_c \\ y_c - y_a \end{bmatrix} + V_S \begin{bmatrix} z_a - z_b \\ z_b - z_c \\ z_c - z_a \end{bmatrix} \quad (1)$$

Phase voltages of the Y-connected load can be represented as follows:

$$\begin{bmatrix} \nu_{an} \\ \nu_{bn} \\ \nu_{cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} \nu_{ab} - \nu_{ca} \\ \nu_{bc} - \nu_{ab} \\ \nu_{ca} - \nu_{bc} \end{bmatrix} = \frac{Vs}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} 9x_a + 3y_a + z_a \\ 9x_b + 3y_b + z_b \\ 9x_c + 3y_c + z_c \end{bmatrix}. \quad (2)$$

The voltage vector is achieved by Park's transformation given in (3)

$$\begin{bmatrix} \nu_d \\ \nu_q \end{bmatrix} = \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \nu_{an} \\ \nu_{bn} \\ \nu_{cn} \end{bmatrix} \quad (3)$$

$$\begin{bmatrix} \nu_d \\ \nu_q \end{bmatrix} = V_s \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} 9x_a + 3y_a + z_a \\ 9x_b + 3y_b + z_b \\ 9x_c + 3y_c + z_c \end{bmatrix}. \quad (4)$$

Using (4), the voltage vector corresponding to any inverter state can be achieved. Alternatively, the voltage vector diagram of the three-stage inverter is drawn by two superposition steps. First, the vector diagram of the three-level medium-voltage stage inverter is drawn at the end of each of the seven vectors of the high-voltage stage. Then, the vector diagram corresponding to the low-voltage stage has been superimposed at the ends of resultant vectors, as shown in Fig. 2.

B. Voltage Vectors in g–h Axis System

The 60^0-spaced *g–h* coordinate system shown in Fig. 3 will be used to represent the voltage vectors in the proposed control algorithm. This system allows straightforward calculations as it is tightly related to the inverter voltage vectors. The *g*-h voltage vector components for the high-voltage stage are given in Equation (5) can be applied to medium- and low-voltage stages after replacing the dc voltage (9Vs) by 3*V s* or *V s* and *xabc* by *yabc* or *zabc*. Equation (5) shows that the inverter vectors have *g–h* coordinates which are integer multiples of *V s*, allowing simple fixed-point calculations.

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$$\begin{bmatrix} v_g \\ v_h \end{bmatrix} = 9V_s \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix}. \qquad (5)$$

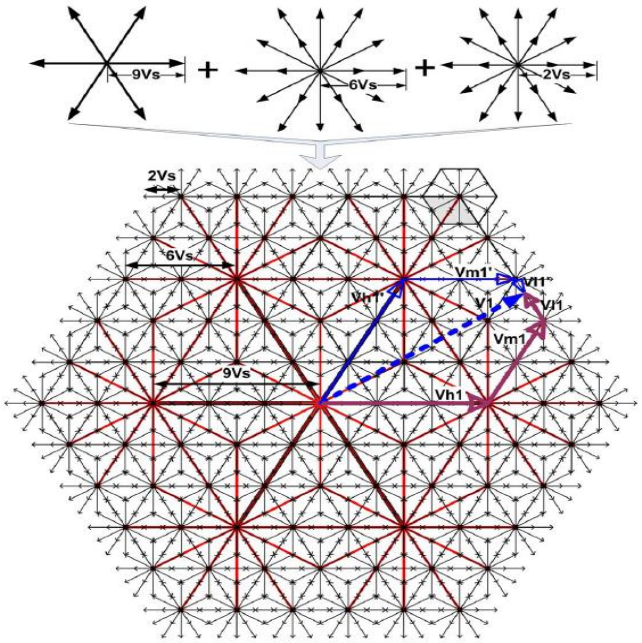

Fig 2.voltage vectors of 18-level inverter

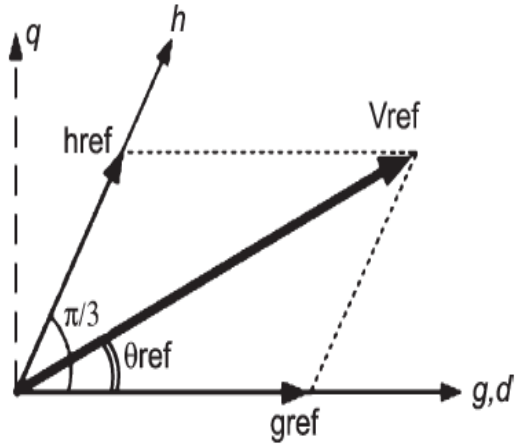

Fig3.60^{0}Spaced g-h System Used To Represent Voltage Vectors

III. DUAL SVM CONTROL STRATEGY

A. High- and Medium-State Domains

Each of the 18-level inverter vectors can be represented by the addition of three vectors that belong to high, medium, and low stages. With the exception of the outmost vectors, most of the 18-level inverter vectors can be represented by more than one combination of the three-stage voltage vectors, as for the example vector *V* 1 shown in Fig.2.To achieve fundamental frequency operation at high-voltage stage, the control algorithm explained in the next section aims to hold the high-voltage state as long as the reference vector can be reached by adding medium and low vectors to this high-voltage state vector. We shall define the hexagonal area marked by the medium- and low-stage vectors superimposed on a given high-state vector by its *domain*. The seven domains of the high-voltage stage vectors are shown in Fig. 4. In Fig. 4, the large hexagon, which is the inverter vector space, is composed of seven partially overlapped high-state hexagonal domains Some regions in the space belong to exactly one high-state domain without overlap, e.g., the region denoted by R1, which is covered only by the domain of state *xabc* = 011.

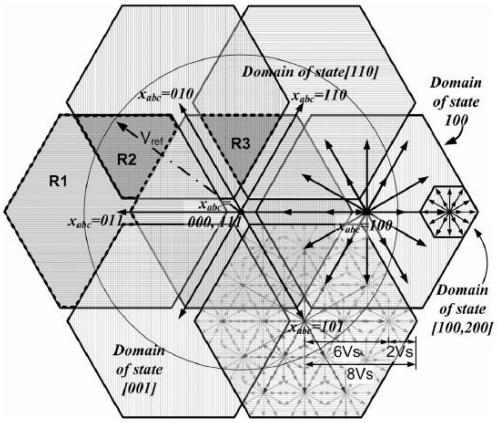

Fig. 4. High-voltage vector domains.

If the reference vector is located in this area, the controller should select the corresponding high state. Other areas are overlaps of more than one high-state domains, such as R2 (R3), which is mutual between *xabc* = 010 and 011 (*xabc* = 000, 110, 010, and 111). If the reference is located in such region, there is more than one option in the selection of *xabc*. The circular trajectory of the reference vector shown in Fig. 4 passes through the six high-state domains consecutively, and the controller will change the high-voltage stage state every 60◦ . The domains of the middle stage vectors can be defined in a similar way. Nineteen hexagons that represent the area covered by low-voltage stage vector diagram can be drawn within each of the seven high-state domains at the tips of the 19 medium-voltage vectors, as shown in Fig. 5, within the domain of *xabc* = 100. The medium-state selection determines which of the 19 hexagons is covered by the SVM control of the low-voltage stage inverter. By holding the state of high-voltage stage, medium-stage state selection and SVM control of the low-voltage stage will cover the high-voltage stage domain area defined in Fig. 4, except the small 12 triangles at the outer side darkly shaded in Fig. 5. To avoid any distortion that may result from the presence of reference vector on the areas out of SVM-controlled lowvoltage stage reach, a modified domain definition is introduced. The exact area covered by the SVM control of the low-voltage stage is the basic domain minus the 12 shaded triangles. The description of the resultant domain, however, is quite complicated. Alternatively, we have elected the smaller hexagons of 7*V s* sides marked with the dashed line in Fig. 5 as the modified domains. The modified domain is entirely located in the SVM-controlled region and enables the use of the same algorithm to handle the basic (8*V s*) and modified (7*V s*) domains. Fig. 5. Medium-stage domains corresponding to the high state *xabc* = 100; the dashed lines define the PWM high-voltage stagedomains. the high state *xabc* = 100; the dashed lines define the PWM high-voltage stage domains.

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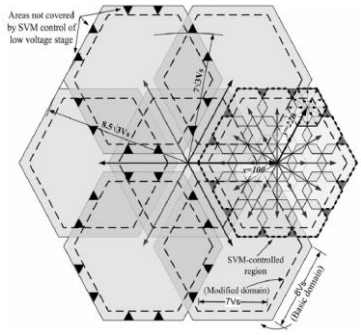


Fig. 5. Medium-stage domains corresponding to the high state *xabc* = 100; the dashed lines define the PWM high-voltage stage domains.

The difference between the basic high-state domain and the modified domain is that, in the basic domain, there are certain areas outside

control areas. However, the maximum amplitude of the reference vector, which is located within the modified domains, is $7\sqrt{3}Vs$, while the maximum amplitude for the basic domain is $8.5\sqrt{3}Vs$, as shown in Fig. 5. Therefore, the basic domain has higher maximum output amplitude by 21.4%, and we will test the controller using both domains.

B. Control Concept

Fig. 6. The reference vector is sampled at a sampling rate of *Ts*. During the sampling period, the controller determines the next switching states for high-, medium-, and low-voltage stages consecutively.

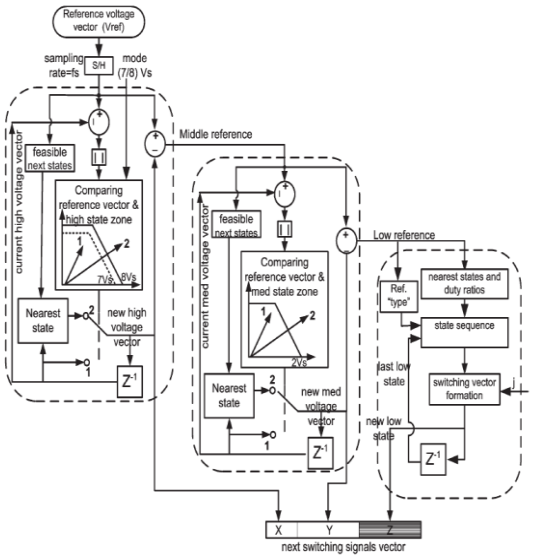


Fig 6.flow diagram

The outputs of the high- and medium stage routines are the values of *xabc* and *yabc* to be applied during the following sampling period. The low-voltage stage routine determines the three vectors nearest to the low-stage reference and their corresponding duty ratios during the following switching period. The output of the low-voltage routine is a *j*-element state vector [*zabc*], rather than one state *zabc*. During the following sampling period, *zabc* will take the values of these vector elements consecutively for subperiods of *Tc*(= *Ts/j*).

IV. SIMULATION RESULTS

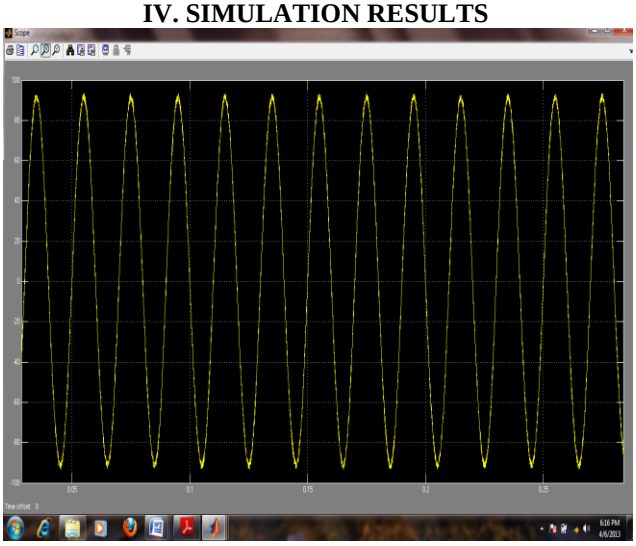
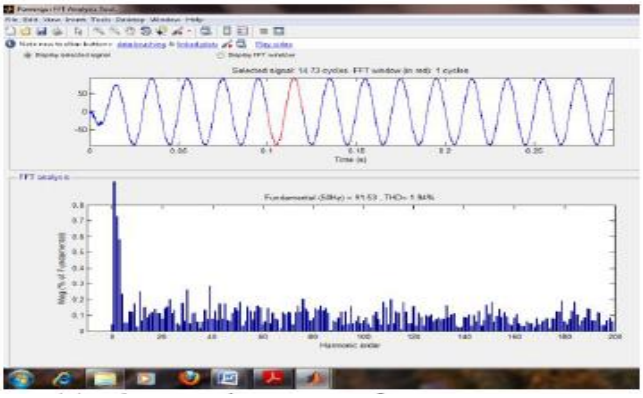


Fig. 8. Phase-voltage measurement with 80% amplitude and 50-Hz frequency reference.



(a) Phase-voltage waveform
(b) Frequency spectrum of the phase voltage.

Fig. 8 shows the measured phase-voltage waveform and its corresponding frequency spectrums with sinusoidal reference of 80% amplitude and 50 Hz. The total harmonic distortion (THD) is less than 2%, reflecting low distortion of the output voltage, and Fig. 8(b) shows that the dominant harmonics order is around 180, which is the number of sampling intervals per cycle.

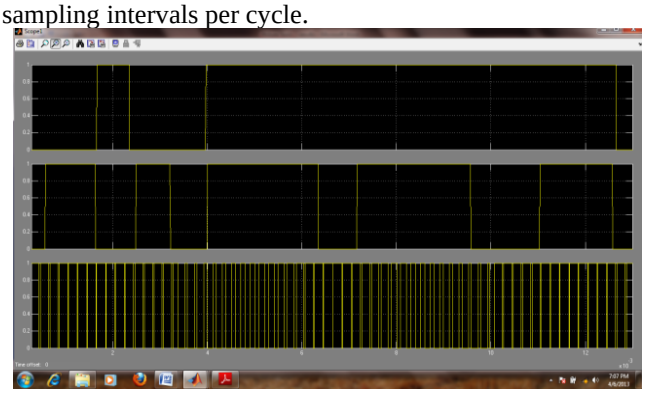


Fig. 9. Switching pulses with $M = 0.9$. From the top: (C1) High-voltage stage, (C2) medium-voltage stage, (C3) low-voltage stage,

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Fig. 9 shows the switching signals of the three stages. The top signal verifies that the high-voltage stage operates in square wave mode, the second signal shows that the medium stage operates at an average switching frequency that is equivalent to four times the fundamental frequency, and the third is the swiching signal for low voltage

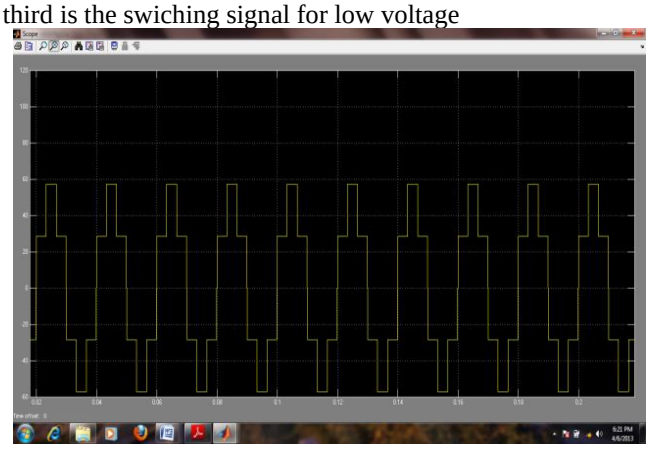

Fig 10 a). Voltage due to high-voltage stage only

Fig. 10. Phase voltage due to the switching signals shown in Fig. 9. From the top: Voltage due to high-voltage stage only, voltage due to high- and medium voltage stages, and voltage due to the three stages

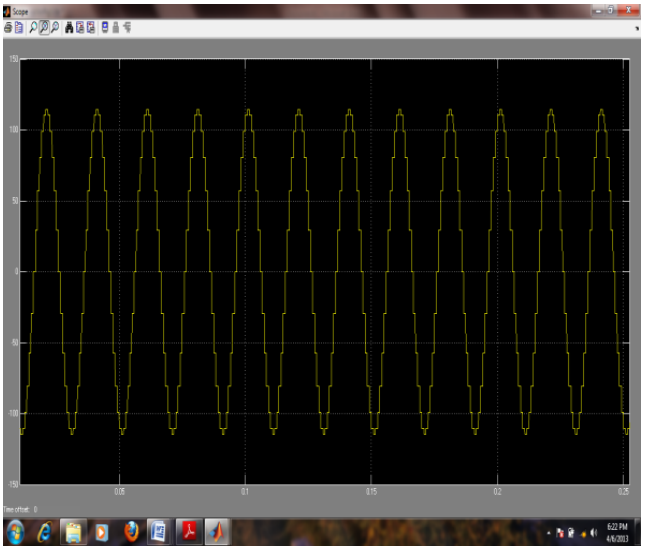

Fig 10 b) voltage due to high- and medium voltage stages

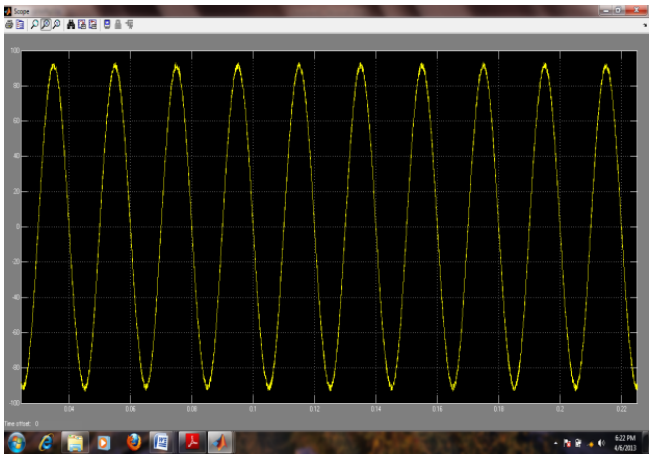

Fig 10 c).voltage due to the three stages.

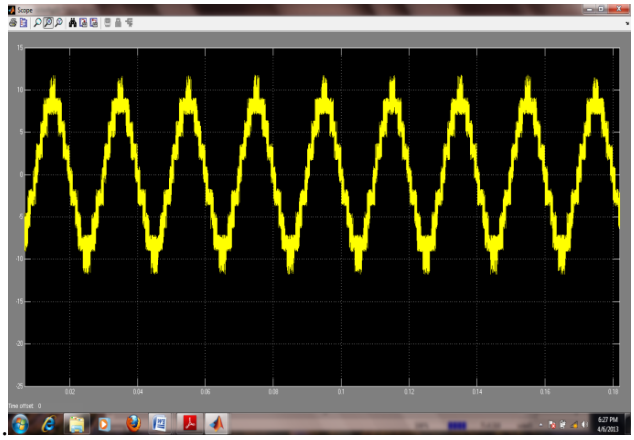

Fig. 11. Phase-voltage measurements with M = 9.4% and 50-Hz frequency reference. (a) Phase-voltage waveform

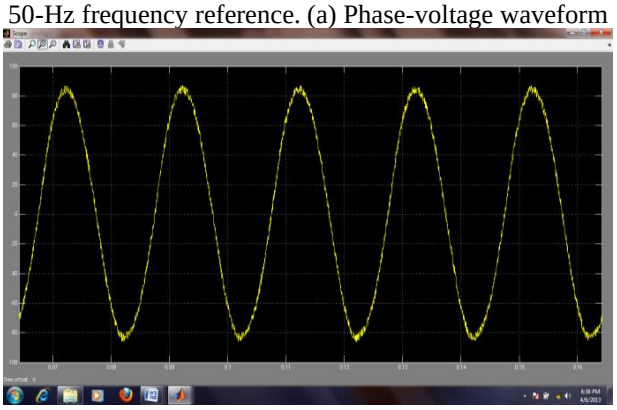

Fig 12.(a) phase voltage with modified 7vs high state domain with 45%reference amplitude

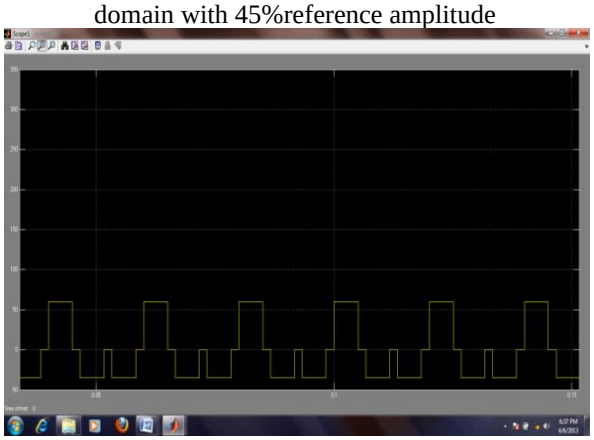

Fig 12.(b)phase voltage to high state only

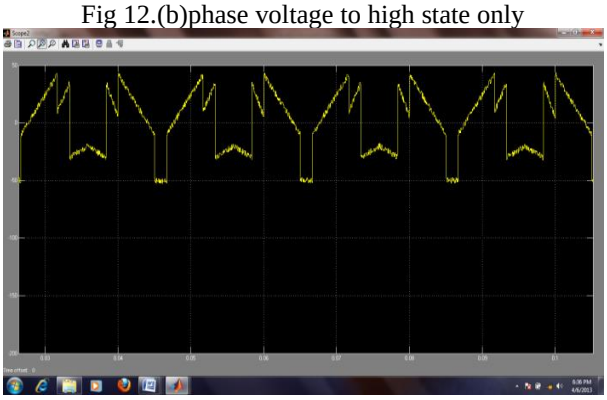

Fig 12.(c) Phase voltage corresponding to medium- and low-voltage stages.

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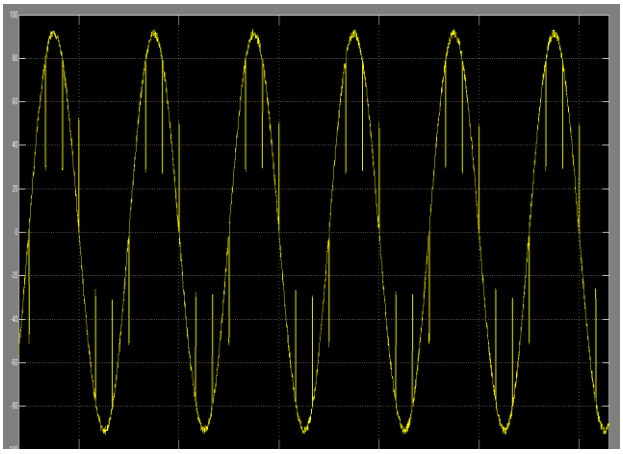

Fig 13. Phase voltage with $M = 0.9$ and modified 7Vs high domain

VI. CONCLUSION

In this paper, a three-stage 18-level inverter and its hybrid control strategy have been presented. The inverter has been designed with one main dc source to reduce the dc supply cost, and the supply voltage ratio has been selected to maximize the number of symmetrical levels. While this design is known to be unsuitable for carrier-based PWM control as it subjects the high-voltage stage to high switching frequency, the suggested control method has been proven to avoid this problem. In the hybrid control algorithm, the high-voltage stage switching frequency equals the output fundamental frequency, and the medium stage operates at no more than five times this frequency. The SVM method is used to control the low-voltage stage which operates at an average frequency that is equivalent to half the sampling frequency and provide all the SVM control advantages.

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