Design and Implementation of Low Power 4:1 Multiplexer using Adiabatic Logic

Sarita, Jyoti Hooda, Shweta Chawla

Abstract*— The main and highly concerned issue in the low power VLSI design circuits is Power dissipation. The basic approaches that we used for reducing energy/power dissipation in conventional CMOS circuits include reducing the supply voltages, on decreasing node capacitances and minimize the switching activities with efficient charge recovery logic. The Adiabatic switching technique based upon the energy recovery principle is one of the techniques which is widely used to achieve low power VLSI design circuits. In the following paper the power dissipation of various adiabatic circuits is calculated and then simulated using T-SPICE tool. From the results of calculation it is observed that among all of the techniques used for multiplexer implementation the efficient charge recovery logic (ECRL) multiplexer exhibits the minimum power dissipation. The adiabatic logic family has been proposed by implementing PMOS and NMOS transistors as pull down network and pull up network. With the help of calculated result, it has been shown that the multiplexer used with adiabatic logic can reduce the power dissipation than conventional CMOS circuit.

Index Terms*— Adiabatic, VLSI, ECRL, T-SPICE.

I. INTRODUCTION

The widely used concept of power dissipation becomes one of the critical issue for the performance because of rapid growth of rapid portable battery powered devices [1]. There are various methods that are widely used for reducing the power dissipation in circuits by reducing switching activities, supply voltage, load capacitances [1]. These methods only try to minimize the power dissipation but still most of the energy down from DC power supply is completely dissipated in the circuit [4]. The alternative method for reducing power dissipation is by the implementation of the adiabatic logic. The adiabatic logic circuits can reduce the power dissipation up to a very large extent by utilizing the AC power supply for the recycling of the energy that is stored into the load capacitances rather than to dissipate the energy in the form of heat in the circuit [4]. The Greek word Adiabatic used for the impassable. The word adiabatic having the concept of Thermodynamics which is used to describe about the thermal process in which there is no loss or gain in the form of heat [1,4]. In the following paper we have calculated the power dissipation for various adiabatic logic circuits using T-SPICE simulation tool. From the calculation we have done, it has also been found that among all the multiplexers, the efficient charge receovery logic (ECRL) multiplexer exhibits minimum power dissipation.

Manuscript received May, 2012.

Sarita Ola, Department of ECE, World College Of Technology & Management, Gurgaon, India.

Jyoti hooda, Department of ECE, World College Of Technology & Managemen ,Gurgaon, India.

Shweta Chawla, Department of ECE , B.M. College Of Technology & Management , Gurgaon , India.

The adiabatic logic family has been designed by implementing PMOS and NMOS transistors of pull down network and pull up network. From the results, it has been shown that the inverter used with the adiabatic logic concept has less power dissipation as compared to conventional CMOS inverter.

In standard CMOS circuits, the power dissipation usually occurs during the switching of the device. The changes are fed from the power supplied steered through the MOS devices and then dumped into the laod capacitor of the circuit. Both of the transistors, PMOS and NMOS transistors can be modeled by implementing an ideal switch in series with a resistor for the representation of the effective channel resistance of the switch as well as the interconnected resistance in the circuit. The pull up and pull down networks are connected to the load capacitance C_L, which is also known as the node capacitance. There is sudden flow of current through R when the used logic level is one, '1'. The charge, $Q= C_L V_{dd}$ supplied by the positive power supply rail for charging the load capacitance C_L to V_{dd}. Hence, the energy dissipation from the power supply is represented by the product of charge Q and supply voltage $V_{dd} = C_{L.} V^2_{dd}$, where Q is the charge and CL is the load capacitance [9]. Now, it is assumed that the energy dissipated from the power supply is equal to that energy which is supplied to $C_{L.}$ and it becomes equal to one half of the total supplied energy, i.e. $E_{stored}= 0.5\ C_L.V^2_{dd.}$ the remaining amount of energy is dissipated in resistance R. The same amount of energy is dissipation is observed during discharging of the NMOS pull down network when the given logic level is at "0". Hence, total amount of energy dissipated in the form of heat during charging and discharging can be represented as the total energy is equal to the sum of the energy dissipating in charging load the capacitor and discharging the capacitor.

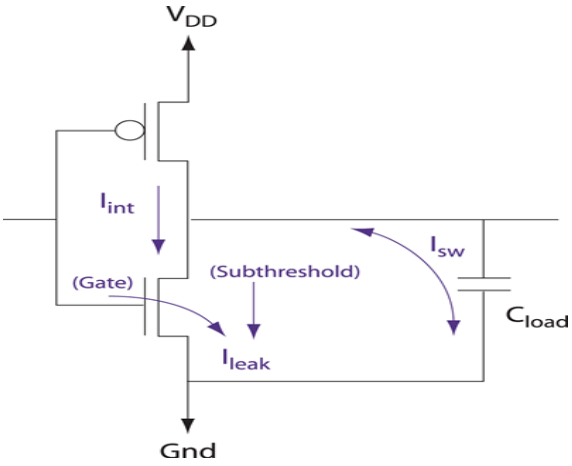


Figure-1.Adiabatic CMOS inverter

Where as in the Adiabatic logic circuits, the load capacitance is charged through a constant current source instead of a constant voltage source as in case of conventional CMOS circuits [1,6]. The Adiabatic switching technique is commonly used to minimize the energy loss during the charging and discharging of the load capacitor. The word adiabatic indicates for the state transition that occurs without any heat loss or heat gain. During the adiabatic logic is used , all of the capacitors are charged or discharged at a constant current for the minimization of the power dissipation. The adiabatic switching can be explained with a constant current source.

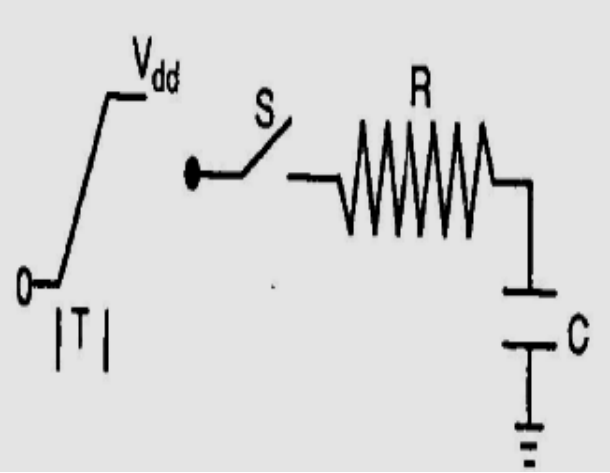


Figure 2- Charging & discharging of capacitor

The adiabatic logic circuit can be explained by the above circuit with a constant current source, a resistor and a capacitor. R is the resistance of PMOS network and V_C be the initial capacitance voltage of the circuit.

Voltage drop across the resistor R = IR

Power dissipated in the resistor $P(R) = I^2R$

Energy during charging of the capacitor = I^2RT

As we already know that I = CV/T then T = CV/I

$E = I^2RT = (CV/T)^2.RT = C^2V^2R/T$

$E= E_{dissipation} = ½ CV^2 x (2CR/T)$

The dissipated energy in the adiabatic circuit is smaller than the conventional CMOS circuit if T is larger than 2RC, that is dissipated energy can be reduced by increasing the charging time of the capacitor [1,6]. The energy dissipation is directly propotional to the resistance R but inversely propotional to the capacitance. Hence, ifor reducing the the energy dissipation, the resistance of PMOS pull up network will also be reduced.

For the conversion of a conventional CMOS logic into the Adiabatic logic, the pull up and pull down network must be replaced with the complementary transmission gate networks [3]. By the implementation of the transmission logic gates, the pull up network (PUN) is used to drive the actual output of the adiabatic gate while the pull down network drives the complementary output . so the main requirement is that all inputs should be available in the complementary form. For the adiabatic operation, the DC voltage supply of the original circuit must be replaced by the pulsed power supply [1,3]. The current drawn from the pused power supply during 0 to 1 transition is very large because of the large drain-source voltage. For reducing the energy dissipation , the drain current must be reduced. It can be easily achieved by implementing the adiabatic logic circuits.

II. CONCEPT OF ECRL

ECRL technology is that in which precharge and evaluation simultaneously performed and by implementing this method energy dissipation is reduced to a large extent. ECRL eliminates the precharge diode which dissipates less energy than the other adiabatic methods. It can also eliminates the need of more number of PMOS switches, in ECRL only two PMOS switches are used and it is the matter of fact that PMOS is the big source of power dissipation. It provides the charge on the output with full swing and it charges the load capacitance with the constant supply which is completely independent of the input signal.

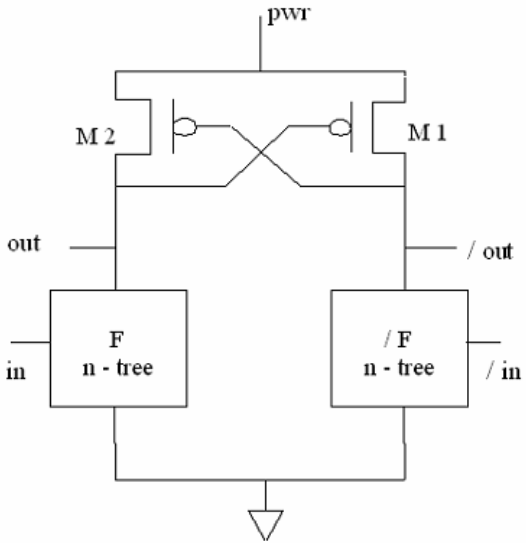


Figure-3.ECRL logic circuit

The circuit has two cross coupled transistors M1 and M2 of PMOS and two NMOS functional blocks for ECRL adiabatic logic implementation. An AC power supply pwr is used, so as to recover and reuse the supplied energy. Both out and /out are drive a constant load capacitance independent of the input signal. The cross coupled PMOS transistors helps for obtaining full swing in both precharge and recover phases. ECRL always provides the charge on the outputwith the full swing . hence, the voltage on the supply clock approaches to |Vtp|, the PMOS transistor gets turned off[11].

III. ADIABATIC AND GATE USING ECRL

Let us consider that one input is at high level and other input is at low level. At the initial cycle, when the power rises from zero to Vdd, the output remains at the ground level because it turns on the NMOS logic block. /out follows the power pwr through M1. When pwr reaches at a level of Vdd, the output holds a valid logic level. These values are restored during the hold state, and they are used as the inputs for the evaluation phase for the next stage. After the hold stage, power falls down to the ground level, /out returns its energy to the pwr so that the charge is recovered back. So, the clock pwr acts as both a clock as well as the power supply.

Let us consider the AND gate having the output , z = x.y, where x and y are the two inputs

And, $/z = \overline{x.y} = \bar{x} + \bar{y}$

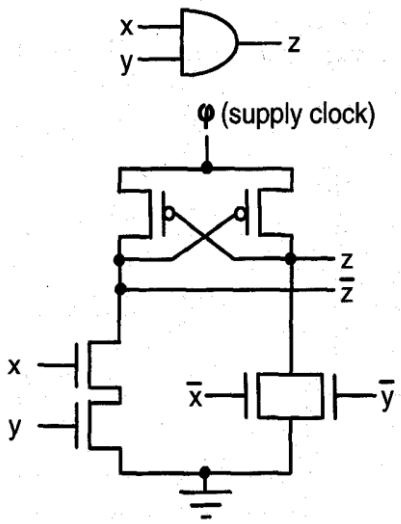


Figure-4. ECRL AND Gate circuit

So by substituting the value of y and $\bar{y}$ at the positions of F and F/ n tree positions in the Figure 3 respectively we get the AND circuit implementation using ECRL technology.[12]

IV. DESIGN IMPLEMENTATION OF 4:1MULTIPLEXER USING ECRL

The 4*1 Multiplexer having four inputs (D0,D1,D2 and D3) along with select lines(S1 and S2), we get the output Y,

Where $y = D_0\overline{S1}\,\overline{S2} + D_1\overline{S1}S2 + D_3S1\overline{S2} + D_3S1S2$

And , $\bar{y} = \overline{D0\overline{S1}\,\overline{S2} + D1\overline{S1}S2 + D3S1\overline{S2} + D3S1S2}$

$\bar{y} = (\overline{D0} + S1 + S2)(\overline{D1} + S1 + \overline{S2})(\overline{D2} + \overline{S1} + S2)(\overline{D3} + \overline{S1} + \overline{S2})$

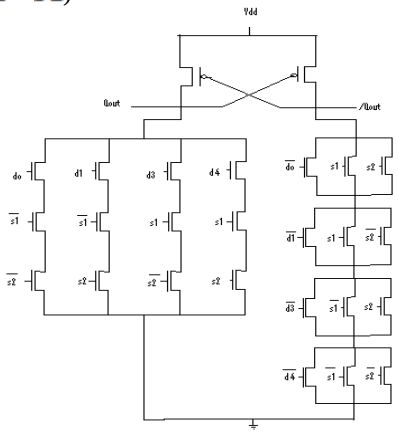
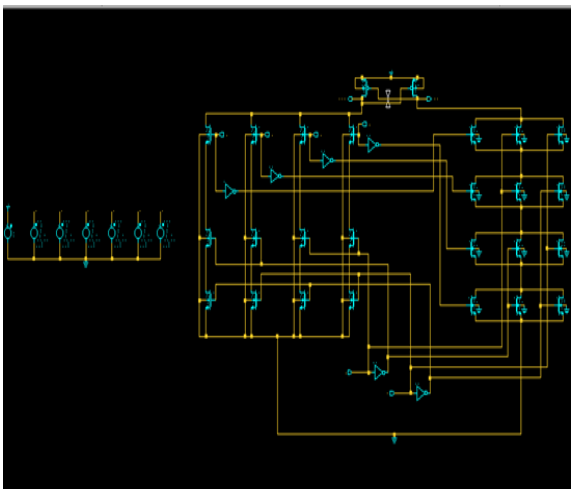
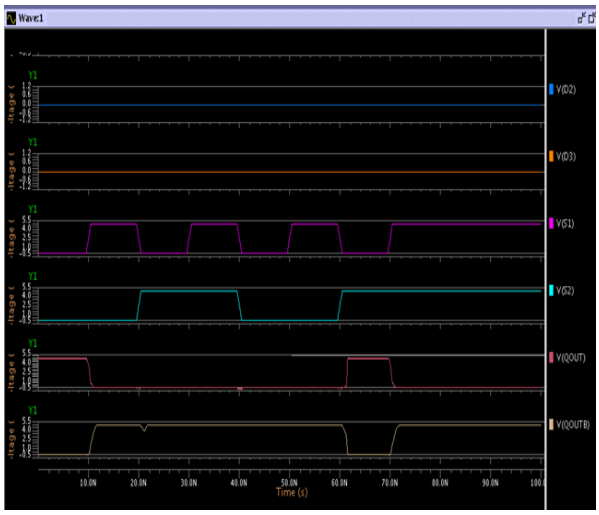


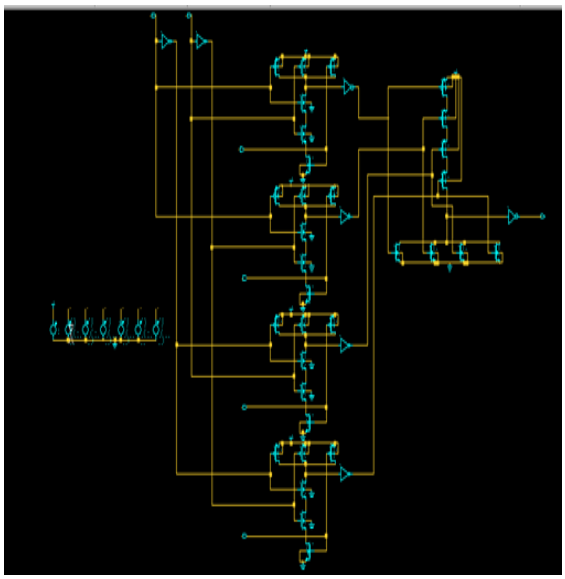
Figure-5. ECRL Multiplexer Circuit



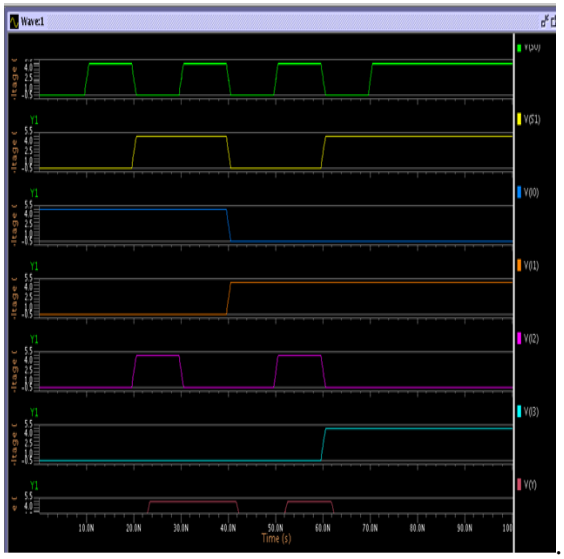
RESULT:



V.IMPLEMENTATION OF 4:1 MULTIPLEXER USING CONVENTIONAL CMOS



RESULTS:



VI. COMPARISON RESULTS BETWEEN ECRL AND MOS TECHNOLOGY

BASIS	ECRL MULTIPLEXER	CMOS MULTIPLEXER
Memory space allocated(bytes)	56631296	56635392
Elements	39	46
Nodes	26	30
Input signals	13	14
Temparature in Celcius	27	27
Total Power	4.4242N	6.2611N

REFERENCES

1. M. Pedram, "Power minimization in IC design: principles and applications," ACM Transactions on Design Automation of Electronic Systems, 1(1): 3-56,January 1996.
2. N. Weste and K. Eshraghian, Principles of CMOS VLSI Design: A Systems Perspective, 2nd ed. New York: Addison - Wesley,1993.
3. J. S. Denker, "A review of adiabatic computing," inProc. of the Symposium on Low Power Electronics,1994, pp. 94-97.
4. Jan Rabey,Massoud Pendram, Low power Design Methodologies:5-7,Kluwer Academic Publishers,5th edition. 2002
5. PD Khandekar, S Subbaraman ,Manish Patil"Low power Digital Design Using Energy-Recovery Adiabatic Logic" International Journal of Engineering Research and Industrial Apllications,Vol1,No. III,pp199-2081994, pp. 94-97.
6. S. Samanta "Adiabatic Computing" a contemporary review" 4th international conference on computer and devices for communication : codec 09" Kolkata 2009.
7. S. Samanta" Power Efficient VLSI Inverter Design using Adiabatic Logic and Estimation of Power dissipation using VLSI-EDA Tool" Special issue of International Journal of computer communication Technology. vol 2. isuue 2,3,4. pp300-303. 2010.
8. Arsalan, M. ; Shams, M. "An investigation into transistor-based adiabatic logic styles. " Circuits and Systems, 2004. NEWCAS 2004. The 2nd Annual IEEE Northeast Workshop on 20-23 June 2004 Page(s):1 – 4
9. J. Marjonen, and M. Aberg, "A single clocked adiabatic static logic- a proposal for digital low power applications," J. VLSI Signal Processing, Vol.27, Issue 27, Feb. 2001, pp. 253-268.
10. Lance Pick up and Scott Tyson, "Efficient Power management in 90 nanometer foundry reference flow" published in August/ September 2004 issue of chip design magazine.
11. Y. MOON AND D. K. JEONG, "An Efficient Charge Recovery Logic Circuit," *IEEE JSSC*, Vol. 31, No. 04, pp. 514-522, April 1996.
12. T. INDERMAUER AND M. HOROWITZ, "Evaluation of Charge Recovery Circuits and Adiabatic Switching for Low Power Design," *Technical Digest IEEE Symposium Low Power Electronics*, San Diego, pp. 102-103, October 2002.

AUTHORS PROFILE

Ms. Sarita received the B.Tech degree in ECE from Maharishi Dyanand University Rohtak, and M.Tech 4th semester student under the department of ECE from World College Technology & Management, Gurgaon. Her research interests are in low power analog circuits design & Digital design .

Ms. Jyoti Hooda is a student of m.tech 2nd year under the Department of Electronics and Communication engineering from World College of Technology and Management Gurgaon . Her area of interest is memory design .

Ms. Shweta Chawla, completed M.Tech in VLSI design fron Bansthali University & presently working as the assiatant professor in B.M. Group Of Institution, Gurgaon. Her research interest are in low power circuits and analog design.