A Fast FPGA Based Architecture for Skin Region Detection

Santanu Halder, Abul Hasnat, Amina Khatun, Debotosh Bhattacharjee, Mita Nasipuri

Abstract*—This paper presents an efficient FPGA based architecture for skin region detection algorithm from a facial image. A lot of research work has been carried out on skin region detection for image processing applications. But there is a very limited work to design a hardware module for the same purpose which is very useful for a real time system where speed is a key factor. In this paper, an attempt has been made towards the designing of an efficient FPGA based skin region detection algorithm which is better than the existing architectures in respect of both space and time complexity. The methodology proposed by Zhang et al. in 2000, has been chosen as the skin region detection algorithm for the present work due to its property of simplicity resulting in faster computation. The experimental result shows a significant improvement in space complexity over an existing architectures and the module is able to operate at 285.919MHz speed which is more than twice of the operating speed of the existing architectures.

***Index Terms*—Skin detection, Pixel classification, FPGA, YIQ.**

I. INTRODUCTION

Face recognition is a vibrant area of research over the last 20 years and today facial image processing has become an active research area all over the world. A lot of research work on facial feature extraction and face recognition for still and video images using skin color is carried out by Q.H. Thu et al [1], D. Saxe and R. Foulds [2], S. McKenna et al.[3], C. Garcia, G. Tziritas [4], N. Sebe et al.[5], A. Hadid et al.[6], Zhang et al.[7], D. Chai, and Zhang et al[8], D. Bhattacharjee et al.[9] etc. There are many skin region detection algorithm[1-7] and among these the algorithm proposed by Zhang et al.[7] is simple and works faster.

FPGA is becoming the most dominant form of programmable logic [10-11] over past few years. FPGA has advantage of low investment cost and desktop testing with moderate processing speed thereby offering itself as suitable one for real time application. In the literature Guangdong Liu and Zhongke Shi[14], Y.M. Mustafah and A.W. Azman[15] proposed a FPGA based architecture for Skin region detection algorithm. In this paper we have designed a different architecture for Skin region detection algorithm proposed by Zhang et al.[7]

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Which is faster and takes less space than the architecture proposed by them [14][15]. In real time system, the algorithm with less time complexity always gets preference. Our work is not only gives better performance in respect of time complexity, this work also takes less space than that of the architecture of Guangdong Liu and Zhongke Shi[14], Y.M. Mustafah and A.W. Azman[15].

This paper is organized as follows: The section II presents the brief description of the Skin region detection algorithm given by Zhang et al [7]. Section III presents the top level design of skin region detection hardware. Section IV depicts the proposed system architecture for Skin region detection. Section V shows the experimental results and finally section VI concludes and remarks about some of the aspects analyzed in this paper.

II. ALGORITHM FOR SKIN REGION DETECTION

To distinguish between skin colors and non-skin colors, the present system first converts the RGB images into YIQ color space. In 2000, Zhang et al. show that the YIQ channels have good clustering properties for human skin tones though distinguished by race, age, or gender and human skin colors are between 20-90 in I channel **[7]**. The steps for Skin region detection are as follows:

Step 1: Convert the RGB face image with size R1×R2 into YIQ color space according to **Eq 1 to Eq 3** and mark it as $I_{YIQ}(a,b,c)$.

$$Y = 0.299 \times R + 0.587 \times G + 0.114 \times B \quad (1)$$

$$I = 0.596 \times R - 0.275 \times G - 0.321 \times B \quad (2)$$

$$Q = 0.212 \times R - 0.523 \times G + 0.311 \times B \quad (3)$$

Step 2: Copy the I values of $I_{YIQ}(a,b,c)$ into another matrix $I_I(a,b)$.

Step 3: Record those pixel co-ordinates whose values lie between two threshold values T_1 and T_2 in $I_I(a,b)$. The values of T_1 and T_2 are considered as 20 and 90 respectively in this work.

Fig. 1 shows an example of skin region detection. The non-skin pixel values are set to white.

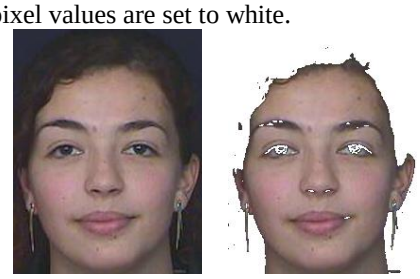

Figure 1. An example of skin region detection

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In the present work, for skin region detection only I color channel of the YIQ color model is needed so only equation Eq. 2 is used to get the I color channel of the YIQ color model from RGB image. While converting a RGB image to an image of YIQ color model, calculation for the values of I color channel, three multiplication, two subtraction operations are needed. Using only a single equation, this method improves both the space and time complexity of the proposed architecture which makes it simple and faster.

III. TOP LEVEL DESIGN

The top level design of Skin region detection architecture is shown in Fig 2. The proposed architecture takes one 8-bit value for each of the red, green, blue color channels for each pixel of the image as input. Then the system calculates only I color value of YIQ model using the taken three inputs. Further the system needs two 8-bit values as threshold inputs for the image which are shown in the top level design as Threshold1 and Threshold2. Finally, the system generates one 1-bit pixel value which is either 1 for the pixel for which I color value falls between Threshold1 and Threshold2 indicating skin region or 0 for those pixels for which I color value does not lie between Threshold1 and Threshold2 indicating non-skin region. Fig. 2 shows the top level design of the proposed architecture.

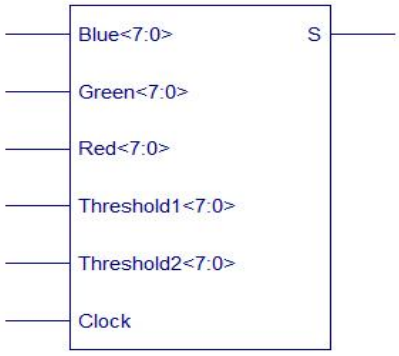
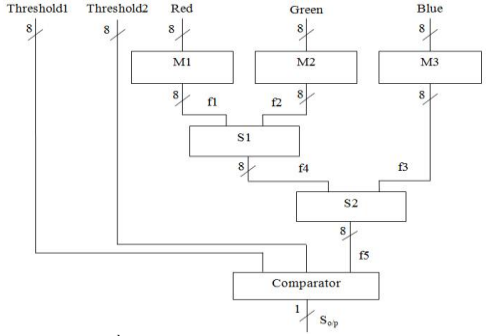


Figure 2. The top level design of Skin region detection architecture

IV. SYSTEM ARCHITECTURE

The proposed architecture for the Skin region detection algorithm is shown in Fig 3. The architecture contains three Multiplier blocks, two Subtractor blocks and one Comparator block. The modeling of the internal architecture of each block is designed using Very high-speed integrated circuit Hardware Description Language (VHDL) and each block is controlled by a global clock. The proposed architecture is implemented on Xilinx Spartan3 XC3S50-5PQ208 FPGA.



M_i : i^{th} Multiplier unit, S_i :Subtraction unit

Figure 3. System Architecture

The various blocks of this architecture are described next:

Multiplier Block

Each of these blocks takes one 8-bit color value for one of the Red, Green, Blue color channels of each pixel of the RGB image and Red, Green and Blue color value is multiplied by the fractional value 0.596,0.275,0.321 respectively. The first block calculates the value of f1, the second block calculates the value of f2 and the third module calculates the value of f3 as shown in the architecture.

Subtractor Block

This block subtracts two 8-bit pixel values, takes the absolute value of the result and produces the result in 8-bit pixel value. The first module calculates the absolute value of the difference between f1 and f2 and produces the value of f4. Similarly, the second module calculates the absolute value of the difference between f4 and f3 and produces the value of f5.

Comparator Block

The comparison of the resultant values from a given threshold value is performed by this block. The output of this block is that skin detected binary image having only two pixel values i.e. 0 and 1. This block produces a 1 value if the f5 is greater than the Threshold1and less than Threshold2 and produces a 0 value otherwise.

V. EXPERIMENTAL RESULTS

The Skin region detection architecture was implemented on VHDL, synthesized for a Xilinx Spartan 3 XC3S50-5PQ208 FPGA with simulation on the Modelsim 6.2c from Mentor Graphics Corporation. The test RGB images with varying size are used.

The proposed architecture operates taking maximum period 3.497ns per pixel using only 3% , 2%, 2%, 33% of Slices, Slice Flip-flops,4 input LUTs, Bonded IOBs respectively The device utilization summary for the proposed method is given in Table I.

FIGURE 4. DEVICE UTILIZATION SUMMARY OF PROPOSED ARCHITECTURE

	Device	No. of Slices	No. of Slice Flip Flops	No. of 4 input LUTs	No. of Bonded IOBs
Our Method	Xilinx Spartan 3 -XC350 00	30	41	33	41
		768	1536	1536	124
		3%	**2%**	**2%**	**33%**

The proposed architecture uses less system resources but operates faster at the speed of 285.919 MHz compared to the other two existing architectures [14][15].

The proposed architecture uses only 3% Slices, 2% of Flip-flops, 2% 4 input LUTs whereas the Quartus II architecture needs 22% of logic elements, 15% of the registers and 11 % of the memory resource. Table II shows the comparison study of device utilization of proposed FPGA architecture and the Quartus II architecture given by Guangdong Liu and Zhongke Shi[14].

TABLE I. COMPARISON STUDY OF DEVICE UTILIZATION BETWEEN PROPOSED ARCHITECTURE AND THE ARCHITECTURE GIVEN BY GUANGDONG LIU AND ZHONGKE SHI

	Device	Logic elements /Slices	Registers /Flip Flops	Memory /LUTs
Guangdong L. and Zhongke S.	**Quartus II**	**22%**	**15%**	**11%**
Our Method	Xilinx Spartan3 -XC35000	**3%**	**2%**	**2%**

The proposed architecture also uses less system resource although synthesized in older version Xilinx Spartan 3 XC3S50-5PQ208 FPGA of compared to the other existing architecture synthesized on Xilinx Spartan-3 XC35000 FPGA Table III shows the comparison study of device utilization of proposed architecture and the architecture given by Y.M. Mustafah and A.W. Azman[15].

TABLE II. COMPARISON STUDY OF DEVICE UTILIZATION BETWEEN PROPOSED ARCHITECTURE AND THE ARCHITECTURE GIVEN BY Y.M. MUSTAFAH AND A.W. AZMAN

	Device		No. of 4 input LUTs	No. of Bonded IOBs
Y.M. Mustafah and A.W. Azman	Xilinx Spartan3 -XC35000	Usage	3154	21
		Total	33280	104
		%	**9%**	**20%**
Our Method	Xilinx Spartan 3 -XC35000	Usage	33	41
		Total	1536	124
		%	**2%**	**33%**

The proposed architecture operates in much higher speed 285.919 MHz compared to the other two existing model. Table IV shows the comparative maximum operating speed that the proposed architecture and the existing two architecture.

TABLE III. COMPARISON STUDY OF TIMING SUMMARY

Architecture	Max. Frequency	FPGA Version
Guangdong L. and Zhongke S.	112.6 MHz	Quartus II
Y.M. Mustafah and A.W. Azman	96 MHz	Xilinx Spartan-*3 XC35000 FPGA*
Our Method	285.919 MHz	Xilinx Spartan 3 XC3S50-5PQ208 FPGA

The snapshot of device utilization summary and timing analysis report is shown in Fig. 4

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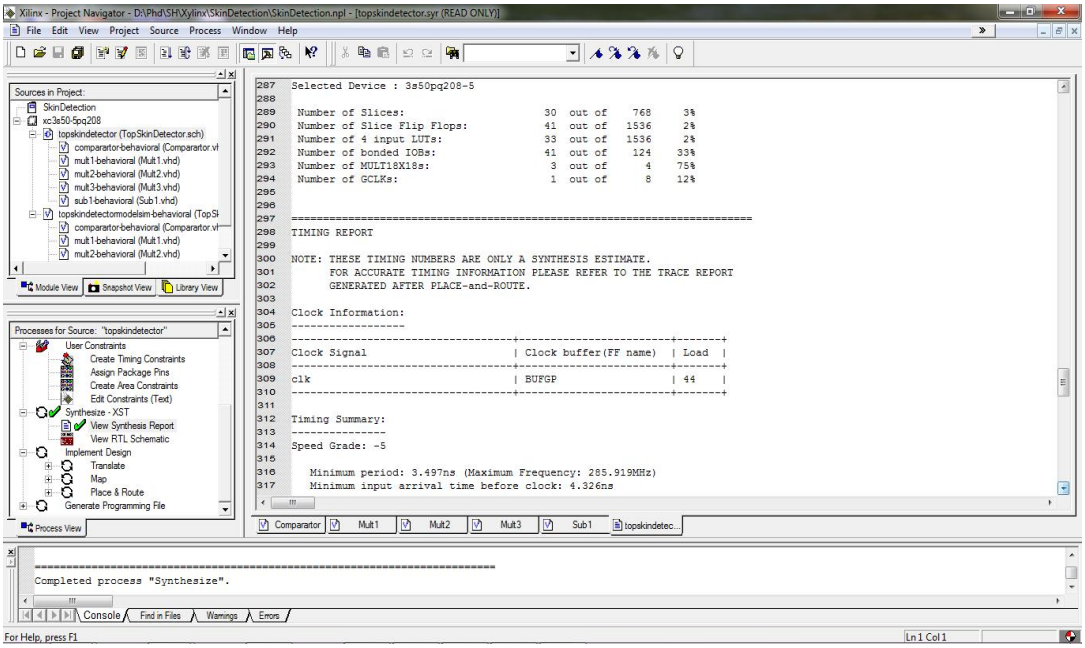
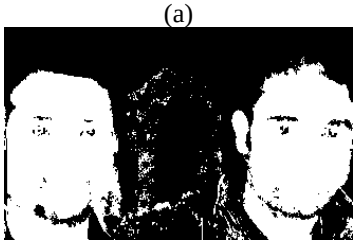


Figure 5. Snap shot of Device utilization summary and Timing Report

Fig. 5 to Fig. 8 show the experimental results obtained from the proposed architecture.

(a)



(b)

Figure 6. Result of Skin region detection a) Original image b) Detected skin region

(a) (b)

Figure 7. Result of Skin region detection a) Original image b) Detected skin region

(a) (b)

Figure 8. a) Original image b) Detected skin region

(a)

(b)

Figure 9. Result of Skin region detection a) Original image b) Detected skin region

VI. CONCLUSION

This paper presents an efficient FPGA based architecture for skin region detection algorithm in respect of both time and space complexity. Various skin region detection algorithms are typically used in image processing. In this paper, the methodology of Zhang et al. has been used to design the hardware module for skin region detection. This algorithm is chosen due to its property of simplicity resulting in faster computation. The result shows a significant improvement of time and space complexity over the existing architectures and the module is able to operate at the speed of 285.919MHz which is more than the twice of the operating speed of the existing architectures.

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REFERENCES

1. T Q.H. Thu, M. Meguro, M. Kaneko, (2002), “Skin-color extraction in images with complex background and varying illumination”, Sixth IEEE Workshop on Applications of Computer Vision.
2. D. Saxe, R. Foulds, (1996), “Toward robust skin identification in video images”, AFGR96.
3. S. McKenna, S. Gong, Y. Raja, (1998), “Modeling facial colour and identity with Gaussian mixtures”, Pattern Recognition 31 (12) pp. 1883–1892.
4. C. Garcia, G. Tziritas, (1999), “Face detection using quantized skin color regions merging and wavelet packet analysis”, IEEE Trans. Multimedia 1 (3) pp. 264–277.
5. N. Sebe, T. Cohen, T.S. Huang, T. Gevers,(2004), “Skin detection a Bayesian network approach”, ICPR04..
6. A. Hadid, M. Pietikinen and B. Martinkauppi, (2002), “Color-Based Face Detection using Skin Locus Model and Hierarchical Filtering”, Proceedings. 16th International Conference on Pattern Recognition, pp. 196 – 200.
7. Zhang H., D. Zhao, W. Gao, X. Chen, “Combining Skin Color Model and Neural Network for Rotation Invariant Face Detection”, ICMI 2000. LNCS, 1948: 237–244. Springer, Heidelberg, 2000.
8. D. Chai, and K.N. Nghan,(1999), “Face Segmentation using Skin Color Map in Videophone Applications”, IEEE Transactions on Circuits and Systems for Video Technology, Vol. 9, No. 4.
9. D. Bhattacharjee, S. Halder , M. Nasipuri, D.K. Basu, M. Kundu, (2009), “Construction of Human Faces from Textual Descriptions”, Soft Computing - A Fusion of Foundations, Methodologies and Applications, Vol. -15, No. – 3, pp. 429-447.
10. Michael John, and Sebastian Smith. (1997). “Application Specific Integrated Circuits”, Pearson Education.
11. Jenkins, Jesse H. (1994). “Designing with FPGAs and CPLDs”, Prentice-Hall Publications.
12. Weste, Neil H. and Eshraghian, Kamran (2000). “Principles of CMOS VLSI Design: A Systems Perspective”, Pearson Education Asia.
13. Wakerly, John F. (2002). “Digital Design: Principles and Practices”, Pearson Education Asia.
14. Guangdong Liu; Zhongke Shi, (2011) "Embedded implementation of real-time skin detection system," Transportation, Mechanical, and Electrical Engineering (TMEE), IEEE International Conference on , vol., no., pp.2463,2466, 16-18 Dec. 2011, doi: 10.1109/TMEE.2011.6199720.
15. Mustafah, Y.M.; Azman, A.W. (2012), "Skin region detector for real time face detection system," Computer and Communication Engineering (ICCCE), 2012 International Conference on , vol., no., pp.653,658, 3-5 July 2012, doi: 10.1109/ICCCE.2012.6271269.