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Waveform Analysis of New Diode Clamped and Cascaded H-Bridge Multilevel Inverters with PWM Technique

N. Mohan Teja, R S Ravi Sankar, Talath Anjum, P.Sanjay

Abstract*— This paper presents the waveform analysis of new diode clamped and cascade H-bridge multilevel inverters using Pulse width modulation technique. Multilevel voltage source converters are emerging as a new breed of power converter options for high-power applications. The multilevel voltage source converters typically synthesize staircase voltage wave from several levels of dc capacitor voltages. One of the major limitations of the multilevel converters is the voltage unbalance between different levels. The techniques to balance the voltage between different levels normally involve voltage clamping or capacitor charge control. An analysis of how existing multilevel carrier-based PWM affect switch utilization for the different levels of a new diode clamped and H-bridge inverter are conducted and compared.

Index Terms – Clamping Diodes, cascaded H-bridge inverter, Multi Level Inverter, Pulse Width Modulation

I. INTRODUCTION

The concept of multilevel converters has been introduced since 1975. The term multilevel began with the three-level converter. Subsequently, several multilevel converter topologies have been developed. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output. However, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency pulse width modulation (PWM). The attractive features of a multilevel converter can be briefly summarized as follows. Staircase waveform quality: Multilevel converters not only can generate the output voltages with very low distortion, but also can reduce the dv/dt stresses; therefore electromagnetic compatibility (EMC) problems can be reduced. Multilevel converters produce smaller Common-mode (CM) voltage.

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Therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced. Switching frequency: Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency. Among the best known topologies are the H-bridge cascade inverter, the capacitor clamping inverter (imbricated cells), and the diode clamping inverter.

II. CASCADED H-BRIDGE WITH SEPARATE DC SOURCES MULTILEVEL INVERTERS

A relatively new converter structure, cascaded-inverters with separate dc sources (SDC's) is introduced here. This new converter can avoid extra clamping diodes or voltage balancing capacitors. Each SDC is associated with a single-phase full-bridge inverter. The phase output voltage is synthesized by the sum of four inverter outputs, i.e., $V_1 + V_2 + V_3 + V_4$. The "level" in a cascaded-inverters based converter is defined by m = 2s + 1, where m is the output phase voltage level, and 's' is the number of dc sources. For example, a 9-level cascaded inverters based converter will have four SDC's and four fullbridges.
The basic cascaded H-bridge inverter is as shown in the Figure 1.

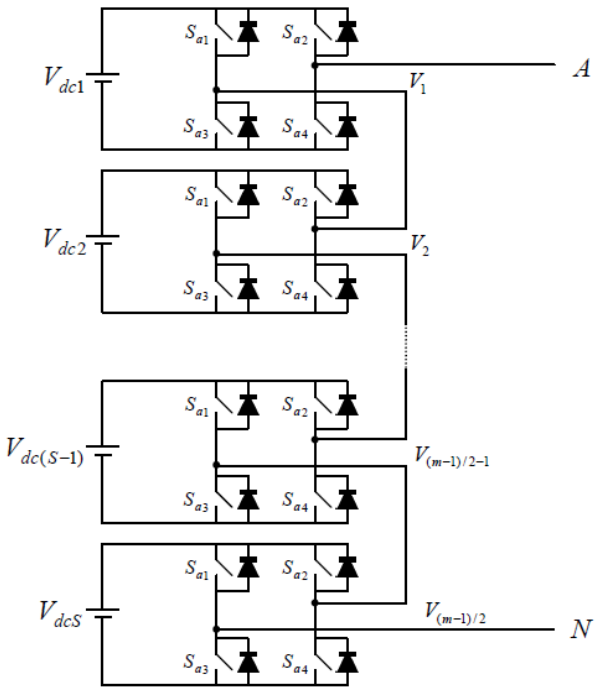

Fig. 1 Circuit Diagram of cascaded H-bridge Inverter

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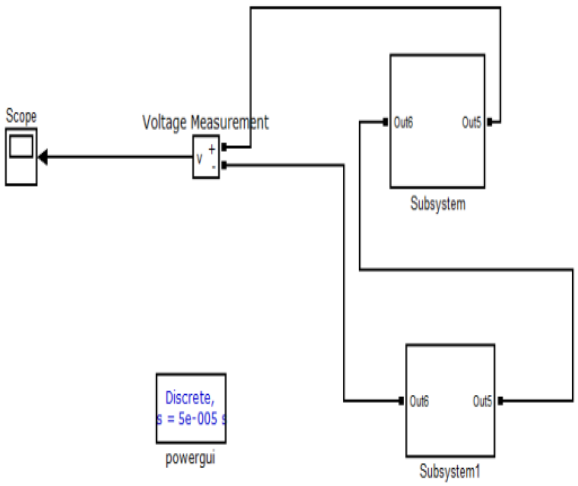

Fig. 2 Simulink of H-bridge Inverter

III. NEW DIODE CLAMPED MULTI LEVEL INVERTER

The new diode clamping inverter is shown in Fig. 2. For the five-level case, a total of eight switches and twelve diodes of equal voltage rating are used, which are the same with the conventional diode clamping inverter with diodes in series. This pyramid architecture is extensible to any level unless otherwise practically limited. A M-level inverter leg requires (M-1) storage capacitors, 2(M-1) switches and (M-1) clamping diodes

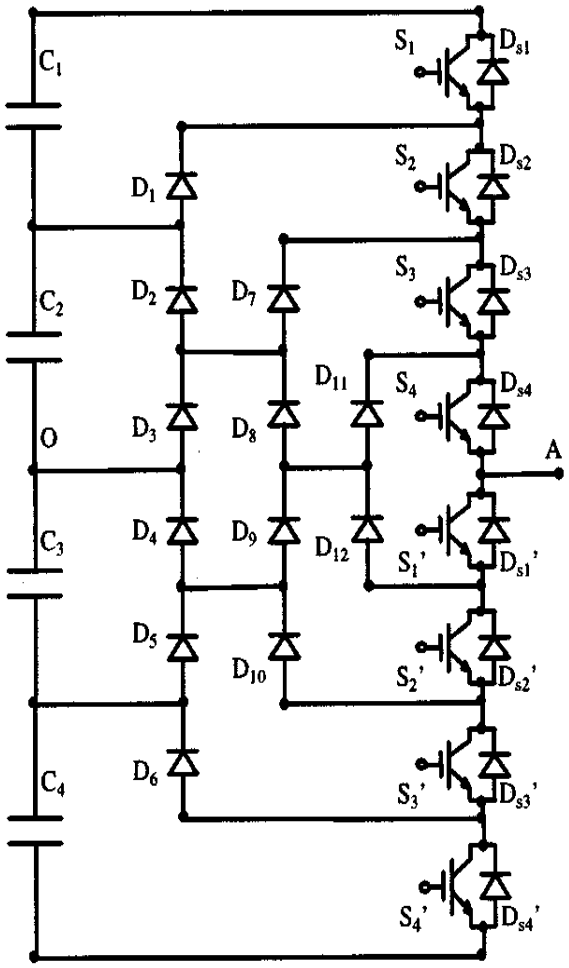

Fig. 3 Circuit Diagram of Five Level New Diode Clamped Inverter

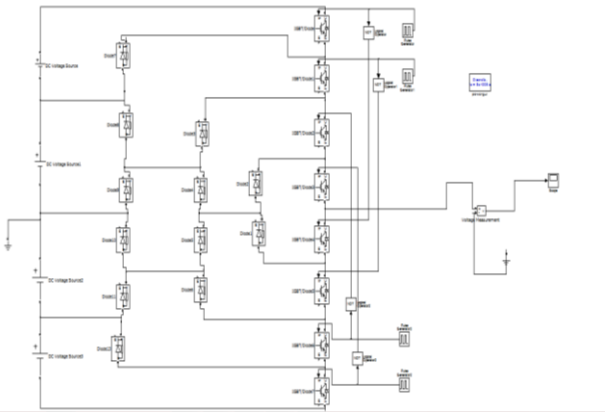

Fig. 4 Simulink of New Diode Five Level Inverter

IV. SINUSOIDAL PULSE WIDTH MODULATION TECHNIQUE

For an m-level inverter, m-1 carriers with the same frequency fc and same peak-to-peak amplitude A_c are disposed such that the bands they occupy are continuous. The reference, or modulation, waveform has peak-to-peak amplitude A_m and frequency f_m, and it is centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on and if the reference is less than a carrier signal, then the active device corresponding to that carrier is switched off. In multilevel inverters, the amplitude modulation index, m_a and the frequency ratio m_f are defined as

$$m_a = \frac{A_m}{(m-1)A_c} \qquad \textit{Equation – 1}$$

$$m_f = \frac{f_c}{f_m} \qquad \textit{Equation – 2}$$

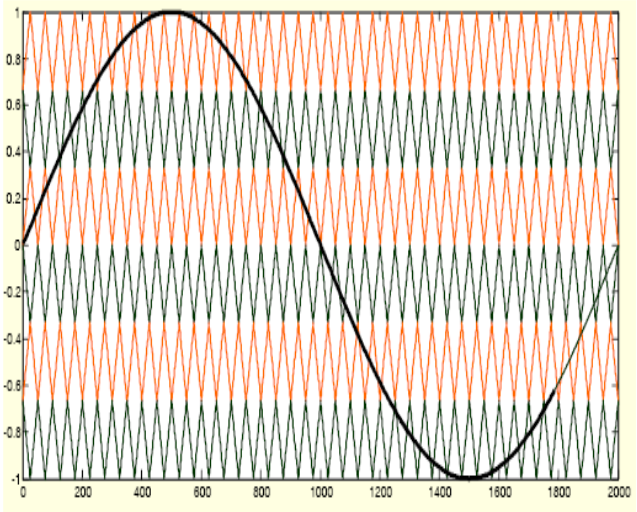

Fig. 5 Sinusoidal Pulse Width Modulation Technique

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V. SIMULINK MODELS OF MULTILEVEL INVERTERS WITH PWM TECHNIQUE

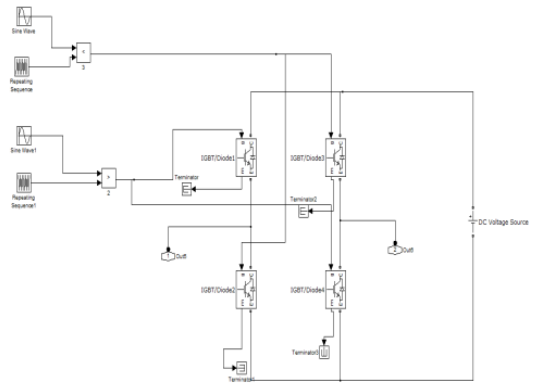

Fig. 6 Simulink subsystem of PWM based cascaded H-bridge Inverter

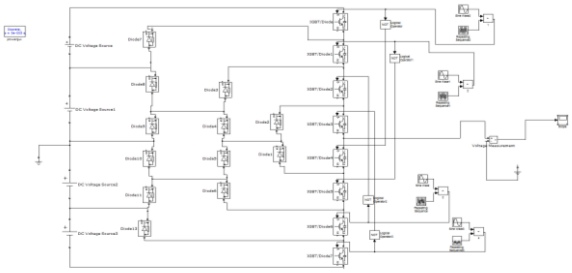

Fig. 7 Simulink of PWM based Five Level New Diode Clamped Inverter

V. SIMULATION RESULTS FOR DIODE CLAMPED INVERTER

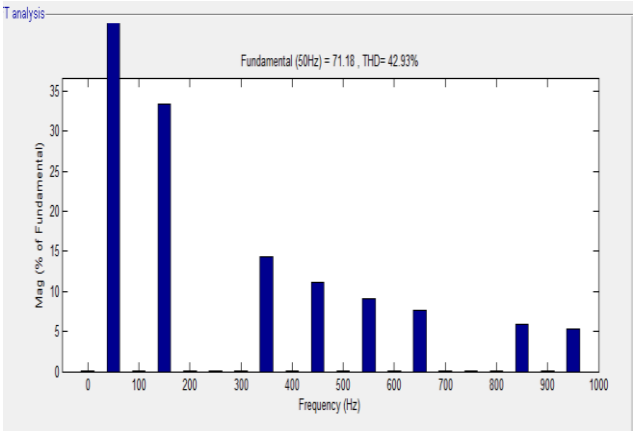

Fig. 8 THD of five level h bridge inverter

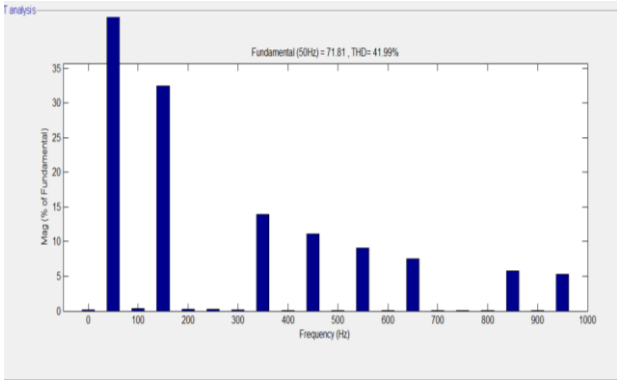

Fig. 9 THD of Five Level New Diode Clamped Inverter

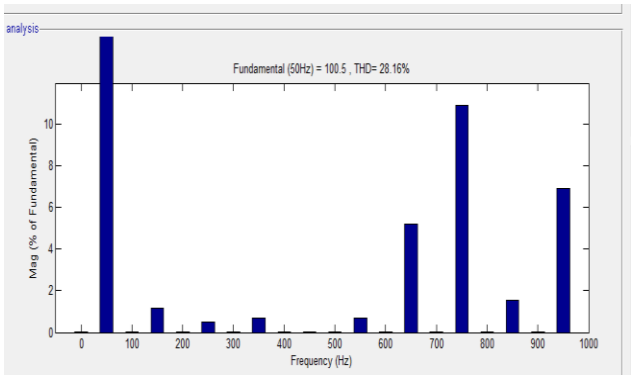

Fig. 10 THD of 5-level H-bridge inverter with PWM Technique

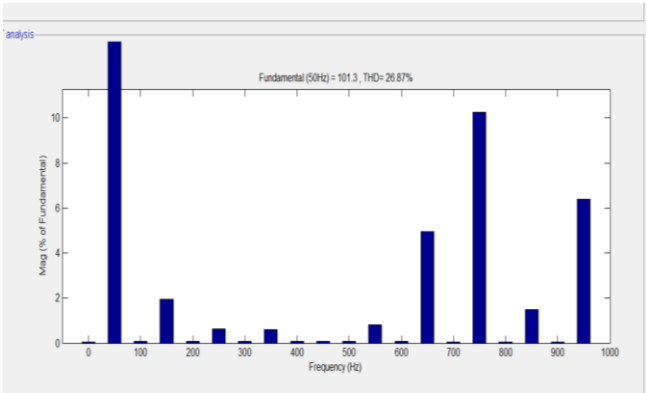

Fig. 11 THD of Five Level New Diode Clamped Inverter with PWM Technique

VI. WAVEFORMS OF NEW DIODE CLAMPED AND CASCADED H-BRIDGE INVERTERS (FIVE LEVEL)

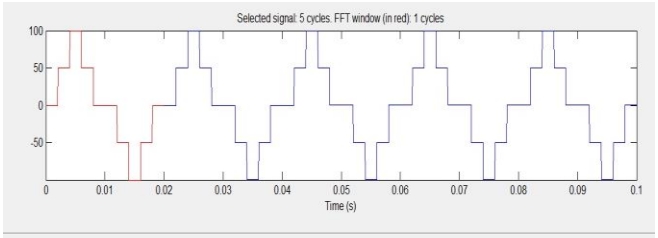

Fig. 12 Simulation Result for Line voltages of 5-level H-bridge Inverter

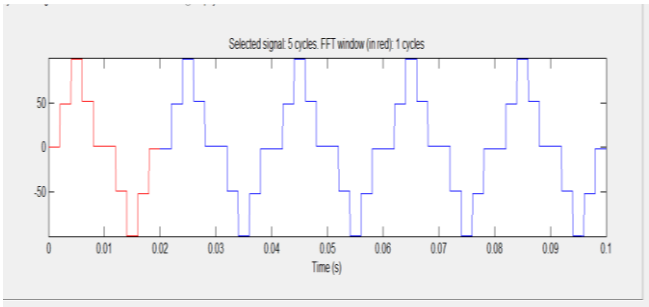

Fig. 13 Simulation Result for Line Voltages of Five Level New Diode Clamped Inverter

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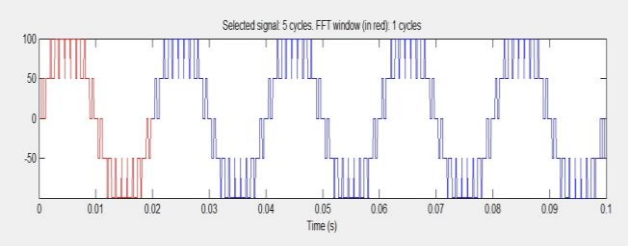

Fig. 14 Simulation Result for Line Voltages generated using PWM Technique of Five Level H-bridge Inverter

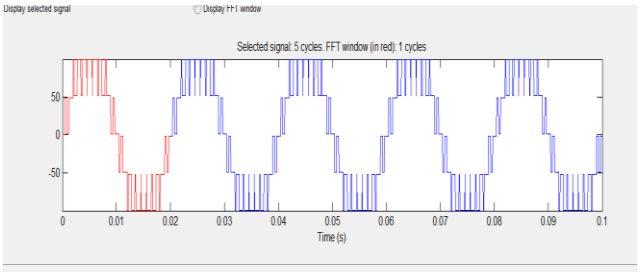

Fig. 18 Simulation Result for Line Voltages generated using PWM technique of Five Level New Diode Clamped Inverter

VII. PERCENTAGE TOTAL HARMONIC DISTORTION ANALYSIS OF H-BRIDGE MULTILEVEL INVERTER WITH DIFFERENT LEVELS USING PWM

Cascaded H-bridge clamped inverter (Levels)	%THD Without using PWM technique	%THD Using PWM technique
3 level	79.89	35.06
5 level	42.93	28.16
7 level	31.35	18.56
9 level	25.79	14.44

VIII. PERCENTAGE TOTAL HARMONIC DISTORTION ANALYSIS OF NEW DIODE CLAMPED MULTILEVEL INVERTER WITH DIFFERENT LEVELS USING PWM

Diode clamped inverter (Levels)	%THD Without using PWM technique	%THD Using PWM technique
3 level	79.43	33.98
5 level	41.99	26.87
7 level	30.25	16.93
9 level	24.62	12.45

IX. CONCLUSION

In this paper Pulse width modulation technique is applied on cascaded H-bridge and new diode clamped multilevel inverters and percentage of total harmonic distortions of several levels of inverter are simulated and compared. The simulated results are presented in this paper and it is concluded that PWM technique has given good fundamental spectrum (101.7%) and Total Harmonic Distortion (12.45%). As the number of levels increases the harmonic distortion also decreases. Comparing with the cascaded H-bridge multilevel inverter new diode clamped inverter has less Total Harmonic Distortion.

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