International Journal of Innovative Technology and Exploring Engineering (IJITEE)
ISSN: 2278-3075 (Online), Volume-3 Issue-11, April 2014

Digitization of Linearized Thermistor Output Using Dual Slope ADC

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Abstract - To measure the temperature using a thermistor, linearization of the thermistor output to compensate the inverse exponential nature of resistance-temperature characteristic is required. A linearized dual slope analog to digital converter (LDSDC) that takes thermistor as input and provides digital output is constructed here. A logarithmic amplifier that counterbalances the exponential nature is presented at the input of the LDSDC. The conversion logic of the dual slope ADC is suitably modified to obtain the required inversion and offset correction so as to obtain linearization over a wide range of temperature. The Time and Logic Unit of the system is constructed using a Field Programmable Gate Array(FPGA) with a high speed clock to ensure resolution of 20ns to have negligible effect of hysteresis loop. The efficiency of the proposed LDSDC is verified through simulation and is will be practically demonstrated through a prototype unit being built and tested upon. Analysis to identify different possible sources of error will thus be proposed.

Index terms- Dual Slope ADC, Field Programmable Gate Array(FPGA), Linearization, Thermistor.

I. INTRODUCTION

Thermistor is usually preferred for its low cost, high sensitivity and accuracy than the other temperature sensing devices. But the only drawback is that the output of the thermistor is nonlinear. Linearizing the thermistor's output and obtaining the equivalent digital value makes it highly compatible. Various methods for linearizing the thermistor output have been studied over time but they mostly lead to reduced sensitivity. The most common example is a resistor being placed in series or parallel to the thermistor. Linearization is also done only for a small range of temperatures. This was overcome by using a four constant fit instead of Bosson's three constant fit that is usually used for denoting the temperature-resistance relationship of a thermistor. The reciprocal time generator method and linear temperature-time converter are a few methods that were studied to obtain a wider range for linearization.

Manuscript published on 30 April 2014.
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Various methods that used multivibrators for the purpose of linearization were also a case of study. These didn't provide linearization over a wide range of temperature. Also different types of multivibrators provided varying degrees of linearization, with the astable multivibrator being the only type that provided linearization over a wide range of temperature.

A delay network used in temperature to frequency converter that made use of an oscillator also resulted in linearization over a considerable range of temperature. However, the methods that were studied do not achieve linearization over the entire range of operation of the thermistor. This preserves the high sensitivity.

Analogue techniques were then followed by software based computing techniques. This involved making use of 'loop up tables' and 'maps'. Iterative linearization of the output of thermistor based circuits is recently carried out by artificial neural networks. The disadvantage of these methods is the sole dependence on computing for finding the best polynomial fit for the equations.

Analog to digital converters are used for obtaining the digital output that can be directly fed to digital instruments. This makes ADC an important part of the linearization circuit. This paper presents the log amplifier for linearization and a dual slope ADC for digitization of the output.

II. MODEL OF LDSDC SUITABLE FOR THERMISTORS

The equation derived by Bosson et al is given as

$$R_\theta = Ae^{\frac{\beta}{\theta+\gamma}} \quad (1)$$

this shows the relation between RΘ, the resistance of the thermistor to the temperature, θ. A is a parameter that is dependent on the material and geometry of the thermistor and B depends only on the material property.

To obtain a linear graph such that the output is directly proportional to temperature the following steps are performed to equation (1):

Applying natural logarithm to equation (1) we get the equation as

$$\frac{\beta}{\theta+\gamma} = lnR_\theta - lnA \quad (2)$$

The next step is to express equation (2) in terms of temperature θ:

$$\theta = \frac{\beta}{lnR_\theta - lnA} \quad (3)$$

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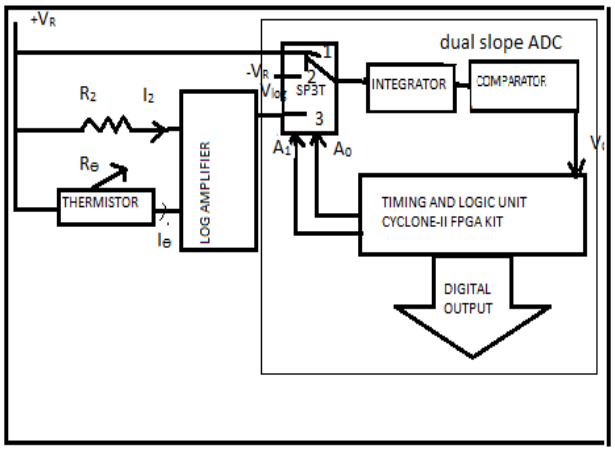

Fig.1: Circuit diagram of LSDSC

In general the V_{log} of logarithmic amplifier is obtained by logarithmic ratio of two currents. Two currents are derived from a single DC reference voltage. Output of logarithmic amplifier is

$$V_{log} = ln(R_\theta) - ln(R_A) \quad (4)$$

Comparing equation (3) and (4) we get $Ra = A$ and therefore we get the equation

$$V_{log} = ln(R_a) - ln(A) \quad (5)$$

Output of the logarithmic amplifier is given as input to dual slope ADC. The ADC consists of an RC integrator, a comparator and a Time and Logic Unit (TLU). The design of TLU is such that it performs two integrations by controlling input to integrator through a single pole 3- way analog switch. Two inputs of the switch are connected to $+V_r$ and $-V_r$ and the third input of switch is connected to V_{log}.

The switch is connected to the lines A_0 and A_1 coming from the TLU. If $A_1A_0 = 01$, then position 1 is selected on the switch and $+V_r$ is the input to the integrator. If $A_1A_0 = 10$, position 2 is selected and $-V_r$ is the input to the integrator. If A_1A_0=11, then the output of the log amp is given as the input to the integrator and if $A_1A_0 = 00$ then the output is forbidden. The integrator output (V_{oi}) is then fed into the comparator whose output V_c is given to TLU. If $V_{oi} > 0$ then $V_c = 1$ else $V_c = 0$. The timing logic inside the TLU is got by either an N-bit or N-digit pre-settable up or down time counter. This timer logic is implemented using FPGA and it is driven by a clock period of T_c. Before the process of conversion of V_{log} can begin, it should be noted that the integrator output is zero. So auto-zero phase is necessary whenever a conversion command is issued freshly.

A. *Auto zero phase*

When the convert command is given in the circuit, initially in the circuit output of the integrator V_{oi} is negative due to which the comparator output V_c is low. V_c being low is sensed by TLU and the control logic $A_1A_0 = 10$ so that $-V_r$ is connected to fixed reference, R. Due to this a constant $I_c = V_r/R$ starts flowing through the capacitor C and the output graph ramps upto zero. At the same time, V_c changes from low to high. When the control logic $A_1A_0 = 01$, V_r gets connected and I_c flows through C causing a current $-V_r / R$ to flow through the capacitor.

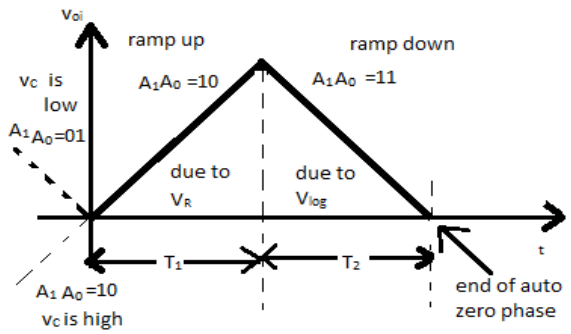

Fig.2: Output of integrator

B. *Conversion Phase*

After the auto zero phase the integrator output V_{oi} becomes equal to zero. At this time a conversion phase is initiated either at the end of the auto zero phase or end of previous conversion phase. The logic of ADC used here and the conventional dual slope ADCis different. In conventional Dual slope ADC the integrator input is connected to the input voltage to be converted. Here integration is performed with integrator input being connected to $-V_r$ and this can executed by keeping $A_1A_0 =$ "10". Again, V_{oi} ramps up with a positive slope. This state is maintained for a fixed time period of T_1, where $T_1 = N_1T_c$. N_1 is a preloaded value in the register and this is accomplished by preloading the timer counter register (N_{TLU}).

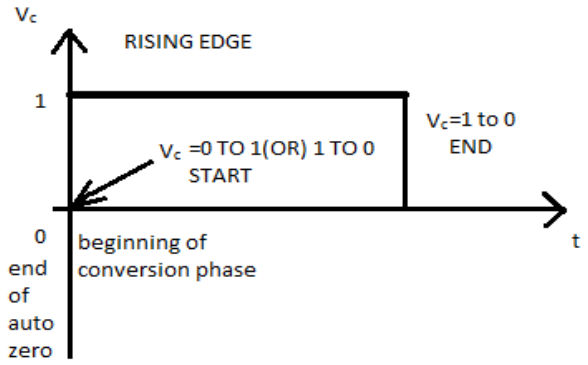

Fig.3: Output of comparator vs. time

The next step is to check whether TLU has reached zero. Once it has reached 0, A_1A_0 = "11" thus switching to input the output of the logarithmic amplifier. Then the N_{TLU} timer counter value is preset with the value $(N_{fs} - N_k)$. The counter rolls to zero after reaching N_{fs} $For\ example, N_{fs} + 1 = 0000$). Logarithmic output is always positive so the V_{oi} starts to ramp down with a slope V_{log}/RC. The total charge acquired by capacitor C over the conversion phase is zero. We get the following equations:

$$(V_r/R_c) * T_1 = (V_{log}/RC) * T_2 \quad (6)$$

$T_1 = N_1T_c$, where Tc is the time period of TLU clock and

$$T2 = (N_k + N_2)Tc$$

At the end of time period T_2, TLU gives the output N_2. N_k is a constant dependent on the thermistorcharacteristic. The total charge acquired by capacitor is zero and hence we come to the conclusion that:

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$$(Vr/RC) * T1 = (V_{log}/RC) * T2 \quad (7)$$

$$V_r(N_1T_c) = V_{log}(N_k + N_2)Tc$$

And hence,

$$N_2 = \Theta \quad (8)$$

III. RESULTS AND DISCUSSIONS

The figure as shown below is the linearized output of the proposed circuit when applied theoretically for dynamic range of temperatures.

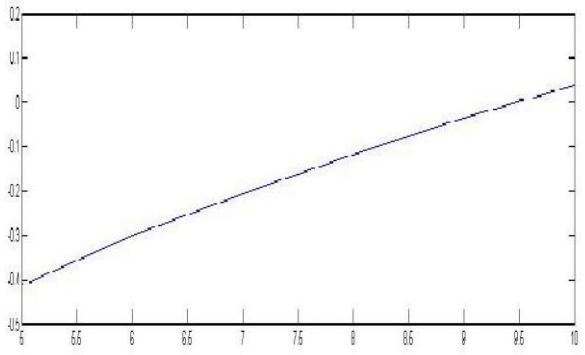

Fig.4: Linearized output

Error percentage for the above linearized output is calculated to be varying from 0.09-11% when applied practically and theoretically, after various approximations. Output of the linearized curve of the thermistor proves forimproved accuracy for different values. Error caused by self-heating of the thermistor is compensated by limiting the current through thermistor or selecting a thermistor with large dissipation constant. The comparator may have a time delay different from that of the switch which responds depending on the digital output. When calculating the time delay, delays caused due to comparator and switch is negligible and does not have an effect on the output and can be avoided . Offset voltage of the comparator will not produce errors in the process if the offset voltage is considered to be negligibly small and does not have any change during the conversion phase. Therefore, it does not affect the LDSDC of the circuit. The assumption of the resistance connected to the reference voltage through a three way switch will have an effect, causing gain error. This is caused due to discrepancy in the ON resistance which results in offset at output. The high clock speed from the FPGA kit will gives us a greater resolution thereby making hysteresis loop a negligible phenomenon.

IV. CONCLUSIONS

The exponential relationship of the resistance-temperature determined from the output of the thermistor is measured for dynamic range of temperatures fed as input to the LDSDC to give a linearized output is analyzed theoretically using MULTISIM software. The characteristic response of the LDSDC was studied and reviewedin detail with varying inputs to obtain accurate results with the calculation of error accuracies and to ameliorate the performance of the proposed method. The various errors that are obtained in practical and theoretical cases are studied and its implementation suggests ways of mitigating the error. Thus, by incorporating the given circuit and mitigating errors by the method suggested, we can use the thermistor for a wider range of its operational functionality as a temperature sensing element. It can be used for temperature-tracking power supplies amongst other applications.

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