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Study of Sense Amplifier for Low offset High Speed SRAM Memory Design

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Abstract— The sense amplifiers is a main peripheral of CMOS memory and play an important role to overall delay, offset, speed , memory access time and power dissipation of the memory and to improve the speed performance of a memory, and to provide signals which conform to the requirements of driving peripheral circuits within the memory, sense amplifiers are applied. In this paper we present study and literature survey of low offset and high speed low power sense amplifier architecture selection for SRAM memory design application and in this paper also present the comparison voltage mode sense amplifier and current mode sense amplifier. Presented Sense amplifier CMOS schematic is design tanner EDA S-edit , Simulate T-spice and 0.13µm technology.

Index Terms—Sense amplifier, current mode sense amplifier, offset, Intrinsic offset.

I. INTRODUCTION

Sense amplifiers are one of the very important peripheral components of CMOS memories. Sense amplifiers are one of the most essential circuits in the periphery of CMOS memories. Sense amplifiers are used to translate small differential voltage to a full logic signal that can be further used by digital logic. The need for increased memory capacity, higher speed, and lower power consumption has defined a new operating environment for future sense amplifiers. Sense amplifiers are mainly used to read the contents of memory (SRAM and DRAM) cells. [1] The performance of sense amplifier affects both memory access time and overall memory power dissipation. CMOS memories are required to increase speed, improve capacity and maintain low power dissipation. These goals are conflicting when it comes to sense amplifier designs RAM cells are known to be highly sensitive to process variations due to the extremely small device sizes. Due to the high demands on the portable products, power consumption is a major concern in VLSI chip designs [1].Today analog CMOS memory design generally speed, power and area are considered as the crucial point. One of the parameter can be achieved with compromisation of other two [4]. The main function of the sense amplifier is to amplify the small voltage swing (voltage difference of bit lines) in large bit line, reduce delay, and power dissipation by reducing large voltage swing.Applications of Sense Amplifier:

i. Automotive Current Monitoring: They monitor supply rails that may need to be powered down to control heat and power dissipation. Consequently, high accuracy is paramount to ensuring reliability and extending battery life. For this we use sense amplifier.
ii. Battery Chargers: Current-sense amplifiers are critical components in portable devices. These small integrated circuits (ICs) are typically used to measure battery charge and discharge currents.
iii. Photovoltaic Systems: Photovoltaic system usually employs a battery bank to store the energy to take care of the uncertainty in availability of solar radiation due to its statistical nature in the biosphere. This entails the use of a sense amplifier to monitor and control the charging of a battery-bank.

One of the major issues in the design of SRAMs is the memory access time (or speed of read operation). For having high performance SRAMs, it is essential to take care of the read speed both in the cell-level design and in the design of a clever sense amplifier. Sense amplifiers are one of the most critical circuits in the organization of CMOS memories. Their performance strongly influences both memory access time and overall memory power consumption. High density memories commonly come with increased bit line parasitic capacitances. These large capacitances slow down voltage sensing and makes bit line voltage swings energy-consuming, which result in slower more power hungry memories. Need for larger memory capacity, higher speed, and lower power dissipation imposes following tradeoffs in the design of sense amplifier:

i. Increase in number of cells per bit line increases the bit line parasitic capacitance.
ii. Increasing cell area to integrate more memory on a single chip reduces the current that is driving the heavily loaded bit line. This causes smaller voltage swing on the bit line.
iii. Decreased supply voltage lead to smaller noise margin that affects the sense amplifier reliability.

II. LITERATURE REVIEW

Sense amplifier the main circuits used in the memory design. There are mainly two types of sense amplifiers and they can be categorized in current mode and voltage mode sense amplifier. Current mode sense amplifier detects the current difference between the bit lines and voltage mode sense amplifier detects the voltage difference between the bit lines to determine whether a “0” or a “1” is stored in the memory cell .It amplifies the voltage signal and transfers it on the output circuits. Various architectures of sense amplifiers are available in literature. We will discuss following architectures**.**

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A. Current mode PMOS Biase type sense amplifier

Ardalan,S et al are proposed current mode PMOS Bias type sense amplifier .the fundamental reason for applying current -mode sense amplifiers in sense circuits is their small input impedances and, in cross-coupled feedback configuration, their small common input/output impedances. Main advantage of small input and input/output impedances, which are coupled to a bit line, include significant reductions in sense circuit delays, voltage swings, cross talking, substrate currents and substrate voltage modulations.[4]

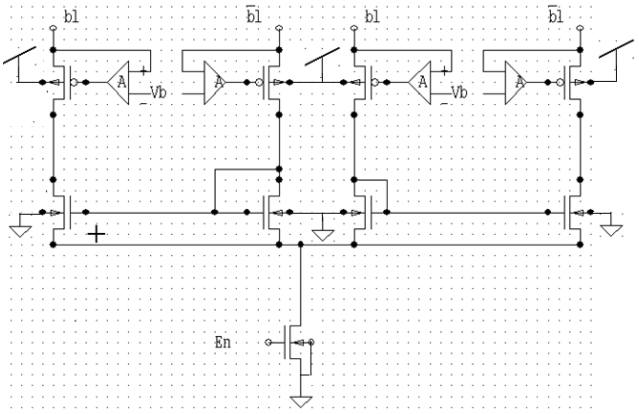

Figure1:PMOS Bias type (PBT6) Sense Amplifier [4]

Current amplification in memories is implemented almost exclusively in feedback circuits. Yet, numerous feedback circuits other than current amplifiers can also provide small input- or small common input-output impedances. Generally, sense amplifier input and output impedances may be optimized for specific memory cell type, load circuit, amplification and other requirements. Clearly, the design should use that amplifier type, or that combination of various amplifiers, which provides the highest performance at the least costs when combined with the other parts of the sense circuit. This architecture includes two current mirror cells that copy the current of bit-lines and then subtract them and the outputs are complementary. PMOS transistors are used for the bit line loads .In this architecture the gain element has been used to increase the bit-line loads and to reduce the effect of bias voltage on delay.

Advantages:

- The active-load PBT architecture (PBT6) gives the best performance in terms of delay.
- The active-load PBT is not affected by changes in Vdd and bias voltage, and proves to be fairly robust.

Disadvantages:

The implementation of the differential gain element is critical to minimize the size of the overall sense amplifier, as well as the power consumed by the sense amplifier

B Enhanced Voltage Mode Sense Amplifier:

The performance of sense circuits can be improved by adding a few devices to the differential voltage sense amplifier. From the great variety of possible enhancements to the basic amplifier the evolution of the memory technology reduced the number of approaches to a few which can be efficiently implemented in CMOS memories;

- Temporary decoupling of the bit lines from the sense amplifiers,
- Separating the input and output in feedback sense amplifiers,
- Applying switchable constant current sources to the source devices,
- Optimizing the output signal amplitude

In memories that are designed with positive-feedback differential voltage sense amplifiers, obtainable sensing speeds are greatly reduced by the high load capacitances C_L is coupled to the sense amplifiers. Generally, C_L is dominated by the capacitance of the memory cells connected to the bit line and by the stray-capacitance of the bit line itself. A significant decrease in capacitance C_L requires major modifications in process technology and in sense circuit design. By a small design alteration, C_L may be reduced by placing a pair of MOS devices MT1-MT2 figure 2, or a pair of preamplifier, next to the sense amplifier inputs to decouple the bit line capacitance from the sense amplifier for the time of the initial high-gain amplification. At the time t_1, decouple devices MT1 and MT2 are turned on, the accessed memory cell generates a small signal difference $\Delta V_{SA}(t_1)$ on the bit line and on the inputs of the amplifier. During this time, the sense amplifier is inactive and the load on its input-output node is $C_L(t_1) = C_B + C_{SA}$, where C_B is the total bit line capacitance, and C_{SA} is the total input-output capacitance of the sense amplifier and $C_B >> C_{SA}$. The sense amplifier is activated at the time t_2 when $\Delta V_{SA}(t)$ achieves the minimum detectable amplitude defined by the operation margins. At the time t_2 devices MT1 and MT2 are turned off. Thus, MT1 and MT2 decouples the C_B from the sense amplifier input and reduces $C_L(t_1)$ to $C_L(t_2) = C_{SA}$, and with the smaller load capacitance $C_L(t_2)$, the sense amplifier can rapidly amplify $\Delta V_{SA}(t)$. At the time t_3 , when the amplified signal $\Delta V_{SA}(t)$ is large enough for rewriting the memory cell, decoupler devices MT1 and MT2 are turned on again, therefore $C_L(t_3) = C_{BL} + C_{SA}$ appears for the sense amplifier.[5]The switching of MT1 and MT2 may be eliminated by the application of depletion mode transistors and by cross-coupling MD1 and MD2 figure 2Pre-amplification in addition to decoupling can be obtained if MT1 and MT2 are designed to operate as a charge transfer or as another non-differential sense amplifier. The use of preamplifiers to a positive-feedback sense amplifier, nevertheless, may not result in a respectable speed improvement, because the increase in offsets and in parasitic capacitances and the preamplifiers' inherent delay counteract the speed gain obtained by pre-amplification.

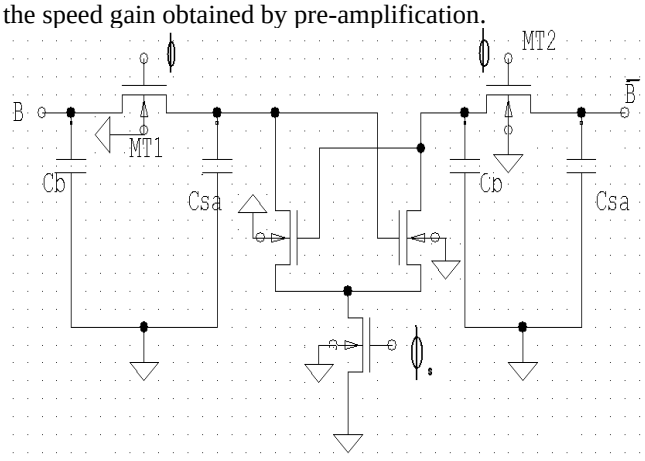

Figure 2: Decoupling of bit-line capacitances from a sense amplifier.[5]

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A widely applied sense amplifier show in figure 4 incorporates the decoupler transistors MT1 and MT2 by taking advantage of the sequential activation of n- and p-channel transistor triads MN3-MN4-MN5 and MP6-MP7-MP8.

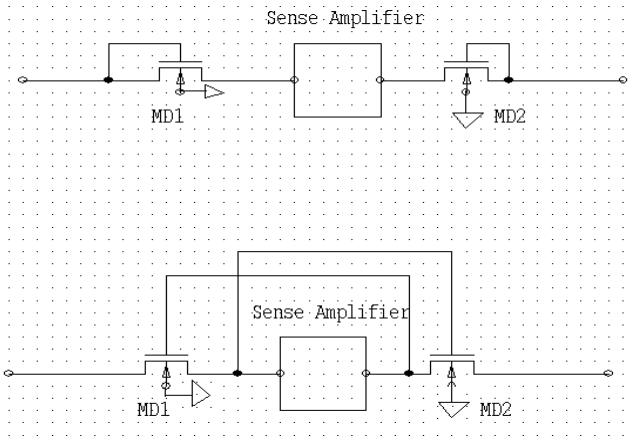

Figure 3: Decoupling provided by depletion mode and cross-coupled devices.[5]

Initially, clock Φs activates the n-channel triad and clock Φ_T turns devices MT1 and MT2 on. MT1 and MT2 are turned off, however, when the differential signal $V_d(t)$ between nodes 1and 2 reaches the minimum signal amplitude that is detectable by the sense amplifier. From this time, MN3-MN4-MN5 can amplify $V_d(t)$ rapidly, because the bit line capacitance CB is decoupled from nodes1 and 2. During this time CB appears on each nodes 3 and When Vd(t) exceeds an intermediate amplitude, e.g., Vd(t) = VT, ΦT turns on MT1 and MT2 again, and the sense amplifier provides a rapid complementary large signal amplification. The switching of MT1 and MT2 requires certain time, but the overall delay time of the sense amplifier may significantly be reduced by the temporary decoupling of the large bit line capacitances from the transistor triad MN3- MN4-MN5.

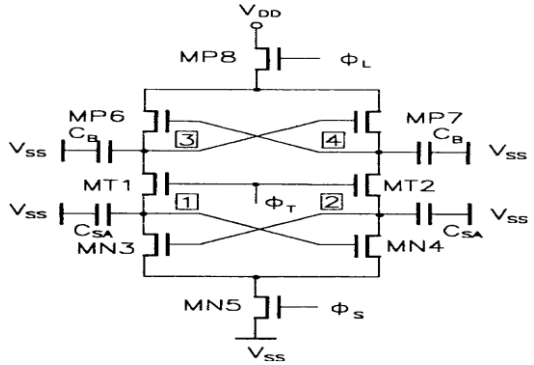

Figure 4: Voltage Mode Sense Amplifier incorporating decouple devices [5]

Advantages:

- Decoupling of the bit lines from the sense amplifiers, decrease the capacitive load of the sense amplifier and hence increase the sensing speed.
- Sense amplifier provides rapid complementary large signal amplification.

Disadvantages:

- This architecture is more complex than already described conventional sense amplifier.

B. Comparison of voltage mode and current mode sense amplifier

- Due to process variations like random dopant fluctuations, V_t of transistors have random variations which cause mismatch among neighboring transistors. This mismatch can induce trip point mismatch among the cross-coupled inverters of sense amplifiers and/or current mismatch in the evaluation branches of the sense amplifier circuit, resulting in operational failures.
- This type of failure mechanism is activated by current mismatch and this is not observed in Voltage mode Sense Amplifier since it does not operate base on current differential.
- Current mode Sense Amplifier shows more failure probability than Voltage Latch Sense Amplifier because it is susceptible to current mismatch.
- Dual V_t assignment is used in Current mode Sense Amplifier because it can control current flow through transistors while in case of Voltage mode Sense Amplifier; the best assignment is the original scheme where all transistors have low V_t.
- Sensing delay of Current mode Sense Amplifier is lower than that of Voltage mode Sense Amplifier because it decreases input bit line capacitance.
- Power dissipation in Current mode Sense Amplifier is more than that of Voltage mode Sense Amplifier.
- If we decrease probability of failure of sense amplifier, Sensing delay in Current mode Sense Amplifier is more than that of Voltage mode Sense Amplifier.
- Probability of failure due to process variation in Current mode Sense Amplifier is more than that of Voltage mode Sense Amplifier.
- We can decrease the probability of failure of both Current mode Sense Amplifier and Voltage mode Sense Amplifier with penalty of power and delay by optimizing the size of the transistors used in design.

III. SENSE AMPLIFIER

In figure 5 shows the full complementary positive feedback amplifier this schematic improve the simple positive feedback amplifier a by using an active load circuit. In figure sense amplifier transistor MP4, MP5 and MP6 in positive feedback configuration. In practically device pairs transistor MP4-MP5 and MN1 -MN2 can not be completely matched despite carefully symmetrical design. Usually the non-symmetricity between the p-channel MP4 and MP5 is more substantial than that between the n-channel MN1 and MN2, because most of the CMOS processes optimize n-channel device characteristics.

To avoid a large initial offset resulting from the added effects of imbalances in the NAND p-channel device pair, source devices MN3 and MP6 are not turned on simultaneously, but first the n-channel and later the p-channel complex is activated by impulses ΦS and ΦL respectively. The delayed activation of transistor triad MP4-MP5-MP6 by clock ΦL results that until the time MP6 is turned on, device triad MN1-MN2-MN3 operates alone.

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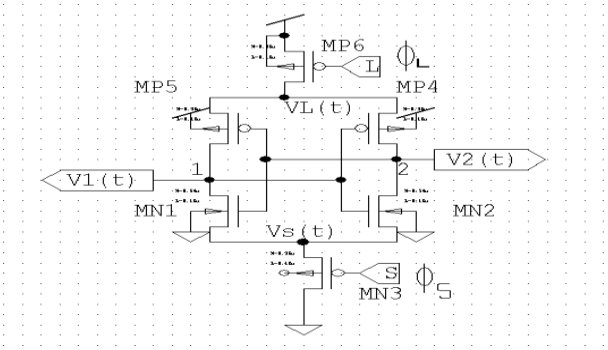

Figure 5: sense amplifier [8]

In figure sense amplifier when the sense signal on the bitline is large enough the drain-source voltage of either MN1 or MN2 reaches the saturation voltage VDSAT, clock ΦL activates triad MP4-MP5-MP6. The activated feedback in MP4-MP5-MP6 introduces a pair of time dependent load resistances r L l (t) = r d4 (t) + 2r d6 (t) and r L2 (t) = r d5 (t) + 2rd6 (t). Here, rd (t) is the time dependent drain-source resistance represent devices respectively MP4, MP5 and MP6. The resistances of these devices may be considered as time invariant parameters during the activation of MP6 tSAT , so that rL = r L1= r L2 may be used.[8]

In the transient analysis, the differential signal development time t_d during the presence of impulse ΦS until the appearance of clock Φ_L is determined by the switching time of the n-channel triad t_{dN}, and t_d is dominated by the transient time of the p-channel triad tdP .With this, the sense-signal development time in the full-complementary positive feedback differential voltage sense amplifier t_d may be approached as[8]

$$t_d = t_{dN} + t_{dP} \approx t_{dN} \log \frac{V_{DSAT}}{2\Delta V_0} + t_{dp} \ln \frac{0.9(V_{DD}-V_{FR})}{V_{DSAT}} \quad (1)$$

Where

$$t_{dN} \approx \frac{C_B + C_{GSN} + 4C_{GDN}}{\beta_N [V_{FR} - V_S(0) - V_{TN}(V_{BC})]} \quad (2)$$

$$t_{dP} \approx \frac{C_B + C_{GSP} + 4C_{GDP}}{\beta_P [V_L(0) - V_{FR} - |V_{TP}(V_{BC})|]}) \quad (3)$$

In above equations indicates N and P designate n- and p-channel, devices, VDSAT is the saturation voltage, ΔVo is the amplitude of the initial voltage difference generated by the accessed memory cell on nodes 1 and2 , VPR is the precharge voltage, CB is the bitline capacitance, CGS and CGD are the gate source and gate-drain capacitances, and β is the individual gain factor for devices MN1, MN2, MP4 and MP5, vS(0) and vL(0) are the initial potentials on the drains of device MN3 and MP6, VT is the threshold voltage and VBG is the backgate bias. The equation of td demonstrate that in a full-complementary positive feedback differential sense amplifier quicker operation can be obtained by increasing the gain factors βN and βP, by decreasing the parasitic gate source capacitance CGS and gate-drain capacitance CGD of the N- channel and P-channel latch devices MN1, MN2, MP4 and MP5, and by decreasing the bitline capacitance CBL. Additionally, reductions in the fall time of vS (t) and in the rise time of vr(t) also shorten td.

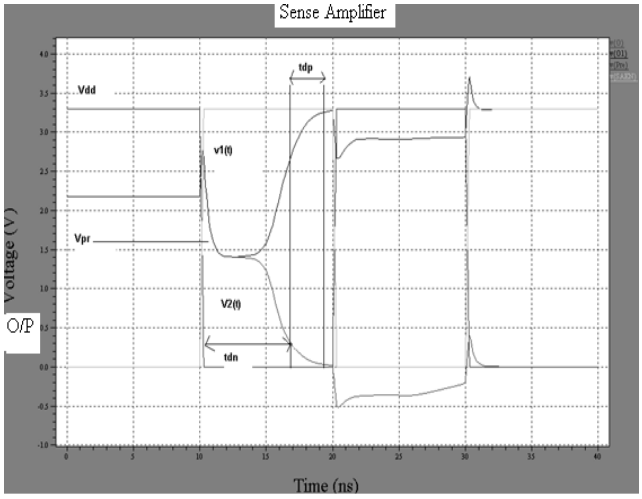

Figure 6: Output Voltage of Sense Amplifier

IV. INPUT DECOUPLED LATCH TYPE SENSE AMPLIFIER

The different architectures described above are susceptible to process variation. Due to process variation like variation in V_T and β of transistors used in architecture, power consumption and probability of failure is more in CLSA than that of VLSA.

Further now, we can decrease the power consumption, probability of failure and sensing delay of CLSA by reducing the offset voltage of CLSA using offset compensation technique for high speed low power SRAM application.[8]Low-power SRAMs have become a critical component of many VLSI chips. This is especially true for embedded memories like on-chip caches. The key to low-power operation in the SRAM is to reduce the signal swings on the high capacitance bit lines. This minimum required signal swing is limited by the offset in the sense amplifier. The higher the offset, the higher is the power consumption and the sense delay. This brings us to the typical trade-off between memory yield and power-delay product. Transistors MP0, MP1**,** MN0 and MN1 form a cross-coupled complementary structure. The speed and loading characteristics of any cross-coupled sense amplifier depend on the conductivity of the discharging chain and the capacitances of cross-coupled nodes. The higher the conductivity and the lower the capacity can speed an amplifier. Discharge chain of sense amplifier consists of only two n channel transistors MN0 (MN1) and MN2, connected in series and thus satisfies the condition on fast discharging the cross coupled nodes. Moreover, this sense amplifier has two decouple transistors isolate the loading of output nodes because the bit line loading is decoupled from the output nodes and a lot of improvement has been made in the sensing delay. However there still exists a current flow, which is caused by the voltage difference between bit lines and output nodes. This is one of the commonly used sense amplifier in high speed memory applications. Without loss of generality we assume that BL_ goes down and BL remains high, when the memory cell is accessed. The offset voltage of the latch is characterized as the minimum input differential voltage between

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BL_ and BL that is required for the correct output of the latch. Ideally the two cross coupled NMOS transistors (MN0 and MN1) and the two PMOS pass transistors (R1 and R2) are perfectly matched. For this ideal case, BL_ can be infinitesimally less than VDD for SAO_ to go down. But due to process variations, perfect matching is not possible, and hence, BL_ needs to be less than VDD by a finite amount for correct reading. This finite value is the offset voltage of the sense amplifier. For the latch output nodes precharged to VDD, mismatch in pull-down NMOS (MN0 and MN1) and input PMOS pass transistors (R1 and R2) contributes to the latch offset. In this thesis, offset contribution

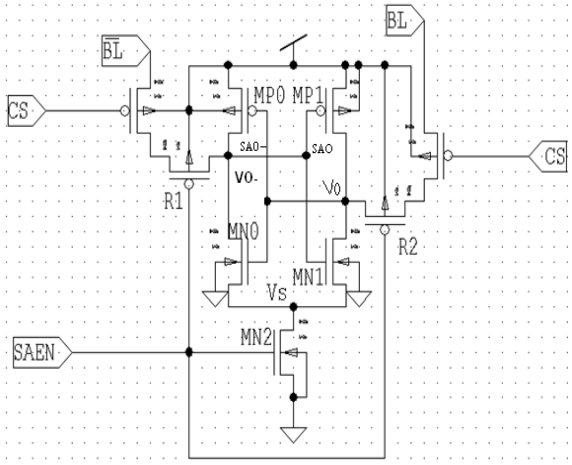

Figure7 input decoupled sense amplifier

From MN0 and MN1 is named as the intrinsic latch offset and that of R1 and R2 as the extrinsic latch offset. The total latch offset is sum of these two offsets. The variations in column pass transistors do not influence the latch offset because column pass transistors remain ON during sensing operation. The pull-up PMOS transistors (MP0 and MP1) do not contribute to the latch offset because they are in subthreshold region during sensing period. It appears that the tail transistor MN2 does not influence the offset, as it is a common mode transistor. But as will be shown in the following discussion, the size of the tail transistor has a significant impact on the latch offset. Also, the rise time of sense enable signal (SAEN), has a very profound influence on both the intrinsic and the extrinsic offset.

A. Intrinsic offset:

Suppose that MN0 is weak transistor and MN1 is strong transistor. When BL_ goes low, MN0 will have Vgs larger than MN1, but V_{DS} smaller than MN1. When the difference between BL_ and BL is less than V_T, both MN0 and MN1 are in saturation. For small output conductance, the current through MN0 and MN1 essentially depends on gate over drive. Thus MN0 can have more drain current, even if MN0 is weak and MN1 is strong, provided BL_ is "suitably lower" than BL. Because of higher drain currentof MN0, SAO_ will discharge more rapidly and sense amplifier will latch into the correct state. The difference in drain currents of MN0 and MN1 resulting from V_T and β variations causes the intrinsic latch offset.

i. Effect of V_s:

V_s should be biased at higher voltage to have smaller offset, and once the latch has started latching in the right direction, VS can be reduced to have rail to rail swing. Thus the SAEN signal should be slower and MN2 should be weaker so that VS falls slowly and remains high at the beginning of latch operation.

ii. Differential Charge Injection (DCI) and Differential Signal Injection (DSI):

The pass transistor R1 has its source connected to BL_, which is at a lower voltage than BL. Also, VT of R1 is more than that of R2 because of body effect. This makes R1 weaker than R2 even when these two transistors are perfectly matched. When SAEN goes from low to high, the node voltages at SAO_ and SAO increase because of capacitive coupling from gates of R1 and R2, respectively. But the resistive conduction of R1/R2 between SAO_/SAO and BL_/BL tends to decrease the effect of this capacitive coupling. Since R1 is weaker than R2, the net increase in voltage at SAO_ is more than SAO. This differential charge injection (DCI) increases the intrinsic latch offset. For longer rise times of SAEN, the capacitive coupling decreases, and hence, DCI decreases.

iii. Output Node Capacitance Mismatch:

For symmetrically laid latch, the output node capacitance mismatch is due to different drain capacitances of transistors connected there. These drain capacitances differ because of different voltages of BL_ and BL and results in capacitance at SAO_ being more than SAO. This capacitance mismatch adds on to the intrinsic offset.

V. SIMULATION RESULT

The figure 8 show the output voltage of sense amplifier and size of transistor MN2 0.54 W (µm) and supply voltage 3.3 volt and simulate using IBM 0.13µm technology . The figure 9 shows the output voltage of Sense Amplifier. It is to read 1 from memory cell. Output voltage shows the logical 1 i.e. V_{dd} .Access time of memory is shown in figure 9 below. It is 3 ns. Precharge signal and sense amplifier enable signal also shown in figure 9.The figure 9 shows the bit line voltage of memory cell. It is to read 1 from memory cell. Difference in bit line voltage is amplified by sense amplifier and gives out when sense amplifier enable signal is enabled. Differential voltage developed between the bit lines is called also offset voltage.

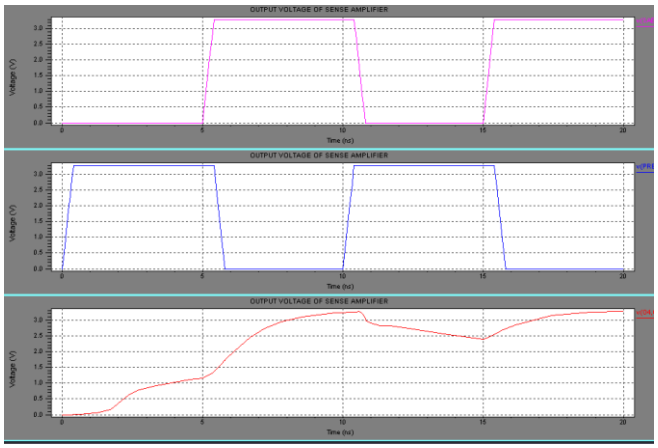

Figure8: Output Voltage of Sense Amplifier

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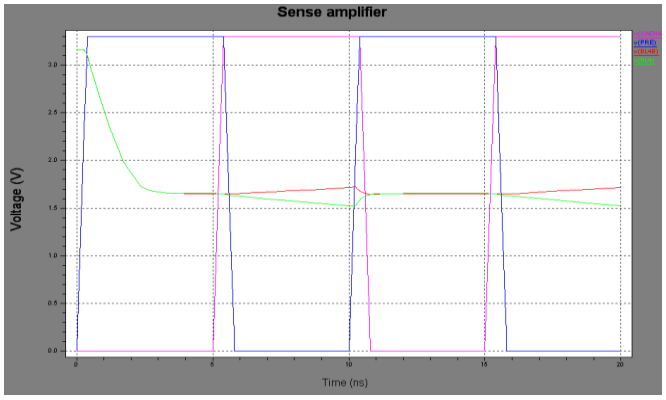

Figure9: Bit Lines Voltage of Memory Cell

VI. CONCLUSION

In this paper present the literature survey and study of sense amplifier for low offset high speed SRAM memory design application and in this paper also study the sense amplifier working, voltage mode sense amplifier and current mode sense amplifier available in literature. In the paper also present the comparison between voltage mode sense amplifier and current mode sense amplifier architecture for low power memory design application. In this paper we literature study transistor mismatch effect on latch type sense amplifier is performed. The total latch offset consists of mainly an intrinsic offset component due to the mismatch in the amplifying NMOS transistors, and an extrinsic offset component due to the PMOS pass transistors. The intrinsic and extrinsic offset voltage is controlled by the source voltage of NMOS transistors differential charge injection and differential signal injection. The higher the rise time of SAEN signal, the lower is the intrinsic offset. A Current mode sense amplifier can be used for low power application but offset compensation is not provided in this case.

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