# Design of Low Power, High Speed Differential Amplifier Ring Voltage Controlled Oscillator in CMOS Technology

**Fahmida Khatoon, Tarana Afrin Chandel**

***Abstract— Designing a compact, power efficient Voltage-Controlled Oscillator (VCO) for high frequency phase lock loop (PLL) in modern wireless communication system is decisively a challenging task. Voltage-Controlled Ring Oscillator are crucial component in many wireless communication systems.VCRO is used in PLL circuit, to generate the oscillations and increase the speed of whole system. In this paper a low power and high speed VCRO is implemented using 250nm CMOS technology provided by generic with 2.5volt power supply. In favour of easy implementation of the module in small die size, a five-stage CMOS differential Voltage Controlled Ring Oscillator has been adopted to fabricate the proposed VCRO.The Voltage Controlled Ring Oscillator is design in Tanner Tool Version 13 environment. Power Consumption should be reduced to improve the performance of the VCRO.We also used of several techniques such as transistor sizing to improve performance of VCRO.Simulated results show that the designed VCRO exhibits an output frequency from 87-910 MHz with tuning voltages of 0.7 V to 2.3 V.The VCRO consumes 0.359mW of power at Vtune=0.7 V supply.***

***Index Terms—CMOS,High Speed, Low Power,VCRO***

## I. INTRODUCTION

As the demand of portable electronic and wireless communication products increases, the attention is provide towards to make devices more portable. The Wireless communication system contains many transceivers such as low noise amplifiers, power amplifiers, mixers and filters[8].The VCO is a critical and essential component in modern wireless communication systems, providing periodic signals required for timing in digital circuits and frequency translation in radio frequency circuits[1].CMOS VCOs with low power consumption, low phase noise and wide tuning range is demanded in the multi-standard wireless communication systems.VCOs are most commonly used building blocks in communication applications like PLL,clock and data recovery circuits[2,3].There are mainly two types of VCOs,Ring oscillator and LC tank.LC based VCO has low level of phase noise among all CMOS VCOs.However ,it has narrow tuning range, greater power dissipation and large die area[4].These shortcomings of LC-VCO are overcome by a ring based VCO or sometimes called as VCRO.The main reason of using ring oscillator in different fields of communication system is a direct consequence of its easy integration.

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Due to their integrated nature, ring oscillators have become one of the most important building block in many digital and communication systems. In addition to improve the performance of the ring oscillator in PLL, various techniques such as transistor sizing have been experimented.

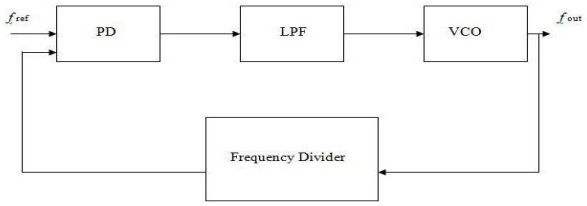


Figure: 1 Block diagram of PLL

The PLL shown in Figure 1 consists of a Phase Detector (PD), Low Pass Filter (LPF) and a frequency divider.
The VCO proposed in this paper use of differential topology that contain of five-stage VCRO which have low power and high speed.

## II. DIFFERENTIAL AND SINGLE-ENDED VCOS

A ring oscillator consists of a number of delay stages, with the output of the last stage fed back to the input of the first. To achieve oscillation, the ring must provide a phase shift of 2π and have unity voltage gain at the oscillation frequency. Ring oscillator structure also employs positive feedback to achieve oscillation [5, 6, and 7].

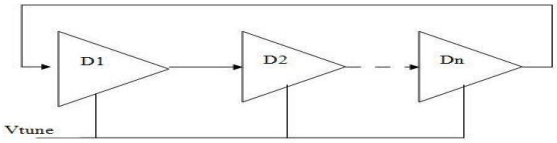


**Figure: 2 N-stage Single Ended Ring VCO**

In the Figure.2 D1 to Dn represents the delay cells, which provide the gain and phase shift. The delay cell for the single-ended VCO is a basic inverter and has the highest frequency of oscillation and minimum power dissipation.

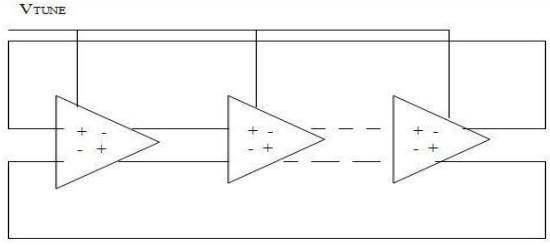


**Figure: 3 N-stage Differential Ring VCO**

The N-stage differential ring voltage controlled oscillator is shown in Figure.3.Differential delay cell rejects the common mode and power supply noise. Therefore to improve the noise performance of ring oscillator, differential delay cell is used.

## III. PROPOSED DIFFERENTIAL AMPLIFIER RING VOLTAGE CONTROLLED OSCILLATOR

Differential amplifier ring VCO is the most standard design for implementing a high speed and low power ring oscillator, and sustained into the analog design market for more than ten years.

Five similar stages of differential amplifier have been shown in Figure.4 where all the stages are connected in cascaded format, and the last stage's output has been the feedback to the input of the first stage. A control block is connected in synchronism with each stage, which basically provides the two way control mechanism of the output frequency. Two biasing potentials Vb1 and Vb2 for the differential stages are also generated from the control block.

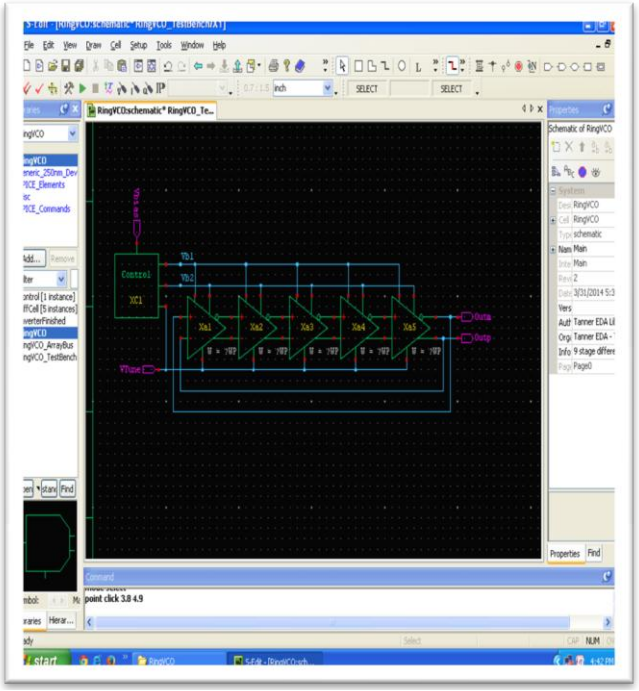

**Figure: 4 Circuit arrangement for Differential Amplifier based ring VCO**

The key role in designing ring VCO is played by Vtune voltage which significantly modulates the current gain of a differential stage. The gain of a differential amplifier therefore varies the output current of the same amplifier which in turn improves the charging time of the output node parasitic capacitor and time delay of a particular stage changes, which in turn changes the overall frequency obtained at the output of the VCO.Therefore, Vtune directly controls the output frequency obtained by the VCO circuit. Using differential amplifier configuration additionally provides the advantage of inverting mode of operation i.e. it gives a phase shift of $\pi$ in each stage.

### A. Control Circuit

The detailed circuit arrangement of the control block has been shown in the Figure.5.The circuit basically reveals the importance of current mirror, which excels in providing the constant and desirable current replica at any part of the circuit.

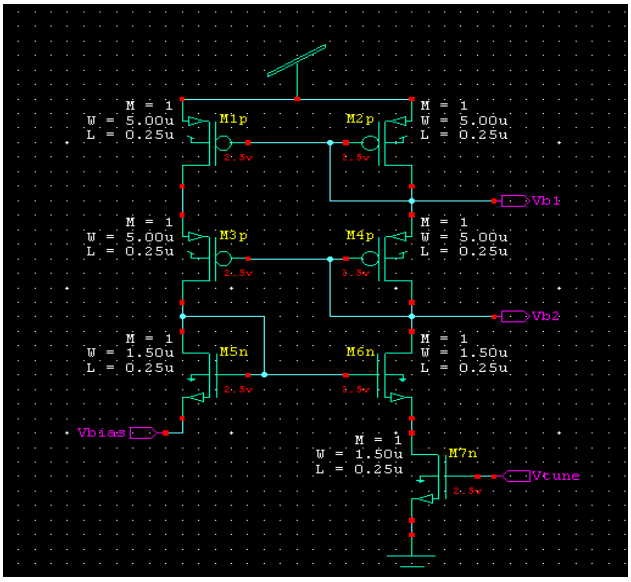


**Figure: 5 Control Circuit**

The control circuit of this VCO design mainly distinguishes it from the other conventional VCO designs based on differential amplifier. This circuit provides an additional control of VCO tuning via. An input Vbias.This Vbias input mainly controls the current of transistor M1p, M3p and M5n.Due to which two biasing potentials are being generated as Vb1 and Vb2 which in addition to Vtune control the output frequency.

### B. Differential Amplifier

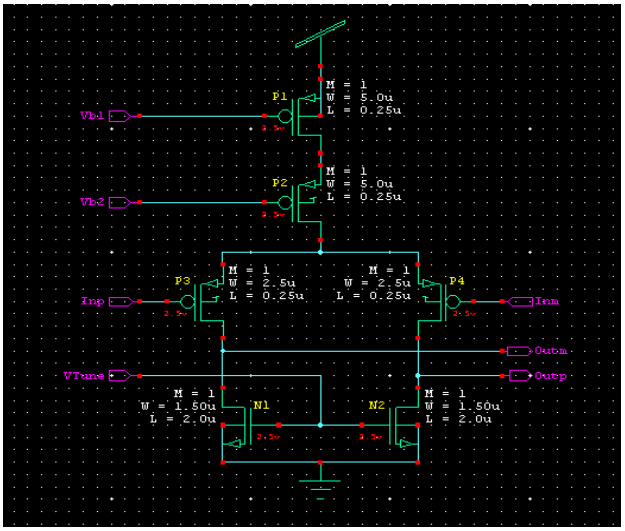


**Figure: 6 Differential Amplifier**

The circuit arrangement of the differential amplifier has been shown in Figure.6. Transistors P3 and P4 are the main driver components (PMOSFETs) for the differential operation purpose, whereas N1 and N2 are serving the purpose of current biasing for the differential design .Current biasing is being achieved by externally controlling the Vtune voltage. Additional current biasing is being controlled by the external Vb1 and Vb2 bias potentials.

## IV. SIMULATION RESULTS

The proposed differential amplifier ring VCO is implemented and simulated with 250nm CMOS technology. The supply voltage required for this design is 2.5V.

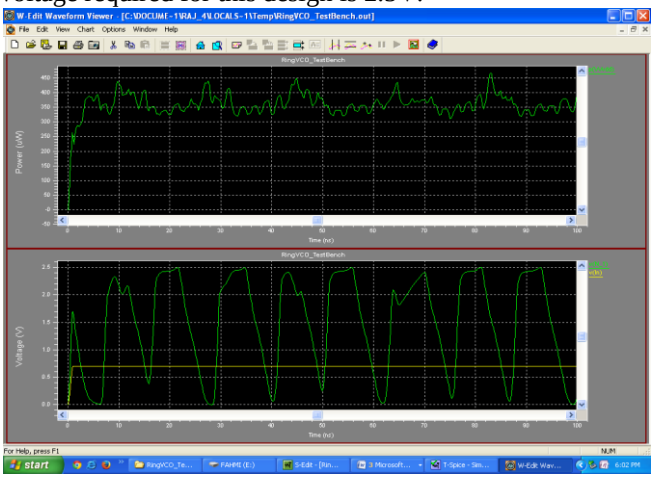

**Figure : 7 Simulation Waveform, when Vtune=0.7V, Power=0.359mW and Speed=87MHz**

When Vtune=0.7V, we have observed the lowest power which is 0.359mW and we obtain the lowest speed that is 87MHz which is shown in Figure.7.

**TABLE 1 : Tuning Voltage (V) Vs Power (mW)**

| Vtune (Volts) | Power (mW) |
|---|---|
| 0.7 | 0.359 |
| 0.8 | 0.612 |
| 0.9 | 0.889 |
| 1.0 | 1.16 |
| 1.1 | 1.42 |
| 1.2 | 1.66 |
| 1.3 | 1.89 |
| 1.4 | 2.13 |
| 1.5 | 2.35 |
| 1.6 | 2.57 |
| 1.7 | 2.75 |
| 1.8 | 2.89 |
| 1.9 | 2.98 |
| 2.0 | 3.03 |
| 2.1 | 3.06 |
| 2.2 | 3.09 |
| 2.3 | 3.11 |

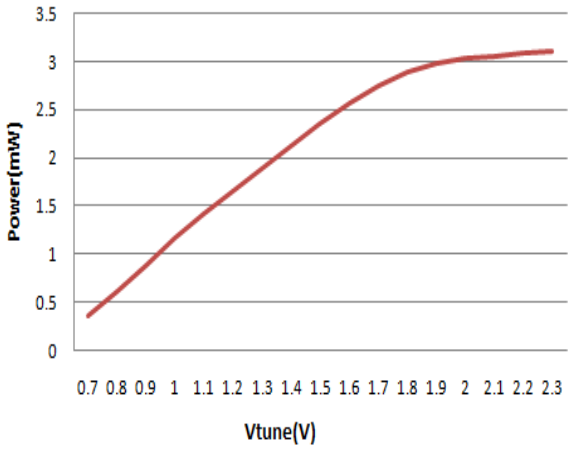


**Figure:8 Power (mW) Vs Tuning Voltage (V)**

When the tuning voltage (V) is varied from 0.7 V to 2.3 V, the power of the designed VCRO ranges from 0.359mW to 3.11mW. Table 1 gives the characteristics of differential amplifier ring VCO i.e. Vtune (V) Vs Power (mW).The graph shown in Figure.8 shows that the relationship between power (mW) Vs tuning voltage (V) is linear.

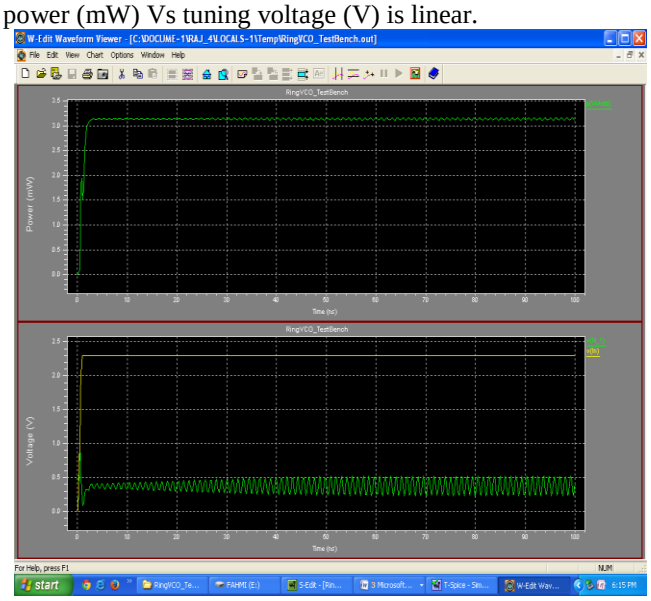

**Figure: 9 Simulation Waveform, when Vtune=2.3V, Power=3.11mW and Speed=910MHz**

When Vtune=2.3V, we have observed that power is 3.11mW and we obtain the highest speed that is 910MHz which is shown in Figure.8.

**TABLE 2 :Vtune (V) Vs Frequency (MHz)**

| Vtune (V) | Frequency (MHz) |
|---|---|
| 0.7 | 87 |
| 0.8 | 133 |
| 0.9 | 186 |
| 1.0 | 218 |
| 1.1 | 268 |
| 1.2 | 332 |
| 1.3 | 397 |

| | |
|---|---|
| 1.4 | 472 |
| 1.5 | 546 |
| 1.6 | 619 |
| 1.7 | 689 |
| 1.8 | 752 |
| 1.9 | 806 |
| 2.0 | 847 |
| 2.1 | 873 |
| 2.2 | 887 |
| 2.3 | 910 |

When the tuning voltage is varied from 0.7 V to 2.3 V, the oscillation frequency of the designed differential amplifier ring VCO ranges from 87 MHz to 910 MHz. Below this voltage ring VCO gives oscillation, but variations are not linear. Due to PMOS based differential ring VCO frequency decreases with an increase in supply voltage. Table 2 gives the characteristics of the differential amplifier ring VCO i.e. frequency (MHz) Vs tuning voltage (V).

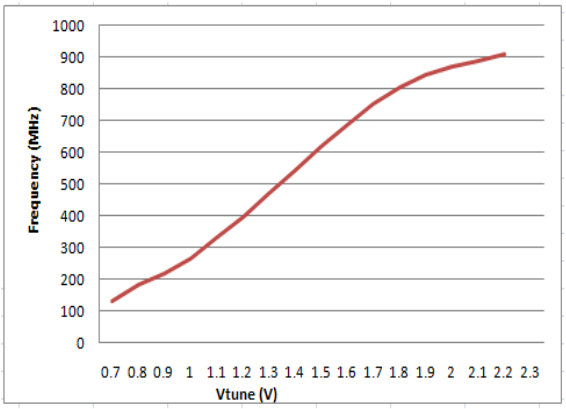


**Figure: 10 Frequency (MHz) Vs Tuning Voltage (V)**

The relationship between frequency and tuning voltage is shown in Figure.10.

**TABLE 3: Final Result of the proposed differential amplifier ring VCO**

| Input tuning range | Power (minimum) | Speed (highest) |
|---|---|---|
| 0.7V-2.3V | 0.359mW | 910 MHz |

## V. CONCLUSION

The proposed design allows implementation of a differential amplifier ring VCO with low power and high speed. The proposed differential amplifier ring VCO is implemented in 250nm CMOS technology. The supply voltage required for this design is 2.5V.From circuit simulations; the oscillation frequency varies from 87 MHz to 910MHz by adjusting the tuning voltage from 0.7V to 2.3V. The low power consumption is achieved which is 0.359mW.

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