Design and Simulation of a Circuit to Predict and Compensate Performance Variability in Submicron Circuit

Sripriya.B.R, Nataraj.K.R

Abstract*— This paper presents a technique for compensating process, voltage and temperature variations due to manufacturing and environmental variability in submicron circuits using canary flip-flop. This canary flip flop predicts the timing error before it actually occurs and compensate the performance so that the system performance does not get affected. I am going to design a 16-bit Brent-Kung adder in 45-nm CMOS technology , whose performance will be controlled by supply voltage scaling. We will show that this technique can compensate process, supply voltage, and temperature variations and improve the energy efficiency of submicron circuits. We also compare Power dissipation for Worst case design and performance compensate design and show performance design has less power dissipation when compared to worst case design.

Index Terms*— Manufacturing variability, Timing error prediction, Brent-Kung adder, Speed control unit, Canary flip-flop.

I. INTRODUCTION

Manufacturing processes necessary to make an integrated circuit (IC) are among the most sophisticated processes ever invented, since they are inherently sensitive to all kinds of disturbances and, as a result, the manufactured IC components exhibit large variations of their electrical parameters [1]. Process-related variability of semiconductor device characteristics has always been a hardest task for IC process engineers and circuit designers. In nanometer scale devices variability approaches the limits determined by the discrete nature of the solid matter and cannot be reduced by means of improvements in manufacturing processes and equipment.

As CMOS transistors are scaled to nanometer feature sizes, variations in transistor performance and leakage has become a critical challenge. There are three main sources of variations Process variation , supply voltage variation and Operating temperature variation.

II. CANARY FLIP-FLOP

Canary FF is augmented with a delay element and a redundant FF named shadow FF, as shown in Figure1. Each FF (main FF) is augmented with a delay buffer and a redundant FF (shadow FF).Timing errors are predicted by comparing the main FF value with that of the shadow FF, which runs into the timing error a little bit before the main FF. Alert signal triggers voltage or frequency control.

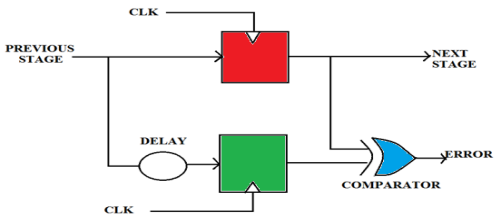

Figure 1 Canary flip-flop

Utilizing canary FFs has the following three advantages.

1. **Elimination of the delayed clock**
2. **Protection offered against timing errors**
3. **Robustness for variations**

III. SPEED CONTROL UNIT

Speed control unit alters speed of the Brent-Kung adder whenever warning signal goes high. Figure. 2 shows a schematic of the speed control unit. Four speed levels can be provided by applying four different voltage. It consists of a 2 bit up/down counter, 2:4 Decoder VDD1, VDD2, VDD3, and VDD4 are selected according to the speed level.

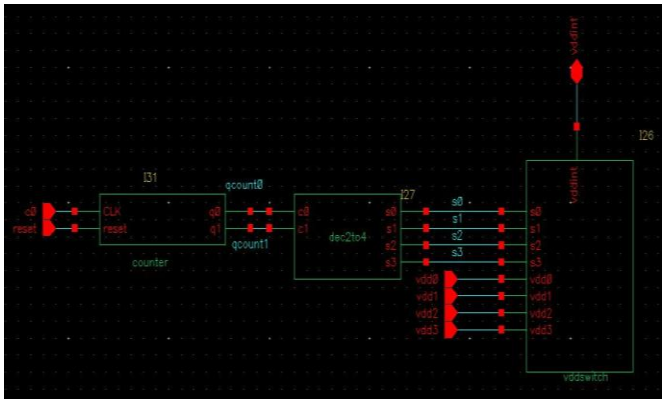

Figure 2. Block Diagram of Speed Control Unit.

IV. BRENT-KUNG ADDER

The Brent-Kung adder is a parallel prefix adder. Parallel prefix adders are special class of adders that are based on the use of generate and propagate signals. The logic depth of Brent-Kung adders increases to 2log (2n-1), so the speed is lower. The block diagram of 4-bit Brent-Kung adder is shown in Figure 3.

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Sripriya.B.R, Department of Electronics and Communication Engineering, SJBIT, Bangalore, India

Dr.Nataraj.K.R, Department of Electronics and Communication Engineering, SJBIT, Bangalore, India

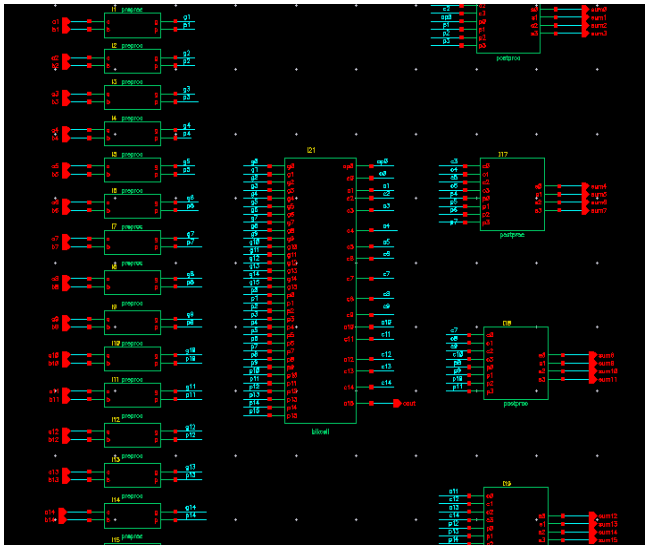

Figure 3. 16 Bit Brent-Kung Adder

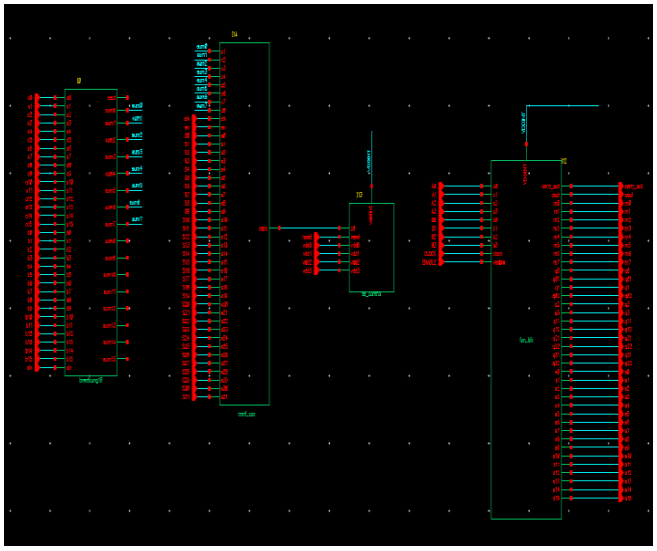

Figure 4. Proposed Block Diagram

V. PROPOSED BLOCK DIAGRAM

The structure of the circuit is as depicted in Figure 4. It consists of Configurable canary flip-flop, Speed control unit, brent-kung adder. A 16-bit Brent-hung adder is adopted as a circuit whose performance is controlled by using speed control unit. The circuit speed is controlled digitally and the term "speed level" is used to describe how fast or slow the circuit is controlled. A higher speed level means the circuit is controlled for faster operation.

The output of Brent-kung adder consists of sum bits as S[0] to S[15], from which only S[0] to s[7] is connected to Configurable canary flip-flop. This uses technique that pads the data-path with a delay element and samples the delayed data-path signal in another flip-flop, called the canary flip-flop, which is as shown in figure 5. Each flip-flop (main flip-flop) is augmented with a delay buffer and a redundant flip-flop (shadow flip-flop). Timing errors are predicted by comparing the main flip-flop value with that of the shadow FF, which runs into the timing error a little bit before the main flip-flop. Alert signal triggers voltage control.

The warning signal is monitored during a specified period. Once the warning signal is detected, which is generated by canary flip-flop , the circuit is controlled to speed up. That means speed gets increased by one level. If no warning signals are observed during the monitoring period, the circuit is slowed down by one level for power reduction. Here each speed level has a difference of 0.1 volt. The speed control unit as in the fig consists of a decoder, 4-bit Counter and a voltage switch. If the warning signal from the configurable canary flip-flop is high and the timer signal is high, then these two bits are given to decoder. Then this output is given to counter which increases the value of decoder by one, that means the speed is increased by one level. Then this value is given to vltage switch, which consists of four pmos each connected to different vdd as in vdd0, vdd1, vdd2, vdd3. Depending upon the output of counter , one out of the four vdd is selected.

VI.RESULTS AND GRAPHS

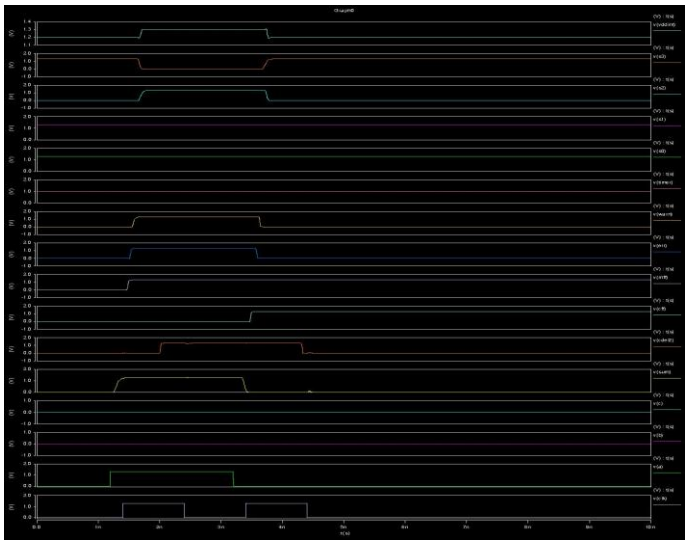

Figure 5.Waveform of CanaryFF with Speed ControlUnit

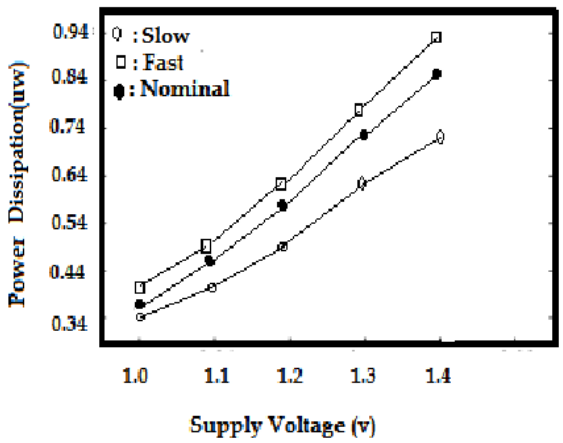

Figure 6.Measurement of power dissipation at various supply voltages at 2 MHz frequency.

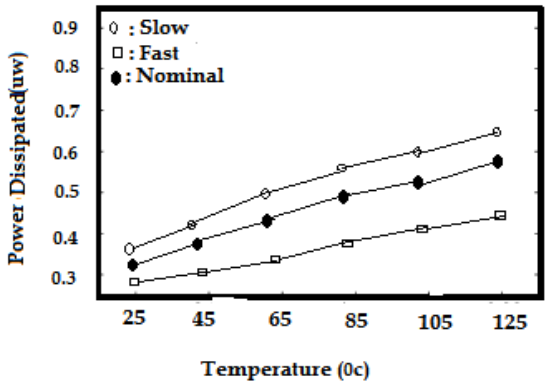

Figure 7. Measurement of Power dissipation at various Temperature conditions at 2 MHz frequency

Figure 6 and 7 shows the variation of Power dissipation for different supply voltage and temperature respectively. Here three Spice models are taken they are slow, fast and nominal. Figure 8 gives the comparison between worst case and performance compensating technique.

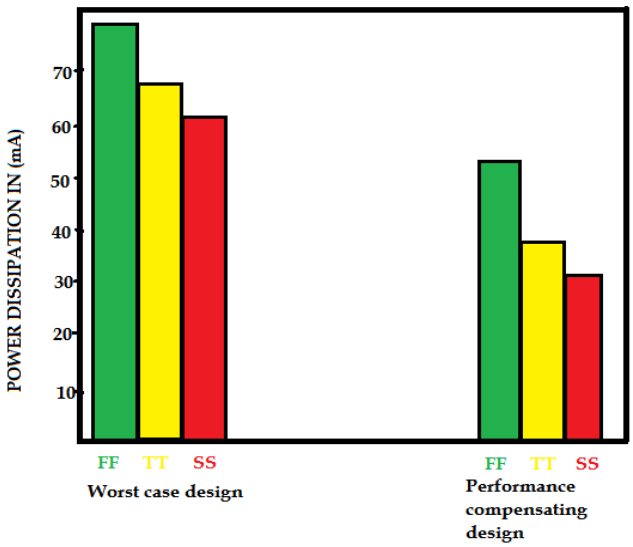

Figure 8 comparisons of worst case and performance compensating designs

VII. CONCLUSION

A performance compensation technique using canary flip-flop for submicron circuits has been disigned. Canary flip-flop, Configurable canary flip-flop and speed control unit is designed in 45nm technology. A 16-bit Brent-Kung adder, whose performance was controlled by speed control unit, was designed in a 45-nm CMOS process using cadence virtuoso tool. Three spice models namely FF, TT and SS are used as design corners to show fast, Nominal and slow chips respectively. Measurement results showed that the adaptive control compensated manufacturing and environmental variability and reduced power dissipation compared to traditional worst-case design. Simulation results indicated that it is appropriate to adjust the buffer delay to attain higher mean time between failures, canary FF insertion with the sufficient buffer delay to cover a wider manufacturing variability space is the most practical.

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AUTHOR PROFILE

Srirpiya.B.R, Mtech(Vlsi and Embedded system) Dept of ECE from SJBIT, Bangalore, BE (ECE) from Global Academy of Technology, Bangalore.

Dr. Nataraj. K. R, HOD and Prof, Dept of ECE, SJBIT, Bangalore. B.E (Electronics & communication) from Siddaganga Institute of Technology Tumkur in the year 1995. M.E (power electronics) First class from BMS college of engineering Bangalore In the year 2000. PhD. (Electronics & Communication) in Dr MGR Deemed University, Chennai, Under the guidance of Dr B.S. Nagabushana PhD (IISce) Director SAN Lab Technologies Bangalore. And Dr S Ramchandran PhD (IIT Madras) in the year August 2010.